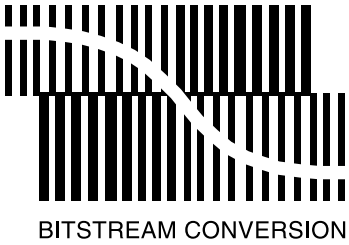
DATA SHEET



UDA1344TS
Low-voltage low-power stereo audio CODEC with DSP features

Preliminary specification
File under Integrated Circuits, IC01

1998 Jul 28

Philips Semiconductors

PHILIPS

Low-voltage low-power stereo audio CODEC with DSP features

UDA1344TS

FEATURES

General

- Low power consumption
- 3.0 V power supply
- 256, 384 and 512f_s system clock
- Support sampling frequencies from 16 to 48 kHz
- Non-inverting ADC plus integrated high pass filter to cancel DC offset
- The ADC supports 2 V (RMS) input signals
- Overload detector for easy record level control
- Separate power control for ADC and DAC
- Integrated digital interpolation filter plus non-inverting DAC
- Functions controllable either by L3 microcontroller interface or via static pins
- The UDA1344TS is pin and function compatible with the UDA1340M
- Small package size (SSOP28)
- Easy application.

Multiple format input interface

- I^2S-bus, MSB-justified and LSB-justified 16, 18 and 20 bits format compatible
- Three combined data formats with MSB data output and LSB 16, 18 and 20 bits data input
- 1f_s input and output format data rate.

DAC digital sound processing

The sound processing features of the UDA1344TS can only be used in L3 microcontroller mode.

- Digital tone control, bass boost and treble
- Digital dB-linear volume control (low microcontroller load) via L3 microcontroller
- Digital de-emphasis for 32, 44.1 and 48 kHz f_s
- Soft mute.

BITSTREAM CONVERSION

Advanced audio configuration

- Stereo single-ended input configuration
- Stereo line output (under microcontroller volume control), no post filter required
- Power-down click prevention circuitry
- High linearity, dynamic range and low distortion.

GENERAL DESCRIPTION

The UDA1344TS is a single-chip stereo Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) with signal processing features employing bitstream conversion techniques. The low power consumption and low voltage requirements make the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates recording and playback functions.

The UDA1344TS supports the I^2S-bus data format with word lengths of up to 20 bits, the MSB-justified data format with word lengths of up to 20 bits and the LSB justified serial data format with word lengths of 16, 18 and 20 bits. The UDA1344TS also supports three combined data formats with MSB-justified data output and LSB 16, 18 and 20 bits data input.

The UDA1344TS can be used either with static pin control or under L3 microcontroller interface. Under L3 control the UDA1344TS has special sound processing features in playback mode such as de-emphasis, volume control, bass boost, treble and soft mute.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1344TS	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$V_{DDA(ADC)}$	ADC analog supply voltage		2.7	3.0	3.6	V
$V_{DDA(DAC)}$	DAC analog supply voltage		2.7	3.0	3.6	V
V_{DDO}	operational amplifiers supply voltage		2.7	3.0	3.6	V
V_{DDD}	digital supply voltage		2.7	3.0	3.6	V
$I_{DDA(ADC)}$	ADC supply current	operation mode	–	9.0	11.0	mA
		ADC power-down	–	3.5	5.0	mA
$I_{DDA(DAC)}$	DAC supply current	operation mode	–	4.0	6.0	mA
		DAC power-down	–	25	75	μA
I_{DDO}	operational amplifier supply current	operation mode	–	4.0	6.0	mA
		DAC power-down	–	250	350	μA
I_{DDD}	digital supply current	operation mode	–	6.0	9.0	mA
$I_{pd(ADC)}$	digital ADC power-down supply current		–	2.5	4.0	mA
$I_{pd(DAC)}$	digital DAC power-down supply current		–	3.5	5.0	mA
T_{amb}	operating ambient temperature		–20	–	+85	°C
Analog-to-digital converter						
$V_{i(rms)}$	input voltage (RMS value)	notes 1 and 2	–	1.0	–	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–80	dB
		at –60 dB; A-weighted	–	–35	–30	dB
S/N	signal-to-noise ratio	V_i = 0 V; A-weighted	–	95	–	dB
α_{cs}	channel separation		–	100	–	dB
Digital-to-analog converter						
$V_{o(rms)}$	output voltage (RMS value)	notes 3 and 4	–	900	–	mV
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–90	–85	dB
		at –60 dB; A-weighted	–	–37	–	dB
S/N	signal-to-noise ratio	code = 0; A-weighted	–	100	–	dB
α_{cs}	channel separation		–	100	–	dB
Power performance						
P_{ADDA}	power consumption in record and playback mode		–	69	–	mW
P_{DA}	power consumption in playback only mode		–	42	–	mW
P_{AD}	power consumption in record only mode		–	37.5	–	mW
P_{PD}	power consumption in power-down mode		–	17	–	mW

Notes

1. The input voltage can be up to 2 V (RMS) when the current through the ADC input pin is limited to about 1 mA by using a series resistor.
2. The input voltage to the ADC scales inversely proportional with respect to the power supply.
3. The output voltage of the UDA1344TS differs from the output voltage of the UDA1340M.
4. The output of the DAC scales proportional with the power supply voltage.

BLOCK DIAGRAM

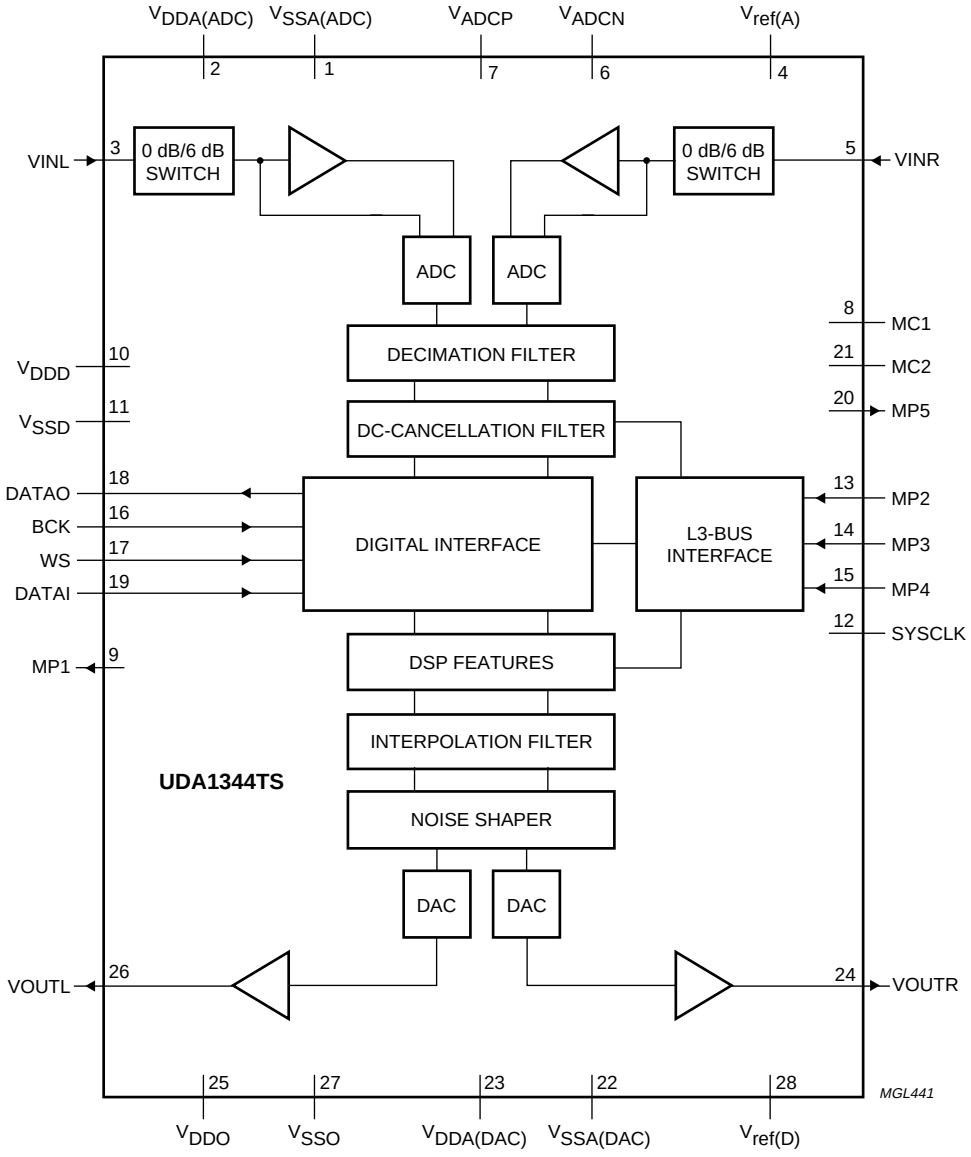


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{SSA(ADC)}$	1	ADC analog ground
$V_{DDA(ADC)}$	2	ADC analog supply voltage
VINL	3	ADC input left
$V_{ref(A)}$	4	ADC reference voltage
VINR	5	ADC input right
V_{ADCN}	6	ADC negative reference voltage
V_{ADCP}	7	ADC positive reference voltage
MC1	8	mode control 1 (pull-down)
MP1	9	multi purpose pin 1
V_{DDD}	10	digital supply voltage
V_{SSD}	11	digital ground
SYSCLK	12	system clock 256, 384 or 512f_s
MP2	13	multi purpose pin 2
MP3	14	multi purpose pin 3
MP4	15	multi purpose pin 4
BCK	16	bit clock input
WS	17	word select input
DATAO	18	data output
DATAI	19	data input
MP5	20	multi purpose pin 5 (pull down)
MC2	21	mode control 2 (pull-down)
$V_{SSA(DAC)}$	22	DAC analog ground
$V_{DDA(DAC)}$	23	DAC analog supply voltage
VOUTR	24	DAC output right
V_{DDO}	25	operational amplifier supply voltage
VOUTL	26	DAC output left
V_{SSO}	27	operational amplifier ground
$V_{ref(D)}$	28	DAC reference voltage

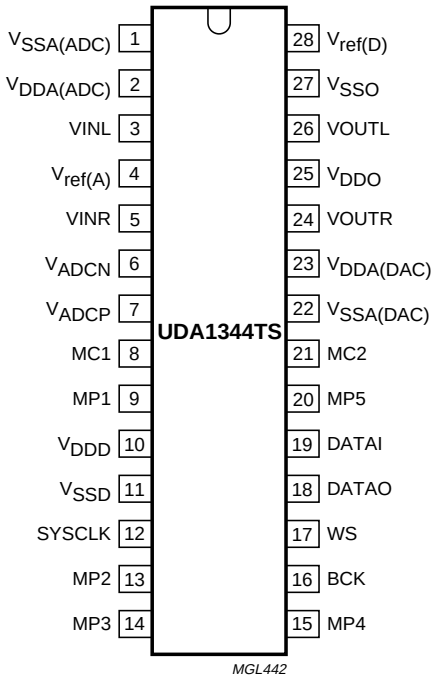


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The UDA1344TS accommodates slave mode only, this means that in all applications the system devices must provide the system clock.

The system clock must be locked in frequency to the audio digital interface input signals.

Analog-to-Digital Converter (ADC)

The stereo ADC of the UDA1344TS consists of two 3rd-order Sigma-Delta modulators. They have a modified Ritchie-coder architecture in a differential switched capacitor implementation. The over-sampling ratio is 128.

In contrast to the UDA1340M, the UDA1344TS supports 1 V (RMS) input and can be set, via an external resistor, to support 2 V (RMS) input.

Analog front-end

The analog front-end is equipped with a selectable 0 dB or 6 dB gain block (the pin to select this mode is given in Section “L3 microcontroller mode”. This block can be used in applications in which both 1 V (RMS) and 2 V (RMS) input signals can be input to the UDA1344TS.

In applications in which 2 V (RMS) is used as input signal, a 12 kΩ must be used in series with the input of the ADC. This makes a voltage divider with the internal ADC resistor and makes sure only 1 V (RMS) maximum is put into the IC. Using this application for a 2 V (RMS) input signal, the switch must be set to 0 dB. When a 1 V (RMS) input signal is input to the ADC in the same application, the gain switch must be set to 6 dB.

In Table 1 an overview is given of the maximum input voltages allowed against the presence of an external resistor and the setting of the gain switch.

Table 1 Application modes using input gain stage

RESISTOR (12 kΩ)	INPUT GAIN SWITCH	MAXIMUM INPUT VOLTAGE
Present	0 dB	2 V (RMS) input signal
Present	6 dB	1 V (RMS) input signal
Absent	0 dB	1 V (RMS) input signal
Absent	6 dB	0.5 V (RMS) input signal

Decimation filter (ADC)

The decimation from $128f_s$ is performed in two stages.

The first stage realizes 3rd-order $\frac{\sin x}{x}$ characteristic.

This filter decreases the sample rate by 16. The second stage, an FIR filter, consists of 3 half-band filters, each decimating by a factor of 2.

Table 2 Decimation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Passband ripple	$0 - 0.45f_s$	±0.05
Stopband	$>0.55f_s$	–60
Dynamic range	$0 - 0.45f_s$	108
Overall gain when 0 dB signal is input to ADC to digital output	DC	–1.16

Mute (ADC)

On recovery from power-down or switching on of the system clock, the serial data output DATAO is held LOW until valid data is available from the decimation filter. This time depends on whether the DC cancellation filter is selected:

DC cancel off: time = $\frac{1024}{f_s}$

t = 23.2 ms when f_s = 44.1 kHz

DC cancel on: time = $\frac{12288}{f_s}$

t = 279 ms when f_s = 44.1 kHz

Interpolation filter (DAC)

The digital filter interpolates from 1 to $128f_s$ by means of a cascade of a recursive filter and an FIR filter.

Table 3 Interpolation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Passband ripple	$0 - 0.45f_s$	±0.03
Stopband	$>0.55f_s$	–50
Dynamic range	$0 - 0.45f_s$	108
Gain	DC	–3.5

Noise shaper (DAC)

The 3rd-order noise shaper operates at $128f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a filter stream digital-to-analog converter.

The Filter Stream DAC (FSDAC)

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post-filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC scales proportionally with the power supply voltage.

L3MODE or static pin control

The UDA1344TS can be used under L3 microcontroller interface mode or under static pin control. The mode can be set via the Mode Control (MC) pins MC1 (pin 8) and MC2 (pin 21). The function of these pins is given in Table 4.

Table 4 Mode Control pins MC1 and MC2

MODE	MC2	MC1
L3MODE	LOW	LOW
Test modes	LOW	HIGH
	HIGH	LOW
Static pin mode	HIGH	HIGH

Important: in L3MODE the UDA1344TS is completely pin and function compatible with the UDA1340M.

L3 microcontroller mode

The UDA1344TS is set to the L3 microcontroller mode by setting both MC1 (pin 8) and MC2 (pin 21) LOW.

The definition of the control registers is given in Section “L3 interface”.

Pinning definition

The pinning definition under L3 microcontroller interface is given in Table 5.

Table 5 Pinning definition under L3 control

SYMBOL	PIN	DESCRIPTION
MP1	9	overload
MP2	13	L3-bus mode input
MP3	14	L3-bus clock input
MP4	15	L3-bus data input
MP5	20	ADC 1 or 2 V (RMS) input control

System clock

Under L3 control the options are 256, 384 and 512f_s.

Multiple format input/output interface

The UDA1344TS supports the following data input/output formats under L3 control:

- I^2S-bus with data word length of up to 20 bits
- MSB-justified serial format with data word length of up to 20 bits
- LSB-justified serial format with data word lengths of 16, 18 or 20 bits
- Three combined data formats with MSB data output and LSB 16, 18 and 20 bits LSB data input.

The formats are illustrated in Fig.3. Left and right data-channel words are time multiplexed.

ADC input voltage control

The UDA1344TS supports 2 V (RMS) input using a series resistor of 12 kΩ as described in Section “Analog front-end”. In L3 microcontroller mode, the gain can be selected via pin MP5.

When MP5 is set LOW 0 dB gain is selected. When MP5 is set HIGH 6 dB gain is selected.

Overload detection (ADC)

In practice the output is used to indicate whenever the output data, in either the left or right channel, is greater than –1 dB (actual figure is –1.16 dB) of the maximum possible digital swing. When this condition is detected the OVERFL output is forced HIGH for at least 512f_s cycles (11.6 ms at f_s = 44.1 kHz). This time-out is reset for each infringement.

DC CANCELLATION FILTER (ADC)

An optional IIR high-pass filter is provided to remove unwanted DC components. The operation is selected by the microcontroller via the L3-bus. The filter characteristics are given in Table 6.

Table 6 DC cancellation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Passband ripple		none
Passband gain		0
Droop	at $0.00045f_s$	0.031
Attenuation at DC	at $0.00000036f_s$	>40
Dynamic range	$0 – 0.45f_s$	>110

Static pin mode

The UDA1344TS is set to static pin control mode by setting both MC1 (pin 8) and MC2 (pin 21) HIGH.

PINNING DEFINITION

The pinning definition under static pin control is given in Table 7.

Table 7 Pinning definition for static pin control

SYMBOL	PIN	DESCRIPTION
MP1	9	data input/output setting
MP2	13	three level pin controlling deemphasis and mute
MP3	14	$256f_s$ or $384f_s$ system clock
MP4	15	three-level pin to control ADC power mode and 1 V (RMS) or 2 V (RMS) input
MP5	20	data input/output setting

SYSTEM CLOCK

Under static pin control the options are $256f_s$ and $384f_s$. With pin MP3 (pin 14) the mode can be set as is given in Table 8.

Table 8 System clock settings under static pin mode

MODE	MP3
$256f_s$ clock mode	LOW
$384f_s$ clock mode	HIGH

MUTE AND DE-EMPHASIS

Under static pin control via MP2 we can select de-emphasis and mute. The definition of the MP2 pin is given in Table 9.

Table 9 Settings for pin MP2

MODE	MP2
No de-emphasis and mute	LOW
De-emphasis 44.1 kHz	$0.5V_{DDD}$
Muted	HIGH

MULTIPLE FORMAT INPUT/OUTPUT INTERFACE

The data input/output formats supported under static pin control.

- I^2S-bus with data word length of up to 20 bits
- MSB justified serial format with data word length of up to 20 bits
- Two combined data formats with MSB data output and LSB 16 and 20 bits LSB data input.

The data formats can be selected using pins MP1 (pin 9) and MP5 (pin 20) as given in Table 10.

Table 10 Data format settings under static pin control

INPUT FORMAT	MP1	MP5
MSB mode	LOW	LOW
I^2S-bus	LOW	HIGH
MSB output LSB 20 input	HIGH	LOW
MSB output LSB 16 input	HIGH	HIGH

The formats are illustrated in Fig.3. Left and right data channel words are time multiplexed.

ADC INPUT VOLTAGE CONTROL

The UDA1344TS supports 2 V (RMS) input using a series resistor as is described in Section “Analog front-end”.

In static pin mode the three-level pin MP4 (pin 15) is used to select 0 or 6 dB gain mode. When MP4 is set LOW the ADC is powered down. When MP4 is set to half the power supply voltage, then 6 dB gain is selected, and when MP4 is set HIGH then 0 dB gain is selected.

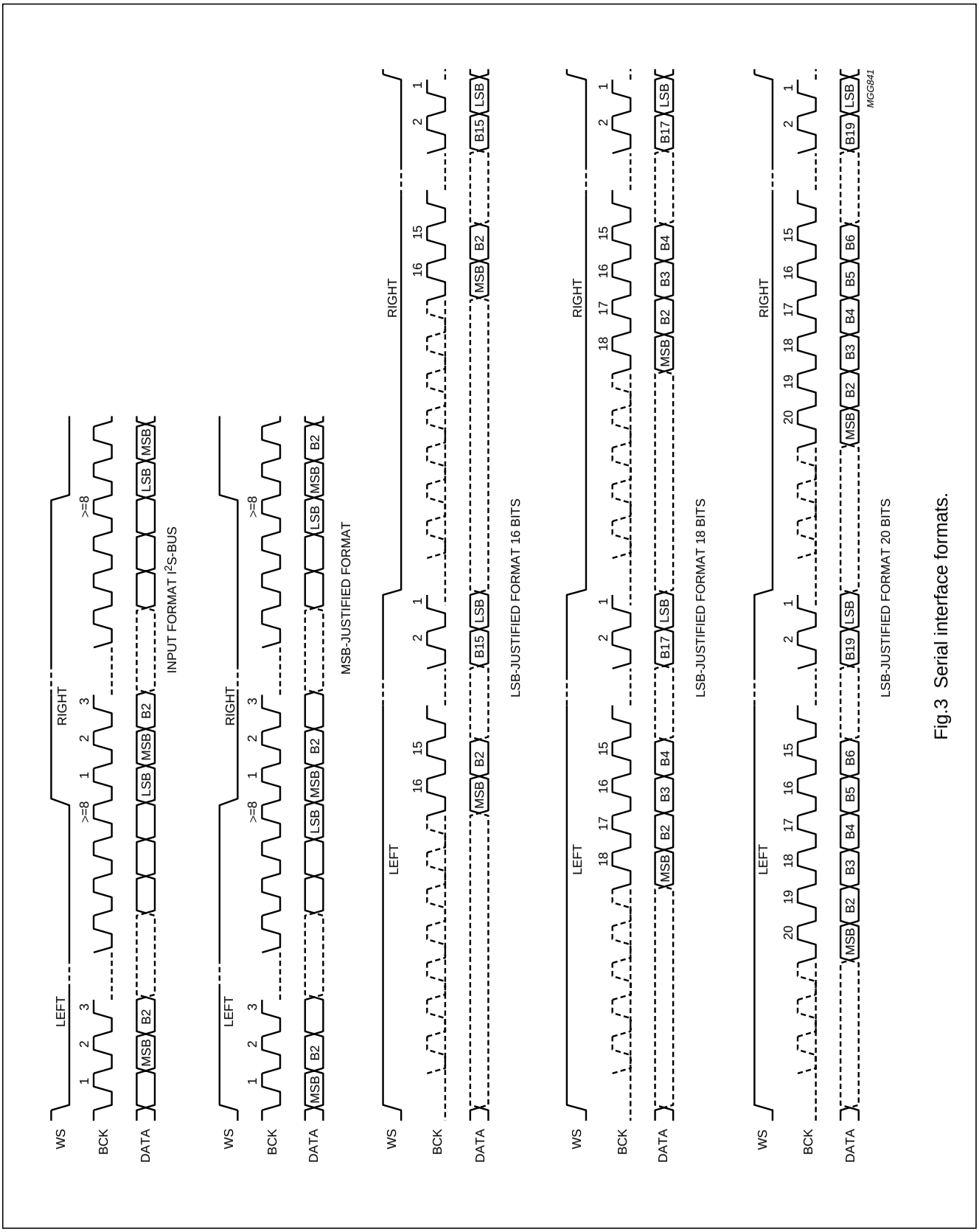


Fig.3 Serial interface formats.

L3 interface

The UDA1344TS has a microcontroller input mode. In the microcontroller mode, all the digital sound processing features and the system controlling features can be controlled by the microcontroller. The controllable features are:

- System clock frequency
- Data input format
- Power control
- DC-filtering
- De-emphasis
- Volume
- Flat/min./max. switch
- Bass boost
- Treble
- Mute.

The exchange of data and control information between the microcontroller and the UDA1344TS is accomplished through a serial hardware interface comprising the following pins:

L3DATA: microcontroller interface data line

L3MODE: microcontroller interface mode line

L3CLOCK: microcontroller interface clock line.

Information transfer via the microcontroller bus is organized in accordance with the so called ‘L3’ format, in which two different modes of operation can be distinguished; address mode and data transfer mode (see Figs 4 and 5).

The address mode is required to select a device communicating via the L3-bus and to define the destination registers for the data transfer mode. Data transfer for the UDA1344TS can only be in one direction, input to the UDA1344TS to program its sound processing and other functional features.

ADDRESS MODE

The address mode is used to select a device for subsequent data transfer and to define the destination registers. The address mode is characterized by L3MODE being LOW and a burst of 8 pulses on L3CLOCK, accompanied by 8 data bits. The fundamental timing is shown in Fig.4. Data bits 0 to 1 indicate the type of subsequent data transfer as given in Table 11.

Table 11 Selection of data transfer

BIT 1	BIT 0	TRANSFER
0	0	DATA (volume, bass boost, treble, de-emphasis, mute, mode and power control)
0	1	not used
1	0	STATUS (system clock frequency, data input format and DC-filter)
1	1	not used

Data bits 7 to 2 represent a 6-bit device address, with bit 7 being the MSB and bit 2 the LSB. The address of the UDA1344TS is 000101 (bit 7 to bit 2). In the event that the UDA1344TS receives a different address, it will deselect its microcontroller interface logic.

DATA TRANSFER MODE

The selection preformed in the address mode remains active during subsequent data transfers, until the UDA1344TS receives a new address command.
The fundamental timing of data transfers is essentially the same as in the address mode, shown in Fig.4.
The maximum input clock and data rate is $64f_s$.
All transfers are byte wise, i.e. they are based on groups of 8 bits. Data will be stored in the UDA1344TS after the eighth bit of a byte has been received. A multibyte transfer is illustrated in Fig.6.

Programming the sound processing and other features

The sound processing and other feature values are stored in independent registers. The first selection of the registers is achieved by the choice of data type that is transferred. This is performed in the address mode, bit 1 and bit 0 (see Table 11). The second selection is performed by the 2 MSBs of the data byte (bit 7 and bit 6). The other bits in the data byte (bit 5 to bit 0) is the value that is placed in the selected registers.

When the data transfer of type ‘data’ is selected, the features Volume, Bass boost, Treble, De-emphasis, Mute, Mode and Power control can be controlled. When the data transfer of type ‘status’ is selected, the features system clock frequency, data input format and DC-filter can be controlled.

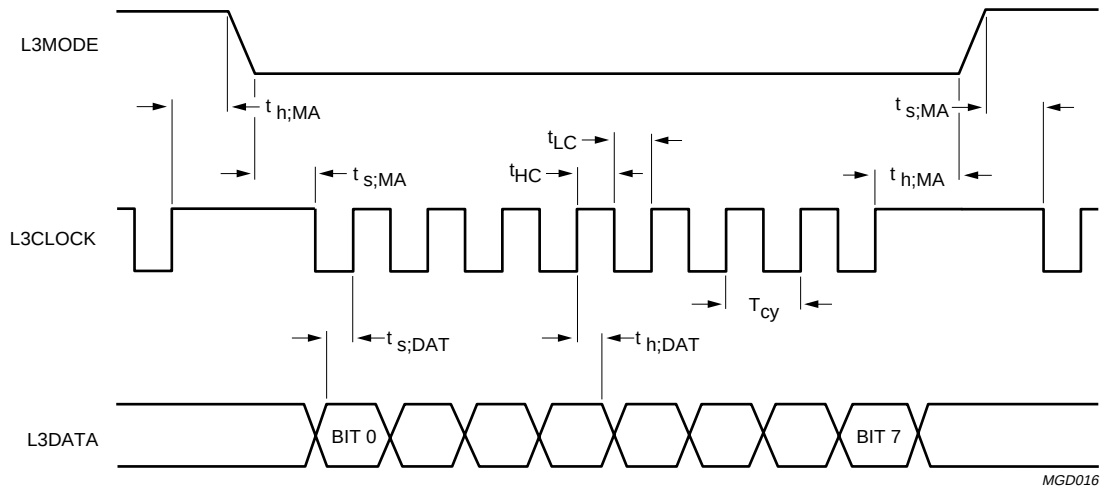


Fig.4 Timing address mode.

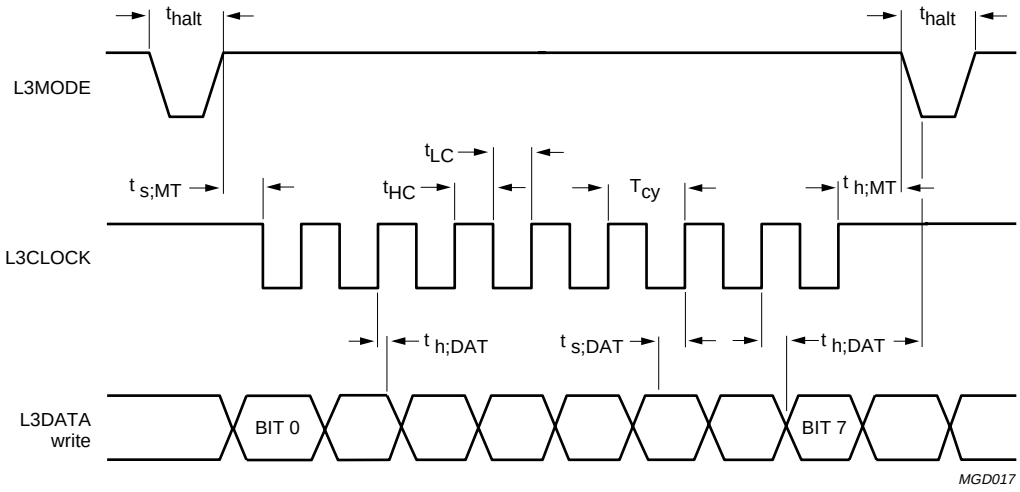


Fig.5 Timing for data transfer mode.

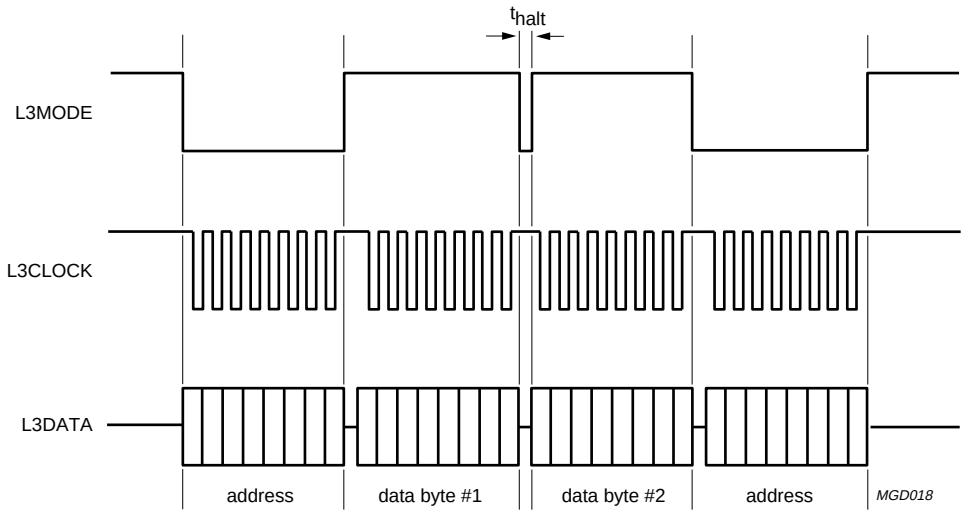


Fig.6 Multibyte transfer.

Table 12 Data transfer of type ‘status’

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER SELECTED
0	0	SC1	SC0	IF2	IF1	IF0	DC	System Clock frequency (5 : 4) data Input Format (3 : 1) DC-filter

Table 13 Data transfer of type ‘data’

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER SELECTED
0	0	VC5	VC4	VC3	VC2	VC1	VC0	VOLUME CONTROL (5 : 0)
0	1	BB3	BB2	BB1	BB0	TR1	TR0	BASS BOOST (5 : 2) TREBLE (1 : 0)
1	0	0	DE1	DE0	MT	M1	M0	DE-EMPHASIS (4 : 3) MUTE MODE (1 : 0)
1	1	0	0	0	0	PC1	PC0	POWER CONTROL (1 : 0)

System clock frequency

A 2-bit value (SC1 and SC0) to select the used external clock frequency (see Table 14).

Table 14 System clock frequency settings

SC1	SC0	FUNCTION
0	0	$512f_s$
0	1	$384f_s$
1	0	$256f_s$
1	1	not used

Data input format

A 3-bit value (IF2 to IF0) to select the used data format (see Table 15).

Table 15 Data input format settings

IF2	IF1	IF0	FUNCTION
0	0	0	I^2S-bus
0	0	1	LSB-justified; 16 bits
0	1	0	LSB-justified; 18 bits
0	1	1	LSB-justified; 20 bits
1	0	0	MSB-justified
1	0	1	MSB-justified output/LSB justified 16 bits input
1	1	0	MSB-justified output/LSB justified 18 bits input
1	1	1	MSB-justified output/LSB justified 20 bits input

DC filter

A 1-bit value to enable the digital DC-filter (see Table 16).

Table 16 DC-filtering

DC	FUNCTION
0	no DC-filtering
1	DC-filtering

Volume control

A 6-bit value to program the left and right channel volume attenuation (VC5 to VC0). The range is 0 dB to –∞ dB in steps of 1 dB (see Table 17).

Table 17 Volume settings

VC5	VC4	VC3	VC2	VC1	VC0	VOLUME (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	–1
0	0	0	0	1	1	–2
:	:	:	:	:	:	:
1	1	1	0	1	1	–58
1	1	1	1	0	0	–59
1	1	1	1	0	1	–60
1	1	1	1	1	0	–∞
1	1	1	1	1	1	–∞

Bass boost

A 4-bit value to program the bass boost setting. The used set depends on the mode bits.

Table 18 Bass boost settings

BB3	BB2	BB1	BB0	BASS BOOST		
				FLAT SET (dB)	MIN. SET (dB)	MAX. SET (dB)
0	0	0	0	0	0	0
0	0	0	1	0	2	2
0	0	1	0	0	4	4
0	0	1	1	0	6	6
0	1	0	0	0	8	8
0	1	0	1	0	10	10
0	1	1	0	0	12	12
0	1	1	1	0	14	14
1	0	0	0	0	16	16
1	0	0	1	0	18	18
1	0	1	0	0	18	20
1	0	1	1	0	18	22
1	1	0	0	0	18	24
1	1	0	1	0	18	24
1	1	1	0	0	18	24
1	1	1	1	0	18	24

Treble

A 2-bit value to program the treble setting. The used set depends on the mode bits.

Table 19 Treble settings

TR1	TR0	TREBLE		
		FLAT SET (dB)	MIN. SET (dB)	MAX. SET (dB)
0	0	0	0	0
0	1	0	2	2
1	0	0	4	4
1	1	0	6	6

De-emphasis

A 2-bit value to enable the digital de-emphasis filter.

Table 20 De-emphasis settings

DE1	DE0	FUNCTION
0	0	no de-emphasis
0	1	de-emphasis; 32 kHz
1	0	de-emphasis; 44.1 kHz
1	1	de-emphasis; 48 kHz

Mute

A 1-bit value to enable the digital mute.

Table 21 Mute

MT	FUNCTION
0	no muting
1	muting

Mode

A 2-bit value to program the mode of the sound processing filters of Bass Boost and Treble. There are three modes: flat, min. and max.

Table 22 The flat/min./max. switch

M1	M0	FUNCTION
0	0	flat
0	1	min.
1	0	min.
1	1	max.

Power control

A 2-bit value to disable the ADC and/or DAC to reduce power consumption.

Table 23 Power control settings

PC1	PC0	FUNCTION	
		ADC	DAC
0	0	off	off
0	1	off	on
1	0	on	off
1	1	on	on

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). All voltages referenced to ground, $V_{DDD} = V_{DDA} = V_{DDO} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	note 1	–	5.0	V
$T_{xtal(max)}$	maximum crystal temperature		–	150	°C
T_{stg}	storage temperature		–65	+125	°C
T_{amb}	operating ambient temperature		–20	+85	°C
V_{es}	electrostatic handling	note 2	–3000	+3000	V
		note 3	–300	+300	V

Notes

1. All V_{DD} and V_{SS} connections must be made to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor via a 2.5 μH series inductor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	90	K/W

DC CHARACTERISTICS

$V_{DDD} = V_{DDA} = V_{DDO} = 3.0$ V; $T_{amb} = 25$ °C; $R_L = 5$ kΩ; note 1; all voltages referenced to ground (pins 1, 11, 22 and 27); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$V_{DDA(ADC)}$	ADC analog supply voltage		2.7	3.0	3.6	V
$V_{DDA(DAC)}$	DAC analog supply voltage		2.7	3.0	3.6	V
V_{DDO}	operational amplifiers supply voltage		2.7	3.0	3.6	V
V_{DDD}	digital supply voltage		2.7	3.0	3.6	V
$I_{DDA(ADC)}$	ADC supply current	operation mode	–	9.0	11.0	mA
		ADC power-down	–	3.5	5.0	mA
$I_{DDA(DAC)}$	DAC supply current	operation mode	–	4.0	6.0	mA
		DAC power-down	–	25	75	μA
I_{DDO}	operational amplifier supply current	operation mode	–	4.0	6.0	mA
		DAC power-down	–	250	300	μA
I_{DDD}	digital supply current	operation mode	–	6.0	9.0	mA
		DAC power-down	–	2.5	4.0	mA
		ADC power-down	–	3.5	5.0	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital input pins						
V_{IH}	HIGH-level input voltage		$0.8V_{DDD}$	–	V_{DDD} + 0.5	V
V_{IL}	LOW-level input voltage		–0.5	–	$0.2V_{DDD}$	V
$\|I_{LI}\|$	input leakage current		–	–	10	μA
C_i	input capacitance		–	–	10	pF
Three-level input pins (MP2; MP4)						
V_{IH}	HIGH-level input voltage		$0.9V_{DDD}$	–	V_{DDD} + 0.5	V
V_{IM}	MIDDLE-level input voltage		$0.4V_{DDD}$	–	$0.6V_{DDD}$	V
V_{IL}	LOW-level input voltage		–0.5	–	$0.1V_{DDD}$	V
Digital output pins						
V_{OH}	HIGH-level output voltage	I_{OH} = –2 mA	$0.85V_{DDD}$	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	–	–	0.4	V
Analog-to-digital converter						
V_{ref}	reference voltage	with respect to V_{SSA}	$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
$R_{o(ref)}$	$V_{ref(A)}$ reference output resistance	pin 4	–	24	–	kΩ
R_i	input resistance	1 kHz	–	9.8	–	kΩ
C_i	input capacitance		–	20	–	pF
Digital-to-analog converter						
V_{ref}	reference voltage	with respect to V_{SSA}	$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
$R_{o(ref)}$	$V_{ref(D)}$ reference output resistance	pin 28	–	28	–	kΩ
R_o	DAC output resistance		–	0.13	3.0	Ω
$I_{o(max)}$	maximum output current	(THD + N)/S < 0.1% R_L = 5 kΩ	–	0.22	–	mA
R_L	load resistance		3	–	–	kΩ
C_L	load capacitance	note 2	–	–	200	pF

Notes

1. All power supply pins (V_{DD} and V_{SS}) must be connected to the same external power supply unit.
2. When higher capacitive loads must be driven then a 100 Ω resistor must be connected in series with the DAC output in order to prevent oscillations in the output operational amplifier.

AC CHARACTERISTICS (ANALOG)

$V_{DDD} = V_{DDA} = V_{DDO} = 3.0$ V; $f_i = 1$ kHz; $T_{amb} = 25$ °C; $R_L = 5$ kΩ all voltages referenced to ground (pins 1, 11, 22 and 27); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-digital converter						
$V_{i(rms)}$	input voltage (RMS value)		–	1.0	–	V
ΔV_i	unbalance between channels		–	0.1	–	dB
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–80	dB
		at –60 dB; A-weighted	–	–35	–30	dB
S/N	signal-to-noise ratio	$V_i = 0$ V; A-weighted	–	95	–	dB
α_{cs}	channel separation		–	100	–	dB
PSRR	power supply rejection ratio	$f_{ripple} = 1$ kHz; $V_{ripple(p-p)} = 1\%$	–	30	–	dB
Digital-to-analog converter						
$V_{o(rms)}$	output voltage (RMS value)		–	900	–	mV
ΔV_o	unbalance between channels		–	0.1	–	dB
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–90	–85	dB
		at –60 dB; A-weighted	–	–37	–	dB
S/N	signal-to-noise ratio	code = 0; A-weighted	–	100	–	dB
α_{cs}	channel separation		–	80	–	dB
PSRR	power supply rejection ratio	$f_{ripple} = 1$ kHz; $V_{ripple(p-p)} = 1\%$	–	50	–	dB

AC CHARACTERISTICS (DIGITAL)

$V_{DDD} = V_{DDA} = V_{DDO} = 2.7$ to 3.6 V; $T_{amb} = -20$ to +85 °C; $R_L = 5$ kΩ; all voltages referenced to ground (pins 1, 11, 22 and 27); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System clock timing; see Fig.7						
T_{sys}	clock cycle	$f_{sys} = 256f_s$	78	88	262	ns
		$f_{sys} = 384f_s$	52	59	174	ns
		$f_{sys} = 512f_s$	39	44	132	ns
t_{CWL}	f_{sys} LOW level pulse width	$f_{sys} < 19.2$ MHz	$0.30T_{sys}$	–	$0.70T_{sys}$	ns
		$f_{sys} \geq 19.2$ MHz	$0.40T_{sys}$	–	$0.60T_{sys}$	ns
t_{CWH}	f_{sys} HIGH level pulse width	$f_{sys} < 19.2$ MHz	$0.30T_{sys}$	–	$0.70T_{sys}$	ns
		$f_{sys} \geq 19.2$ MHz	$0.40T_{sys}$	–	$0.60T_{sys}$	ns
Serial input/output data timing; see Fig.8						
t_{BCK}	bit clock period		$1/64f_s$	–	–	ns
$t_{BCK(H)}$	bit clock HIGH time		100	–	–	ns
$t_{BCK(L)}$	bit clock LOW time		100	–	–	ns
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{s;DATI}$	data input set-up time		20	–	–	ns
$t_{h;DATI}$	data input hold time		0	–	–	ns
$t_{d(DATO)(BCK)}$	data output delay time (from BCK falling edge)		–	–	80	ns
$t_{d(DATO)(WS)}$	data output delay time (from WS edge)	MSB-justified format	–	–	80	ns
$t_{h;DATO}$	data output hold time		0	–	–	ns
$t_{s;WS}$	word selection set-up time		20	–	–	ns
$t_{h;WS}$	word selection hold time		10	–	–	ns
Address and data transfer mode timing; see Figs 4 and 5						
T_{cy}	L3CLOCK cycle time		500	–	–	ns
t_{HC}	L3CLOCK HIGH period		250	–	–	ns
t_{LC}	L3CLOCK LOW period		250	–	–	ns
$t_{s;MA}$	L3MODE set-up time	address mode	190	–	–	ns
$t_{h;MA}$	L3MODE hold time	address mode	190	–	–	ns
$t_{s;MT}$	L3MODE set-up time	data transfer mode	190	–	–	ns
$t_{h;MT}$	L3MODE hold time	data transfer mode	190	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{s;DAT}$	L3DATA set-up time	data transfer mode and address mode	190	–	–	ns
$t_{h;DAT}$	L3DATA hold time	data transfer mode and address mode	30	–	–	ns
t_{halt}	L3MODE halt time		190	–	–	ns

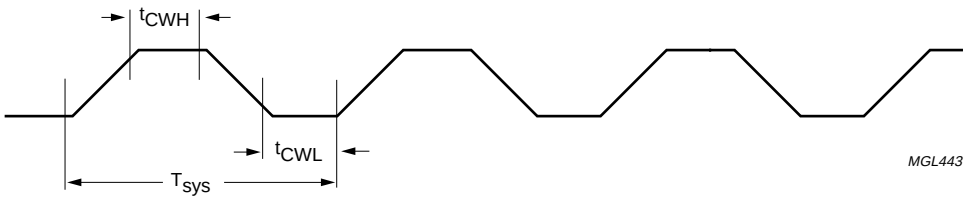


Fig.7 System clock timing.

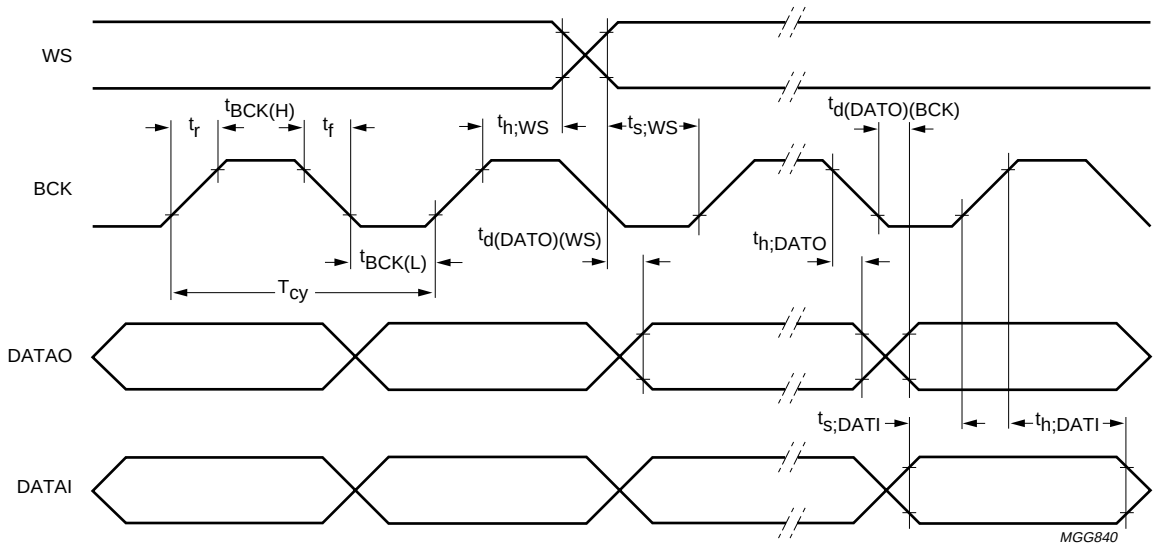


Fig.8 Serial interface timing.

APPLICATION INFORMATION

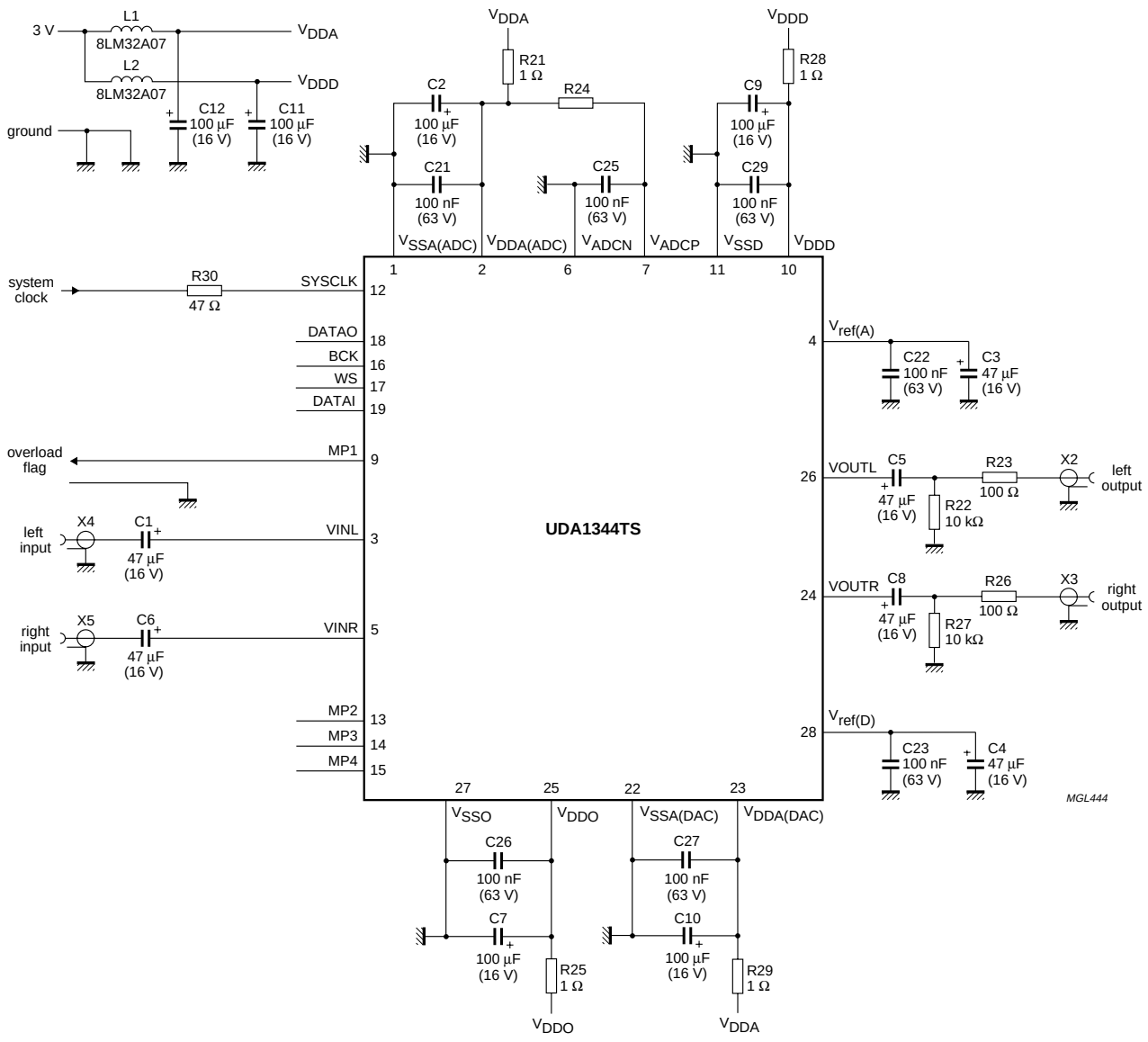
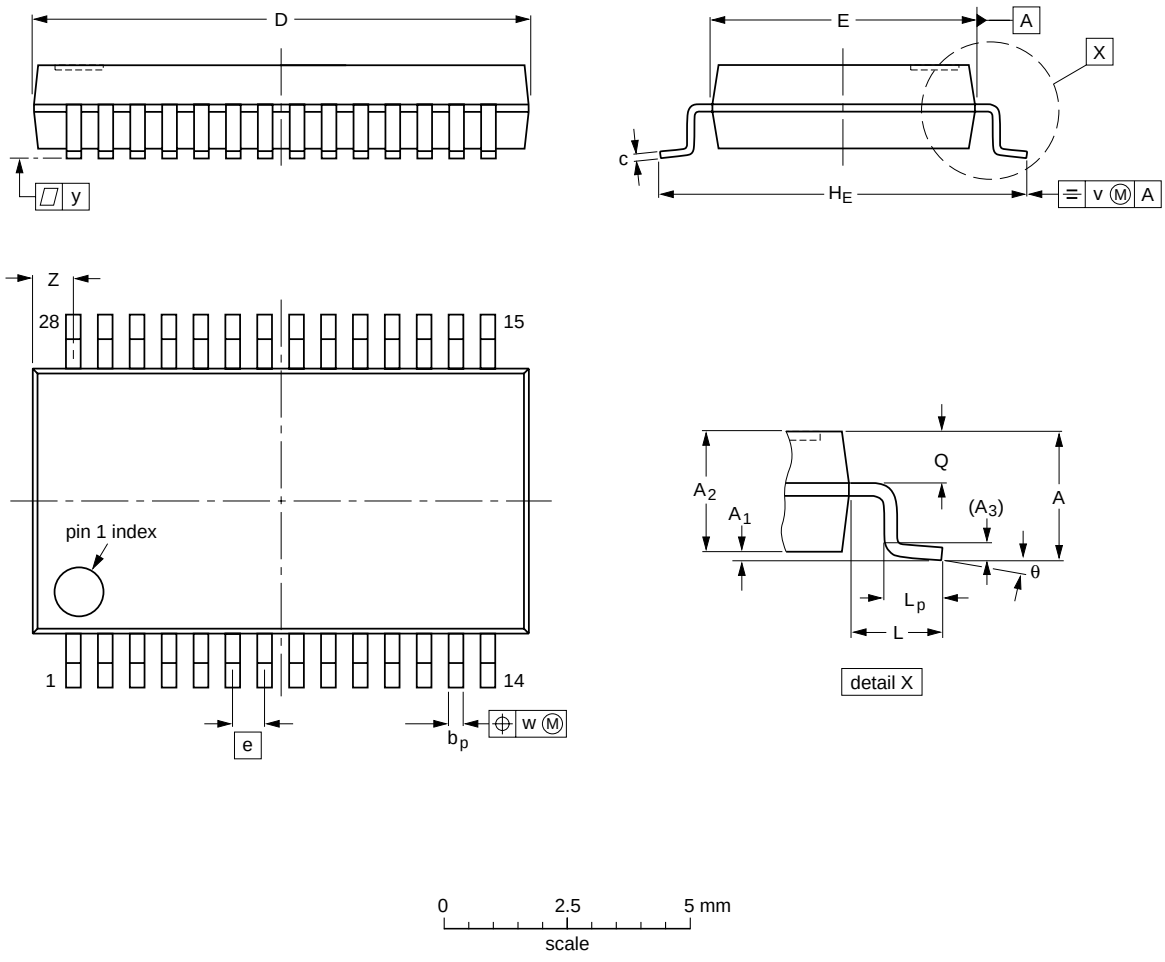


Fig.9 Application diagram.

PACKAGE OUTLINE

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				~~93-09-08~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

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Colombia: see South America

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Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
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Indonesia: PT Philips Development Corporation, Semiconductors Division,
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Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
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Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
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Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
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Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
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Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
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Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
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Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
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New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

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Philippines: Philips Semiconductors Philippines Inc.,
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Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
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Portugal: see Spain

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Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
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TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

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Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
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United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
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International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
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