UC Series

Universal Logic Circuits

Description

The UC series of ULC™s is well suited for converting medium- to large-sized CPLDs and FPGAs. Devices are implemented in high-performance CMOS technology with 0.85-mm (drawn) channel lengths, and are capable of supporting flip-flop toggle rates of 150 MHz, operating clock frequencies up to 90 MHz, and input to output delays as fast as 9 ns.

The architecture of the UC series allows for efficient support for conversions of many PLD architecture and FPGA device types up through 240 pins. The large number of available gates allows the implementation of limited amounts of RAM in FPGA architectures that support this feature, as well as JTAG boundary-scan and scan-path testing.

Conversion to the UC series of ULC can provide a significant reduction in operating power when compared to the original PLD or FPGA. This is especially true when compared to many PLD and CPLD architecture devices, which typically consume 100 mA or more even when not being clocked. The UC series has a very low standby consumption of 0.4 nA/gate typically, which would yield a standby current of 4 mA on a 10,000 gate design. Operating consumption is a strict function of clock frequency, which typically results in a power reduction of 50% to 90% depending on the device being compared.

The UC series provides several options for output buffers, including a variety of drive levels up to 24 mA (commercial temperature range only), current-controlled, and slew-rate limited. Schmitt-trigger inputs are also an option.

UC series ULCs exhibits very good immunity to latch-up, through the use of an epitaxial p-type substrate.

Features

- High-performance ULC family suitable for medium- to large-sized CPLDs and FPGAs
- Conversions to approximately 75,000 FPGA gates
- Pin counts to 240 pins
- Any pin-out matched due to limited number of dedicated pads
- High current drive capability on each I/O
  - Sink/source current up to 24 mA per buffer (commercial), 12 mA (industrial, military)
- 0.85-mm (drawn)/0.65-mm (effective) dual-layer metal CMOS technology
- Full range of packages: DIP, SOIC, LCC/PLCC, PQFP/TQFP, PGA/PPGA
- 3.3-V to 5-V operation
- Low quiescent current: 0.4 nA/gate
- Available in commercial, industrial, automotive, military and space grades

Product Outline

Part Number	Pads	Equivalent FPGA Gates	Maximum Drive
UC04	32	1000	N/A
UC08	44	2100	N/A
UC2	68	5000	N/A
UC5	88	10000	500
UC8	128	14000	850
UC10	128	18000	1100
UC12	160	20000	1300
UC22	148	30000	1850
UC29	200	40000	2500
UC35	184	48000	4300
UC50	220	60000	5700
UC66	292	75000	7500

Architecture

The basic element of the UC family is called a cell. One cell can typically implement from two to three FPGA gates. Cells are arranged in rows, with horizontal routing resources provided between the rows. Vertical routing is provided with metal two. I/O cells are provided at each pad, and may be configured as inputs, outputs, I/Os, V_{DD} or V_{SS} as required[a] to match any FPGA or PLD pin-out.

a) Except for one pin in each corner (four each on UC66) dedicated as only V_{DD} or V_{SS}, which typically are unused.

The “Max Bits RAM” column listed in the Product Outline table details the maximum amount of Xilinx XC4000 style RAM (16 X 1 blocks etc.) that could be implemented in each matrix if all of the cells were used for RAM. In an actual circuit, some of the cells would be required to implement logic, so the actual amount of RAM would need to be reduced to accommodate the logic.

In order to improve noise immunity within the device, separate V_{DD} and V_{SS} busses are provided for the internal cells and the I/O cells.

I/O Options

Inputs

Each input can be programmed as TTL, CMOS, or Schmitt Trigger, with or without a pull-up or pull-down resistor.

Fast Output Buffer

Fast output buffers are able to source or sink 3 mA to 12 mA or 24 mA in commercial temperature according to the chosen option.

Current Controlled Output Buffer

These buffers have been designed to smooth high current spikes during output transitions, especially when high-speed operation is required, while maintaining a good switching performance.

At the beginning of an output transition, one third of the total output power is applied to the load, until the output voltage reaches $V_{DD/2}$. Then, the full output stage is activated to speed up the second half of the switching phase.

The auto-adaptive technique provides a very good compromise between noise and switching performance.

Slew Rate Controlled Output Buffer

In this mode, the p- and n-output transistor commands are delayed, so that they are never “ON” together, resulting in a low switching current and low noise. These buffer are dedicated to very high load drive.

3.3-V Compatibility

Several factors are influencing the growing trend toward 3.3-V circuit operation. Among these are the desire to increase battery operating life, while at the same time decreasing battery weight, improving performance and adding features to notebook and sub-notebook personal computers. Another is the heat dissipation in ever denser and faster VLSI semiconductors, such as the latest generation of high-performance microprocessors. The UC series of ULCs is fully capable of supporting operation at 3.3 V or 5 V. The performance specifications of any given ULC design, however, must be explicitly specified as 3.3 V, 5 V or both.

Absolute Maximum Ratings

Supply Voltage (V_{DD}) . . . . . –0.5 V to 7.0 V
Input Voltage (V_{IN}) . . . . . –0.5 V to V_{DD} + 7.0 V
Storage Temperature . . . . . –65 to 150°C

Recommended Operating Range

V_{DD} . . . . . 5 V ±5% or 3.3 V ±5%
Operating Temperature
Commercial . . . . . 0 to 70°C
Industrial . . . . . –40 to 85°C
Military . . . . . –55 to 125°C

DC Characteristics

Parameter	Symbol	Test Conditions T_A = Commercial	Min	Typ	Max	Unit
Output Voltage	V_{OH}	V_{DD} = 5 V, I_{OH} (See Note a)	2.4			V
			3.84			
		V_{DD} = 3.3 V, I_{OH} (See Note a)	2.4			
	V_{OL}	I_{OL} = –24, 12, 6, 3 depending on buffer			0.4	
Input Voltage	V_{IH}		2.2			
	V_{IL}				0.8	
Input Leakage Current	I_{IX}	V_{IN} = V_{SS}	–5	–1		
		V_{IN} = V_{DD}		1	5	mA
		With pull-up, V_{IN} = V_{SS}	–100	–40		
		With pull-down, V_{IN} = V_{DD}		40	100	
Output Leakage Current	I_{OX}	V_{OUT} = V_{SS} or V_{DD}	–5		5	
Output Short Circuit Current	I_{OS}	V_{OUT} = V_{SS} or V_{DD}			110	mA
		V_{OUT} = V_{SS}	–90			
Standby Current	I_{CSB}			0.4	1	nA/ Gate
Operating Current	I_{DDOP}			1	3	mA/ Gate/ MHz
Input Capacitance	C_{IN}	V_{DD} = 5.0 V, V_{IN} = 2.0 V		3		pF
Output Capacitance	C_{OUT}	V_{OUT} = 2.0 V		3		

Notes
a. I_{OH} =24, 12, 6, 3. Selection determined by FPGA or PLD data sheet requirements.

Internal Timing Characteristics

These timing parameters for selected macro cells are provided for information only. Only pin-to-pin timing characteristics are guaranteed for ULCs, and the actual specification is determined by the original FPGA or PLD data sheet plus any specific parameters that are agreed to separately by MHS.

Conditions: V_{DD} = 5 V, T_A = 25°C, Typical Process, Statistical Wire Length. All delays measured at V_{IN}/V_{OUT} = 2.5 V.

Macro Type		Parameter	Symbol	Min	Max (1)[a]	Max (4)[a]	Units
2-Input NAND	NAND2				0.3	0.8	
8-Input NAND	NAND8	Propagation Time	t_{PD}		1.2	1.4	ns
Inverter	INV1				0.02	0.7	

Internal Timing Characteristics (Cont'd)

Macro Type		Parameter	Symbol	Min	Max (1)[a]	Max (4)[a]	Units
Inverting Tri-State Buffer	TRISTAN	Propagation Time	t_{PD}		0.5	1.2	ns
		Enable Time	t_{EN}		0.8	1.5	
Resetable Latch	LATCHNR1	Setup Time	t_{SU}	1.2			
		Hold Time	t_H	0.8			
		Pulse Width	t_{PW}	1.4			
		Propagation Time	t_{DQ}		0.8	1.3	
		Enable Time	t_{EN}		1.3	1.8	
		Reset Time	t_{RN}		0.6	1.1	
D Flip-Flop with Reset	DFFNR	Setup Time	t_{SU}	0.5			
		Hold Time	t_H	0.7			
		Pulse Width	t_{PW}	0.8			
		Clock Delay Time	t_{CQ}		1.3	1.8	
		Reset Time	t_{RN}		1.0	1.3	
TTL Compatible Input Buffer	BUFINTTL	Propagation Time	t_{PLH}		0.9	1.4	
			t_{PHL}		1.2	1.3	
TTL Compatible I/O Buffer Input Mode	BUFIOTTL		t_{PLH}		0.9	1.4	
			t_{PHL}		1.2	1.3	
Output Buffer	BUFOUT		t_{PLH}		2.2	4.2	
			t_{PHL}		2.4	3.8	
TTL Compatible I/O Buffer	BUFIOTTL		t_{PLH}		2.6	4.6	
			t_{PHL}		2.6	4.0	
Tri-State Output Buffer	BUF3STA		t_{PLH}		2.6	4.6	
			t_{PHL}		2.6	4.0	
		Enable Time	t_{PZH}		2.6	4.6	
			t_{PZL}		2.6	4.0	

Notes
a. Fan-outs for internal connection are: Max (1) = 1 internal load, Max (4) = 4 internal loads. Fanouts for output buffers are: Max (1) = 25 pF, Max (4) = 100 pF. Max values are provided for worst case of THL or TLH for internal cells.

Derating Factors: $t_P = K_P \times K_t \times K_V \times t_{NOMINAL}$

Process											
Process		Best			Nominal			Worst			
K_P		0.70			1.00			1.40			
Ambient Temperature °C											
T_A	–55	–40		0	25		70	85		125	
K_T	0.64	0.71		0.88	1.00		1.20	1.26		1.44	
Supply Voltage											
V_{DD}	3	3.13	3.3	3.47	3.63	4	4.5	4.75	5	5.25	5.5
K_V	1.74	1.66	1.56	1.48	1.40	1.27	1.13	1.06	1	0.96	0.93

External Timing Characteristics

(Over the Operating Range)

These timing parameters are provided for information only. Actual pin-to-pin timing characteristics guaranteed for ULCs are determined by the original FPGA or PLD data sheet plus any specific parameters that are agreed to separately by MHS.

Parameter	Symbol	Test Conditions	SSO	Min	Max		Unit
					Typ	Max	
Propagation Time	t_{PD}	UC04, UC08			9.0	14.0	ns
		UC2			11.0	18.0	
		UC5			11.0	18.0	
		UC8, UC10			12.0	19.0	
		UC12, UC22			12.0	19.0	
		UC29, UC35			13.0	21.0	
		UC50, UC66			15.0	24.0	
Clock Delay Time	t_{CO}	UC04, UC08	32		11.0	18.0	
		UC2	52		13.0	21.0	
		UC5	64		13.0	21.0	
		UC8, UC10	100		15.0	24.0	
		UC12, UC22	124		15.0	24.0	
		UC29, UC35	164		27.0	27.0	
		UC50, UC66	200		20.0	32.0	
Hold Time	t_H			0.8			
Output Enable Time	t_{EN}	UC04, UC08	32		9.0	14.0	
		UC2	52		11.0	18.0	
		UC5	64		11.0	18.0	
		UC8, UC10	100		13.0	21.0	
		UC12, UC22	124		13.0	21.0	
		UC29, UC35	164		15.0	24.0	
		UC50, UC66	200		18.0	29.0	

Power Consumption

Static Power Consumption for UC Series ULCs

There are three main factors to consider:

1. Leakage in the core:

   $P_{LC} = V_{DD} * I_{CCSB} *$ number of used gates

2. Leakage in inputs and tri-stated outputs:

   $P_{LIO} = V_{DD} * (I_{IX} * N + I_{OZ} * M)$

   where: N = number of inputs

   M = number of tri-stated outputs

   Care must be taken to include the appropriate figure for pins with pull-ups or pull-downs. In practice, the static consumption calculation is typically done to determine the standby current of a device; in this case only those pins sourcing current should be included, i.e. where V_{IN} or $V_{OUT} = V_{DD}$.

3. Dc power dissipation in driving I/O buffers due to resistive loads:

   In practice, the static consumption calculation is typically done to determine the standby current of a device, and under circumstances where all of the outputs are tri-stated or in input mode. So this term is zero.

   Global formula for static consumption:

   $P_{SB} = P_{LC} + P_{LIO}$

Dynamic Power Consumption for UC Series ULCs

There are four main factors to consider:

1. Static power dissipation is negligible compared to dynamic and can be ignored.

2. Dc power dissipation in I/O buffers due to resistive loads:

   P_1 (mW) = $V_{OL} * \Sigma_n (D_{Ln} * I_{OLn}) + (V_{DD} - V_{OH}) * \Sigma_n (D_{Hn} * I_{OHn})$

   where: Σ_n is a summation over all of the outputs and I/Os.

   I_{OLn} and I_{OHn} are the appropriate values for driver n

   D_{Ln} = percentage of time n is being driven to V_{OL}

   D_{Hn} = percentage of time n is being driven to V_{OH}

   It is difficult to obtain an exact value for this factor, since it is determined primarily by external system parameters. However, in practice this can be simplified to one of two cases where the device is either driving CMOS loads or driving TTL loads. CMOS loads can be approximated as purely capacitive loads, allowing this term to be treated as zero. TTL loads source significant current in the low state, but not the high state, allowing the second summation to be ignored. If a 50% duty cycle is assumed for dynamic outputs driving TTL loads, this can be approximated as:

   P_1 (mW) = $V_{OL} * (\Sigma_n * I_{OLn}/2 + \Sigma_m * I_{OLm})$ (TTL loads)

   where n are dynamic outputs and m are static low outputs.

3. Dynamic power dissipation for the internal gates:

   P_2 (mW) = $V_{DD} * I_{DDOP} * \Sigma_g (N_f * f_g)/1000$

   where: N_f = number of gates toggling at frequency f_g

   f_g = clock frequency of internal logic in MHz

   Note: If the actual toggle rates are not known, a rule of thumb is to assume that the average used gate is toggling at one half of the input clock frequency.

4. Dynamic power dissipation in the outputs:

   P_3 (mW) = $V_{DD}^2 * \Sigma_n f_n * (C_{OUT} + C_n)/1000$

   where: f_n = clocking frequency in MHz of output n

   C_n = output load capacitance in pF of output n

   C_{OUT} = output capacitance from DC Characteristics

   Global formula for dynamic consumption:

   $P = P_1 + P_2 + P_3$

Example:

Static calculation

A 100-pin ULC with 3000 used gates, 10 inputs, 20 I/Os in input mode, 40 outputs all tri-stated. No pull-ups or pull-downs. Half of the pins are at V_{DD}, half at V_{SS}. Input clock is not toggling. For this example only the current calculation is desired, so the V_{DD} term in the equations is dropped.

$P_{LC} = 1 * 3000 = 3$ mA

$P_{LIO} = ((10 + 20) * 5 + 40 * 5)/2 = 105$ mA

$P_{SB} = 3 + 105 = 108$ mA

Dynamic Calculation

We take a 16-bit resettable ripple counter which is approximately 100 gates, operating at a clock frequency of 33 MHz, which gives an average clock frequency of 33 MHz/16 for each bit and each output. There are no static outputs on this device. Operation is at 5 V, and 6-mA outputs are used and loaded at 25 pF. The output buffers are driving CMOS loads.

$P_1 = 0$

$P_2 = 5 * 3 * 100 * 33/16/1000 = 3$ mW

$P_3 = 5^2 * 16 * 33/16 * (25 + 2)/1000 = 22$ mW

$P = 0 + 5 + 22 = 27$ mW

Typical ULC Test Conditions

For ac specification purposes, an improved output loading scheme has been defined for MHS high-drive (24 mA), high-speed ULC devices. The schematic below (Figure 1) describes the typical conditions for testing these ULC devices, using the standard loading scheme commonly available on high-end ATE.

Compared to a no-load condition, this provides the following advantages:

- Output load is more representative of “real life” conditions during transitions.
- Transient energy is absorbed at the end of the line to prevent reflections which would lead to inaccurate ATE measurements.

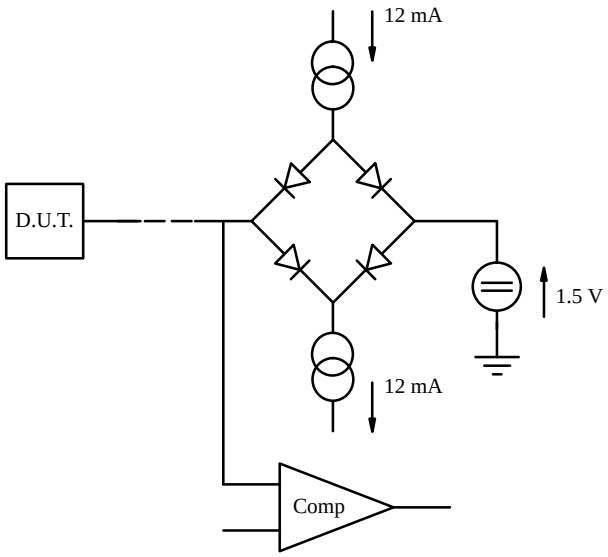

Figure 1. Typical ULC Test Conditions

ULC™ Ordering Information

Prior to conversion, ULCs are referred to by a generic ULC part number and separate package designation plus an optional temperature range formed as follows:

ULC/ *base PLD or FPGA* *pins-package*

where *base PLD or FPGA* refers to 22 V, 10 or EPM7128 or XC3030

Example:
ULC part number for XC3030A-5PL84C would be: ULC/XC3030, 84-PLCC

After conversion, a specific ULC code is ordered as follows:

UC 12 – PQS 160 – MZZ

ULC Series

- **UC** — 0.85-mm, 2-metal CMOS
- **UD** — 0.8-mm, 1-metal CMOS
- **UG** — 0.8-mm, 2- or 3-metal CMOS

Base Matrix

- **UC** — 04, 08, 2, 5, 8, 10, 12, 22, 29, 35, 50, 66
- **UD** — 02, 03, 09, 10, 14, 16, 27
- **UG** — 00, 01, 02, 04, 09, 14, 20, 33, 42, 52, 70, 90, 120, 140, 200

Package

- **PD** — Plastic Dual-In-Line Package (PDIP)
- **SD** — Plastic Skinny Dual-In-Line Package (SDIP)
- **TQ** — Plastic Thin Quad Flatpack—1.4 mm (TQFP)
- **VQ** — Plastic Very-Thin Quad Flatpack—1.0 mm (VQFP)
- **BQ** — Plastic Bumpered Quad Flatpack (BQFP)
- **PL** — Plastic J-Lead Chip Carrier (PLCC)
- **PQS** — Plastic Quad Flatpack with Short Leads (PQFP)
- **PQL** — Plastic Quad Flatpack with Long Leads (PQFP)
- **PP** — Plastic Pin-Grid Array (PPGA)
- **RS** — Plastic Small Outline Package 300-mil (SOIC)
- **SS** — Plastic Small Outline Package 150-mil (SOIC)
- **CD** — Ceramic Dual-In-Line (CDIP)
- **CL** — Ceramic Leadless Chip Carrier (CLCC)
- **CQ** — Ceramic Quad Flatpack (CQFP)
- **CP** — Ceramic Pin-Grid Array (CPGA)
- **CJ** — Ceramic J-Lead Chip Carrier (CLCCJ)

Pin Count
Number of Pins

Pattern
Unique Customer Pattern Code