DATA SHEET

TDA8006
Multiprotocol IC Card coupler

Product specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

Multiprotocol IC Card coupler TDA8006

FEATURES

- 80C52 core with 16-kbyte ROM and 256-byte RAM
- Extra 1-kbyte RAM outside the core for data storage
- Control and communication through a standard RS232 full duplex interface or a parallel interface
- Specific ISO 7816 UART with parallel access on I/O for automatic convention processing, variable baud rate through frequency or division ratio programming, error management at character level for T = 0, extra guard time register
- V_{CC} generation (5 V ±5% or 3 V ±5%, 65 mA maximum with controlled rise and fall times)
- Cards clock generation (up to 10 MHz) with two times synchronous frequency doubling
- Cards clock STOP HIGH, clock STOP LOW or 1.25 MHz (from internal oscillator) for cards power-down mode
- CLKOUT output for clocking external devices with f_{xtal}, $\frac{1}{2}f_{xtal}$ or $\frac{1}{4}f_{xtal}$ possibility
- Automatic activation and deactivation sequence through an independent sequencer
- Supports the asynchronous protocols T = 0 and T = 1 in accordance with ISO 7816 and Europay, Mastercard, Visa (EMV)
- Supports synchronous cards
- Current limitations in case of short-circuit
- Special circuitry for killing spikes during power-on or off
- Supply supervisor for power-on/off reset
- Step-up converter (supply voltage from 4.2 to 6 V)
- Power-down and sleep mode for low power consumption
- Enhanced ESD protections on card side (6 kV minimum)
- Software library for easy integration within the application.

APPLICATIONS

- Smart card readers for multiprotocol applications (EMV banking, digital pay TV, access control, etc.).

GENERAL DESCRIPTION

The TDA8006 is controlled through a standard serial interface or a parallel bus, it takes care of all ISO 7816, EMV and GSM11.11 requirements. It gives the card and the set a very high level of security, due to its special hardware against ESD, short-circuiting, power failure, etc. Its integrated step-up converter allows operation within a supply voltage range of 4.2 to 6 V.

A special version where the internal connections to the controller are fed outside through pins allows easy development and evaluation, together with a 80CL580 microcontroller or development tool (emulation board available).

A software library has been developed, taking care of all actions required for T = 0, T = 1 and synchronous protocols. This library may be either linked with the application software before masking, or masked in the internal ROM (see *"Application Note AN97080"*).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8006H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2
TDA8006AH	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

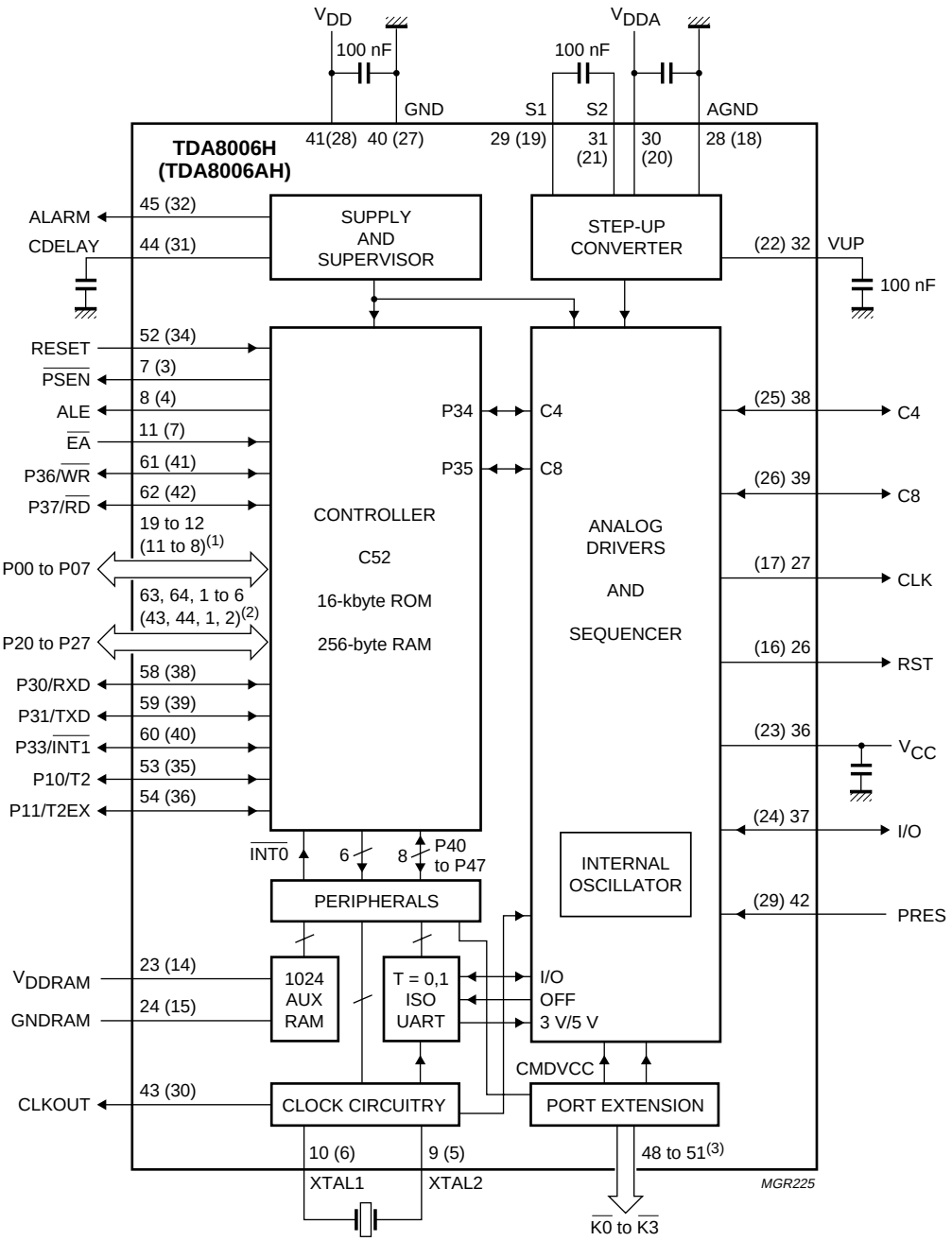
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.2	–	6	V
$I_{DD(pd)}$	supply current in power-down mode	V_{DD} = 5 V; card inactive; note 1	–	–	250	µA
$I_{DD(sm)}$	supply current in sleep mode	card powered but clock stopped; note 1	–	–	1500	µA
V_{CC}	card supply voltage	including static loads (5 V card)	4.75	5.0	5.25	V
		with 40 nAs dynamic loads on 100 nF capacitor (5 V card)	4.6	–	5.4	V
		including static loads (3 V card)	2.80	–	3.20	V
		with 24 nAs dynamic loads on 100 nF capacitor (3 V card)	2.75	–	3.25	V
I_{CC}	card supply current	operating	–	–	65	mA
		overload detection	–	80	–	mA
SR	slew rate (rise and fall)	maximum load capacitor pin V_{CC} 400 nF (including typical 100 nF decoupling)	0.10	0.16	0.22	V/µs
t_{de}	deactivation cycle duration		–	–	100	µs
t_{act}	activation cycle duration		–	–	225	µs
f_{xtal}	crystal frequency		4	–	25	MHz
f_{oper}	operating frequency	external frequency applied on pin XTAL1	0	–	25	MHz
T_{amb}	operating ambient temperature		–25	–	+85	°C

Note

1. I_{DD} in all configurations include the current at pins V_{DD}, V_{DDA} and V_{DDRAM}.

BLOCK DIAGRAM



Minimum value for capacitor between V_{DDA} and AGND is 2.2 µF.

Pin numbers in parenthesis represent the TDA8006AH.

(1) Ports P04 to P07 not applicable for QFP44 package.

(2) Ports P24 to P27 not applicable for QFP44 package.

(3) Ports $\overline{K0}$ to $\overline{K3}$ not applicable for QFP44 package.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	QFP64	QFP44	
P22	1	1	address 10/general purpose I/O port
P23	2	2	address 11/general purpose I/O port
P24	3	–	address 12/general purpose I/O port
P25	4	–	address 13/general purpose I/O port
P26	5	–	address 14/general purpose I/O port
P27	6	–	address 15/general purpose I/O port
$\overline{PSEN}$	7	3	program store enable output
ALE	8	4	address latch enable
XTAL2	9	5	crystal connection
XTAL1	10	6	crystal connection or external clock input
$\overline{EA}$	11	7	external access
P07	12	–	address/data 7/general purpose I/O port
P06	13	–	address/data 6/general purpose I/O port
P05	14	–	address/data 5/general purpose I/O port
P04	15	–	address/data 4/general purpose I/O port
P03	16	8	address/data 3/general purpose I/O port
P02	17	9	address/data 2/general purpose I/O port
P01	18	10	address/data 1/general purpose I/O port
P00	19	11	address/data 0/general purpose I/O port
n.c.	20	12	not connected
n.c.	21	13	not connected
n.c.	22	–	not connected
V_{DDRAM}	23	14	supply voltage for the auxiliary RAM
GNDRAM	24	15	ground for the auxiliary RAM
n.c.	25	–	not connected
RST	26	16	card reset output (ISO C2 contact)
CLK	27	17	clock output to the card (ISO C3 contact)
AGND	28	18	ground for the analog part
S1	29	19	contact 1 for the step-up converter (a ceramic capacitor of 100 nF must be connected between S1 and S2)
V_{DDA}	30	20	analog supply voltage for the voltage doubler
S2	31	21	contact 2 for the step-up converter (a ceramic capacitor of 100 nF must be connected between S1 and S2)
VUP	32	22	output of the step-up converter; must be decoupled with a 100 nF ceramic capacitor
n.c.	33	–	not connected
n.c.	34	–	not connected
n.c.	35	–	not connected
V_{CC}	36	23	card supply output voltage (ISO C1 contact)

SYMBOL	PIN		DESCRIPTION
	QFP64	QFP44	
I/O	37	24	data line to/from the card (ISO C7 contact)
C4	38	25	auxiliary I/O for ISO C4 contact (synchronous cards for instance)
C8	39	26	auxiliary I/O for ISO C8 contact (synchronous cards for instance)
GND	40	27	ground
V_{DD}	41	28	supply voltage
PRES	42	29	card presence contact input (active HIGH or LOW by mask option); see Table 12
CLKOUT	43	30	output for clocking external devices
CDELAY	44	31	external capacitor connection for delayed reset signal
ALARM	45	32	open drain reset output (active HIGH or LOW by mask option); see Table 12
TEST	46	33	test pin (must be left open-circuit in the application)
INHIB	47	–	test pin (must be left open-circuit in the application)
$\overline{K0}$	48	–	output port from port extension (±2 mA push-pull)
$\overline{K1}$	49	–	output port from port extension (±2 mA push-pull)
$\overline{K2}$	50	–	output port from port extension (±2 mA push-pull)
$\overline{K3}$	51	–	output port from port extension (±2 mA push-pull)
RESET	52	34	input for resetting the microcontroller (active HIGH)
P10/T2	53	35	general purpose I/O port (connected to P10)
P11/T2EX	54	36	general purpose I/O port (connected to P11)
n.c.	55	37	not connected
n.c.	56	–	not connected
n.c.	57	–	not connected
P30/RXD	58	38	general purpose I/O port or serial interface receive line
P31/TXD	59	39	general purpose I/O port or serial interface transmit line
P33/$\overline{INT1}$	60	40	general purpose I/O port or interrupt (connected to P33)
P36/$\overline{WR}$	61	41	general purpose I/O port or external data memory write strobe
P37/$\overline{RD}$	62	42	general purpose I/O port or external data memory read strobe
P20	63	43	address 8/general purpose I/O port
P21	64	44	address 9/general purpose I/O port

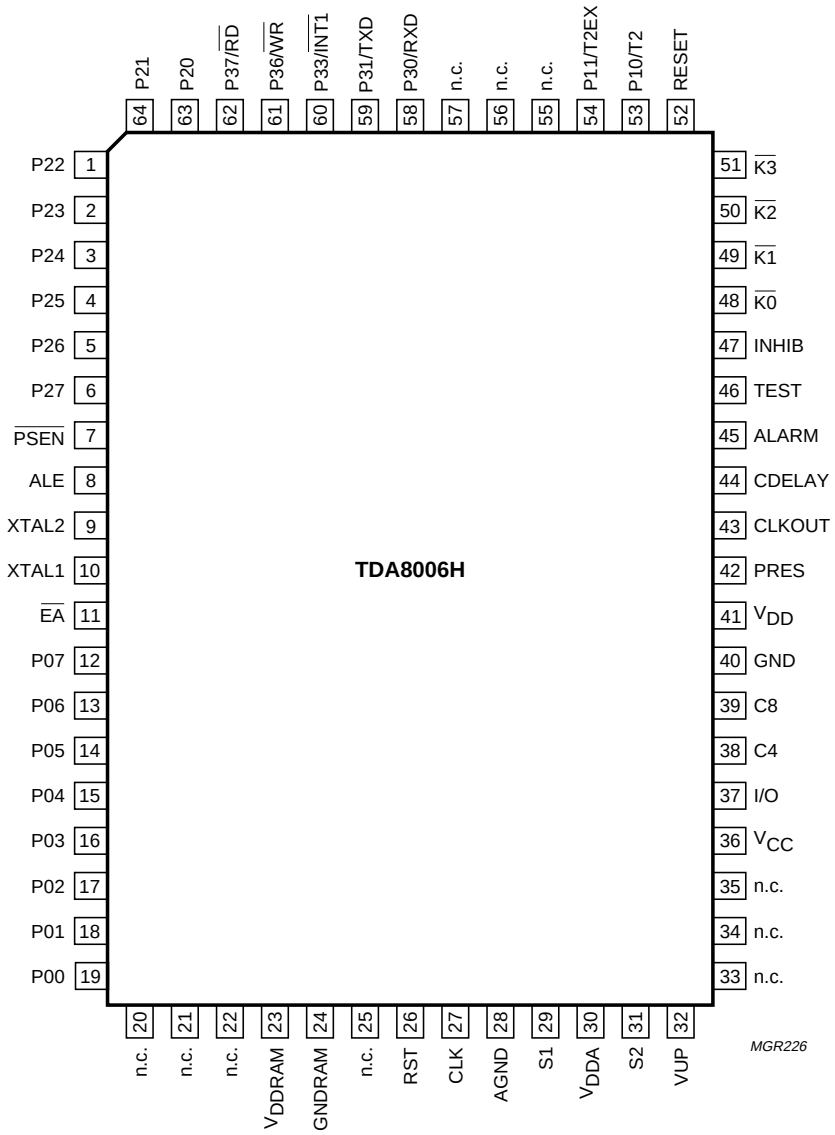


Fig.2 Pin configuration (QFP64).

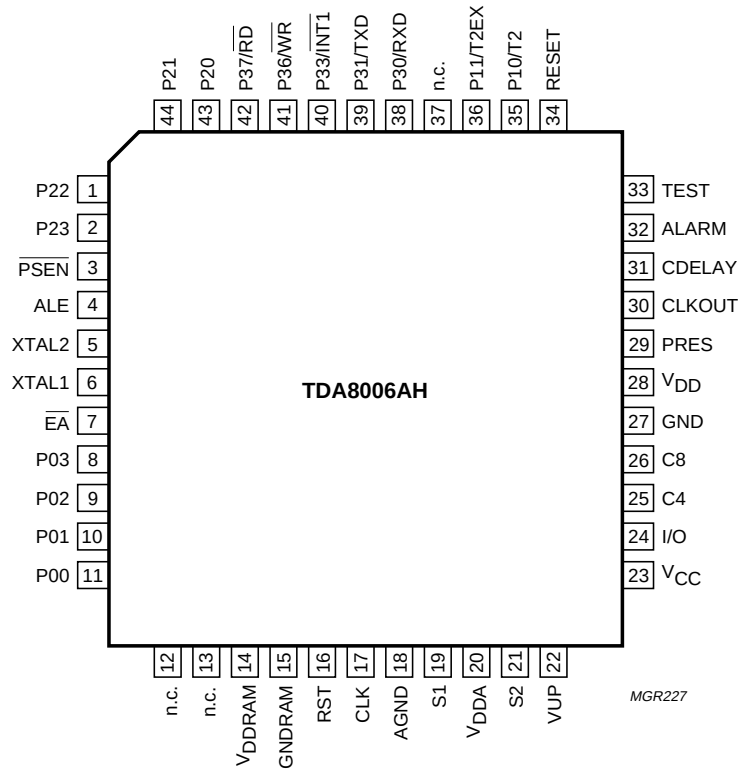


Fig.3 Pin configuration (QFP44).

FUNCTIONAL DESCRIPTION

It is assumed that the reader of this data sheet is familiar with ISO 7816.

Microcontroller

The microcontroller is an 80C52 with 16 kbytes of ROM, 256 bytes of RAM, timers 0, 1, 2 and 5 I/O ports (port P0: open-drain; ports P1 to P3: weak pull-up). Port P4 is as in 83CE560, except that precharge circuitries ensure fast rising time also when leaving read mode (transition times <0.5 μs). The ROM code content may be tested by signature, thus avoiding read-out of the ROM code after masking (for security bit option see Table 12). The CPU, timers 0 and 1, serial UART, parallel I/O ports, 256-byte RAM, 16-kbyte ROM and external bus are conventional C51 family library elements. Timer 2 is a conventional C52 element (interrupt enable bit ET2: bit 3 in register IEN1 at byte address E8H and interrupt priority bit PT2: bit 3 in register IP1 at byte address F8H). Register PCON contains an added feature: PCON.5 = RFI (reduced radio frequency interference bit). When set to logic 1, the toggling of pin ALE is prohibited. This pin is cleared on RESET.

If an access to the external data memory via MOVX instructions (see Table 1) is desired, bit PCON.6 = ARD inside the PCON register must be set to logic 1.

Please refer for any further information to the published specification of the 83CE560 in *"Data Handbook IC20; 80C51-Based 8-Bit Microcontrollers"*.

Ports P40 to P47, $\overline{INT0}$, P12, P13, P14, P15, P16 and P17 are used internally for controlling the smart card interface and the other peripherals. P34 and P35 are used to control the auxiliary contacts C4 and C8.

The list of differences given in Table 1 may help to develop the software on the dedicated emulation board for TDA8006 or other device.

Table 1 List of differences between TDA8006, CE560, CL580 and C52

FEATURES	TDA8006	83CE560	CL580	INTEL C52
P4 address	C0	C0	C1	no
Timer 2	Intel	Philips	Intel	Intel
ROM size	16 kbytes	64 kbytes	6 kbytes	8 kbytes
External 0 interrupt vector	0003H	0003H	0003H	0003H
External 0 interrupt priority	highest (1st)	highest (1st)	highest (1st)	highest (1st)
Timer 0 interrupt vector	000BH	000BH	000BH	000BH
Timer 0 interrupt priority	2nd	2nd	4th	2nd
External 1 interrupt vector	0013H	0013H	0013H	0013H
External 1 interrupt priority	3th	3th	7th	3th
Timer 1 interrupt vector	001BH	001BH	001BH	001BH
Timer 1 interrupt priority	4th	4th	10th	4th
Serial 0 interrupt vector	0023H	0023H	0023H	0023H
Serial 0 interrupt priority	5th	5th	13th	5th
Timer 2 interrupt vector	004BH	0033H, etc. (8)	0033H	002BH
Timer 2 interrupt priority	lowest (6th)	miscellaneous	5th	lowest (6th)
I^2C	no	yes	yes	no
ADC	no	yes	yes	no
32 kHz oscillator	no	yes	no	no
PWM	no	yes	yes	no
Watchdog	no	yes	yes	no

FEATURES	TDA8006	83CE560	CL580	INTEL C52
Interrupts on P1	no	no	yes	no
Additional RAM	1-kbyte peripheral	2-kbyte MOVX	no	no
Wake-up from PDOWN	reset, $\overline{INT0}$, $\overline{INT1}$	reset, $\overline{INT0}$, $\overline{INT1}$ + other	reset, $\overline{INT2}$ to $\overline{INT8}$	reset

Table 2 Bit addresses (special function registers)

REGISTER	BYTE ADDRESS	BIT ADDRESS								RESET VALUE
		(MSB)							(LSB)	
IP1		–	–	–	–	PT2	–	–	–	XXXX 0XXX
	F8H	FFH	FEH	FDH	FCH	FBH	FAH	F9H	F8H	
B										0000 0000
	F0H	F7H	F6H	F5H	F4H	F3H	F2H	F1H	F0H	
IEN1		–	–	–	–	ET2	–	–	–	0000 0000
	E8H	EFH	EEH	EDH	ECH	EBH	EAH	E9H	E8H	
ACC										0000 0000
	E0H	E7H	E6H	E5H	E4H	E3H	E2H	E1H	E0H	
PSW		CY	AC	F0	RS1	RS0	OV	F1	P	0000 0000
	D0H	D7H	D6H	D5H	D4H	D3H	D2H	D1H	D0H	
T2CON		TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2N	CP/RL2N	0000 0000
	C8H	CFH	CEH	CDH	CCH	CBH	CAH	C9H	C8H	
P4										1111 1111
	C0H	C7H	C6H	C5H	C4H	C3H	C2H	C1H	C0H	
IP0		–	–	–	PS0	PT1	PX1	PT0	PX0	XXX0 0000
	B8H	BFH	BEH	BDH	BCH	BBH	BAH	B9H	B8H	
P3										1111 1111
	B0H	B7H	B6H	B5H	B4H	B3H	B2H	B1H	B0H	
IEN0		EA	–	–	ES0	ET1	EX1	ET0	EX0	0XX0 0000
	A8H	AFH	AEH	ADH	ACH	ABH	AAH	A9H	A8H	
P2										1111 1111
	A0H	A7H	A6H	A5H	A4H	A3H	A2H	A1H	A0H	
S0CON		SMO	SM1	SM2	REN	TB8	RB8	TI	RI	0000 0000
	98H	9FH	9EH	9DH	9CH	9BH	9AH	99H	98H	
P1										1111 1111
	90H	97H	96H	95H	94H	93H	92H	91H	90H	
TCON		TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	0000 0000
	88H	8FH	8EH	8DH	8CH	8BH	8AH	89H	88H	
P0										1111 1111
	80H	87H	86H	85H	84H	83H	82H	81H	80H	

Table 3 Bit addresses (other registers)

REGISTER	BYTE ADDRESS	RESET VALUE
SP	81H	0000 1111
DPL	82H	0000 0000
DPH	83H	0000 0000
PCON	87H	0000 0000
TMOD	89H	0000 0000
TL0	8AH	0000 0000
TL1	8BH	0000 0000
TH0	8CH	0000 0000
TH1	8DH	0000 0000
S0BUF	99H	XXXX XXXX
RCAP2L	CAH	0000 0000
RCAP2H	CBH	0000 0000
TL2	CCH	0000 0000
TH2	CDH	0000 0000

Supply

The circuit operates within a supply voltage range of 4.2 to 6 V. The supply pins are V_{DD}, V_{DDA}, GND, AGND, V_{DDRAM} and GNDRAM. Pins V_{DDA} and AGND supply the analog drivers to the card and have to be externally decoupled because of the large current spikes that the card and the step-up converter can create. V_{DDRAM} and GNDRAM supply the auxiliary RAM and should be decoupled separately. V_{DD} and GND supply the rest of the chip. An integrated spike killer ensures the contacts to the card remain inactive during power-up or power-down. An internal voltage reference is generated which is used within the step-up converter, the voltage supervisor and the V_{CC} generator.

The voltage supervisor generates an alarm pulse, whose length is defined by an external capacitor tied to the CDELAY pin, when V_{DD} is too low to ensure proper operation (1 ms per 1 nF typical). This pulse is used as a reset pulse by the controller, in parallel with an external reset input, which can be tied to the system controller. It is also used in order to either block any spurious on card contacts during controllers reset or to force an automatic deactivation of the contacts in the event of supply drop-out (see Sections “Activation sequence” and “Deactivation sequence”). It is also fed to an external open-drain output (called ALARM) which can be chosen active HIGH or LOW by mask option (see Table 12).

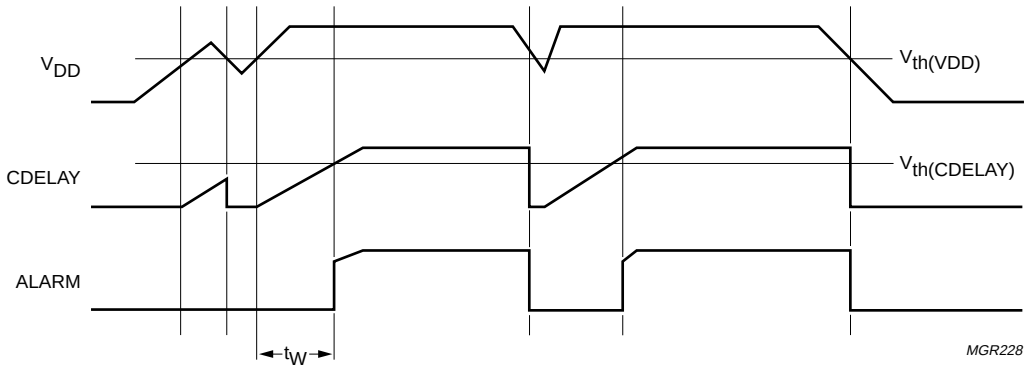


Fig.4 Voltage supervisor.

Step-up converter

Except for the V_{CC} generator and the other card contacts buffers, the whole circuit is powered by V_{DD}, V_{DDA} and V_{DDRAM}. If the supply voltage is 4.2 V, then a higher voltage is needed for the ISO contacts supply. When a card session is requested by the controller, the sequencer first starts the step-up converter, which is a switched capacitors type, clocked by an internal oscillator at a frequency of approximately 2.5 MHz. The output voltage VUP is regulated at approximately 6 V and then fed to the V_{CC} generator. V_{CC} and GND are used as a reference for all other cards contacts.

ISO 7816 security

The correct sequence during activation and deactivation of the card is ensured through a specific sequencer, clocked by a division ratio of the internal oscillator.

Activation (bit CMDVCC within the ports extension register is HIGH) is only possible if the card is present (pin PRES HIGH or LOW according to mask option) and if the supply voltage is correct (ALARM signal inactive).

The presence of the card is signalled to the controller by the OFF bit (within the status register, generating an interrupt if enabled when toggling).

During a session, the sequencer performs an automatic emergency deactivation in the event of card take-off, supply voltage drop or short-circuit. The OFF bit goes LOW, thereby warning the controller through the interrupt line $\overline{INT0}$ and the status register.

Peripheral interface (see Figs 5 and 6)

This block allows parallel communication with the four peripherals (ISO 7816 UART, clock generator, on/off sequencer and auxiliary RAM) through an 8-bit data bus, 6-bit address and control bus and one interrupt line to the controller. The data bus consists of ports P40 (data 0) to P47 (data 7). The address bus consists of ports AD0 (P12), AD1 (P13), AD2 (P14) and AD3 (P15). The control lines are R/$\overline{W}$ (P16) and $\overline{EN}$ (P17). The interrupt line is $\overline{INT0}$.

During a read operation, data is available on the bus when $\overline{EN}$ is LOW and the controller may read them at this moment. During a write operation, the data should be present on the bus before asserting $\overline{EN}$ LOW, which writes them in the registers. After resetting $\overline{EN}$ HIGH, the controller must not omit to release the bus by setting P4 HIGH again (the transition times on port P4 are less than 500 ns).

The interrupt line is reset HIGH when reading out the status register.

READ OPERATION

- Set P4 to FFH
- Select the register with AD0, AD1, AD2, AD3
- Assert R/$\overline{W}$ HIGH
- Assert $\overline{EN}$ LOW; the data is available on data bus P4
- Read the data on P4
- Set $\overline{EN}$ HIGH: the bus is set to high impedance.

WRITE OPERATION

- Select the correct register with AD0, AD1, AD2, AD3
- Assert R/$\overline{W}$ LOW
- Write the data on the data bus P4
- Assert $\overline{EN}$ LOW; the data is written in the register
- Set $\overline{EN}$ back HIGH
- Set P4 to FFH: the bus is back to high impedance.

Integrated precharges allow fast rising edges on P4 when changing from read mode to write mode, thus avoiding to trigger the active pull-ups on P4.

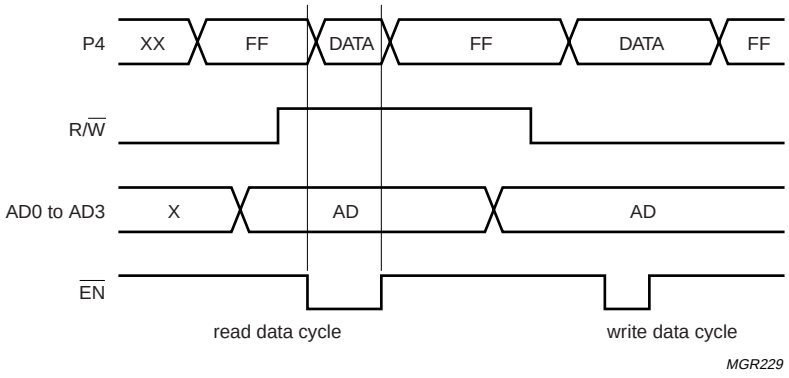


Fig.5 Use of peripheral interface.

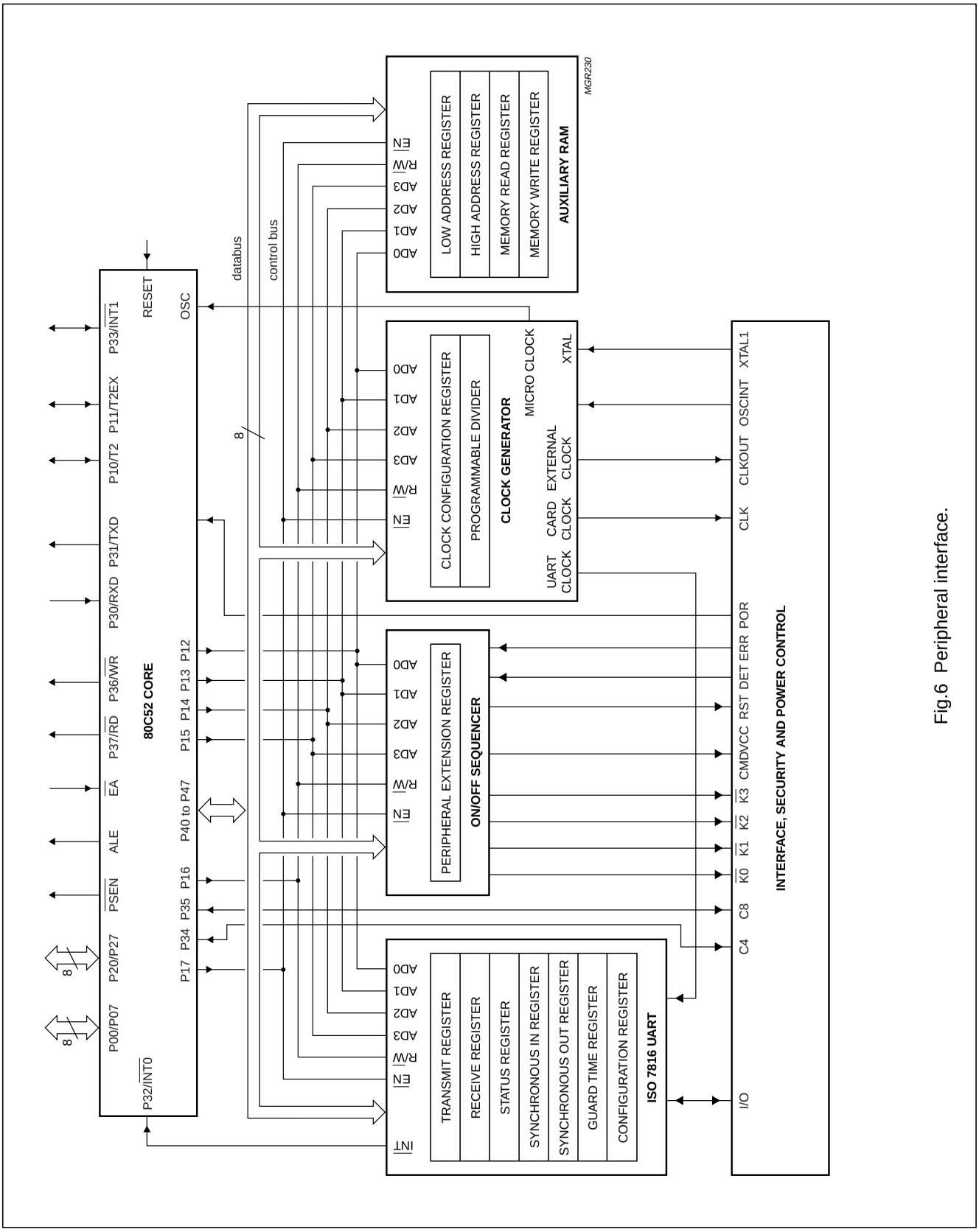


Fig.6 Peripheral interface.

Register addresses

Table 4 Register addresses

AD3	AD2	AD1	AD0	R/$\overline{W}$	REGISTER	PERIPHERAL
0	0	0	0	0	CCR (Clock Configuration Register)	clock generator
0	0	0	1	0	PDR (Program Divider Register)	
0	0	1	1	0	SOR (Synchronization Out Register)	ISO 7816 UART
0	0	1	1	1	SIR (Synchronization In Register)	
0	1	0	0	0	UTR (UART Transmit Register)	
0	1	0	0	1	URR (UART Receive Register)	
0	1	0	1	1	USR (UART Status Register)	
0	1	0	1	0	UCR (UART Configuration Register)	
0	1	1	0	0	GTR (Guard Time Register)	
0	1	1	1	0	PER (Ports Extension Register)	on/off sequencer
1	1	0	X	0	MAR0 (Memory Address LOW)	auxiliary RAM
1	1	1	X	0	MAR1 (Memory Address HIGH)	
1	0	0	X	0	MWR (Memory Write Register)	
1	0	0	X	1	MRR (Memory Read Register)	

Clock circuitry

The clock to the microcontroller (OSC), the clock to the card (CLK), the clock to the ISO 7816 UART and the clock to the external world (CLKOUT) are derived from the main clock signals (XTAL from 4 to 20 MHz, or an external clock signal applied on XTAL1), or the internal oscillator (f_{INT}).

Microcontroller clock (OSC): after power-on or reset, the microcontroller is clocked with $\frac{1}{8}f_{INT}$. Then, the application may decide to clock it with $\frac{1}{2}f_{INT}$, $\frac{1}{2}f_{xtal}$ or f_{xtal}.
All frequency changes are synchronous, thereby ensuring no hang-up due to short spikes etc.

Cards clock (CLK): the application may select to send the card $\frac{1}{2}f_{xtal}$, $\frac{1}{4}f_{xtal}$, $\frac{1}{8}f_{xtal}$ or $\frac{1}{2}f_{INT}$ (≈1.25 MHz), or to stop the clock HIGH or LOW. All transition are synchronous, ensuring correct pulse length during start or change in accordance with ISO 7816.

After power-on or reset, CLK is stopped at LOW.

External clock output (CLKOUT): CLKOUT is a permanent clock output which may be used by the external world. The following frequencies are possible: f_{xtal}, $\frac{1}{2}f_{xtal}$ and $\frac{1}{4}f_{xtal}$. All transitions are synchronous. After power-on or reset, CLKOUT is fixed at $\frac{1}{4}f_{xtal}$.

ISO 7816 UART clock: the clock to the ISO 7816 UART is the same as the clock to the card.

Two items act on this clock in order to achieve the different baud rates on I/O as defined by the F and D factors: a prescaler by 31 or 32 and an auto-reload 8-bit programmable counter.

All these configurations are controlled by the clock configuration register and the programmable divider register.

Table 5 Clock Configuration Register (CCR; address 0; write-only; all bits cleared after reset)

D7	D6	D5	D4	D3	D2	D1	D0	UART PRESC	CLK	CLKOUT	OSC
X	X	X	X	X	X	X	0	/31			
X	X	X	X	X	X	X	1	/32			
X	X	X	X	0	0	0	X		STOP LOW		
X	X	X	X	0	0	1	X		$\frac{1}{2}$XTAL		
X	X	X	X	0	1	0	X		$\frac{1}{4}$XTAL		
X	X	X	X	0	1	1	X		$\frac{1}{8}$XTAL		
X	X	X	X	1	0	0	X		$\frac{1}{2}$FINT		
X	X	X	X	1	0	1	X		STOP HIGH		
X	X	0	0	X	X	X	X			$\frac{1}{4}$XTAL	
X	X	0	1	X	X	X	X			XTAL	
X	X	1	0	X	X	X	X			$\frac{1}{2}$XTAL	
0	0	X	X	X	X	X	X				$\frac{1}{8}$FINT
0	1	X	X	X	X	X	X				XTAL
1	0	X	X	X	X	X	X				$\frac{1}{2}$XTAL
1	1	X	X	X	X	X	X				$\frac{1}{2}$FINT

Table 6 Programmable Divider Register (PDR; address 1; write-only; all bits cleared after reset)

D7	D6	D5	D4	D3	D2	D1	D0	DIVISION FACTOR
x7	x6	x5	x4	x3	x2	x1	x0	x7x6x5x4x3x2x1x0H

The hexadecimal value stored in the PDR is the auto-reload value of an 8-bit counter clocked by the cards clock; the counter is loaded with this value and counts from this value till overflow; then it is reloaded with the same value and the counter starts counting again. The output of the counter is then divided by 31 or 32 in accordance with the programmed value of the prescaler (UART PRESC). The result is ISO 7816 UART CLK, used for shifting the data in or out on the I/O line.

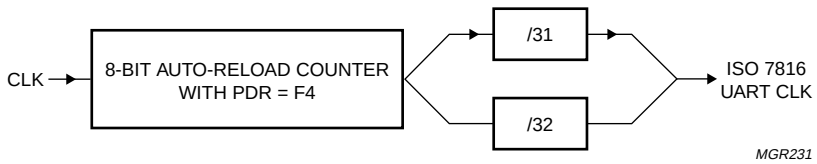


Fig.7 Baud rate selection on I/O.

The example shown in Fig.7 shows how to program a division factor of 372. With these registers, the baud rates given in Table 7 are achievable according to ISO 7816 (31 or 32 depends on the choice for the prescaler, and the hexadecimal value is the programmed value within the PDR).

Table 7 Baud rates according to F and D and prescaler and programmable divider values

D	F											
	0000	**0001**	**0010**	**0011**	**0100**	**0101**	**0110**	**1001**	**1010**	**1011**	**1100**	**1101**
0001	31;F4	31;F4	31;EE	31;E8	31;DC	31;D0	31;C4	32;F0	32;E8	32;E0	32;D0	32;C0
0010	31;FA	31;FA	31;F7	31;F4	31;EE	31;E8	31;E2	32;F8	32;F4	32;F0	32;E8	32;E0
0011	31;FD	31;FD	–	31;FA	31;F7	31;F4	31;F1	32;FC	32;FA	32;F8	32;F4	32;F0
0100	–	–	–	31;FD	–	31;FA	–	32;FE	32;FD	32;FC	32;FA	32;F8
0101	–	–	–	–	–	31;FD	–	32;FF	–	32;FE	32;FD	32;FC
0110	–	–	–	–	–	–	–	–	–	32;FF	–	32;FE
1000	31;FF	31;FF	–	31;FE	31;FD	31;FC	31;FB	–	32;FE	–	32;FC	–
1001	–	–	–	–	–	–	31;FD	–	–	–	–	–

On/off controller (PER; address 7; write-only; all bits cleared after reset)

Table 8 Bits of on/off controller

BIT	NAME	DESCRIPTION
D0	CMDVCC; set and reset by software	set to 1 for starting activation sequence of the card, and reset to 0 for starting deactivation
D1	RSTIN; set and reset by software	control line for card RST in manual mode (active HIGH)
D2	Force Inverse Parity (FIP); set and reset by software	when LOW, the UART processes the parity according to ISO 7816; when HIGH, the UART processes the inverse parity (which causes parity errors during transmission and ‘not acknowledge’ signals during reception)
D3	automatic ATR processing enabling (ATREN); set by software, reset by hardware	when HIGH, the UART counts automatically the clock pulses during ATR and controls the RST contact; this bit is automatically reset by hardware when a start bit is detected on I/O or when the card is declared as mute; when LOW, this automatic processing is disabled (manual mode)
D4	$\overline{K0}$; set and reset by software	auxiliary ±2 mA push-pull output control (inverted output)
D5	$\overline{K1}$; set and reset by software	auxiliary ±2 mA push-pull output control (inverted output)
D6	$\overline{K2}$; set and reset by software	auxiliary ±2 mA push-pull output control (inverted output)
D7	$\overline{K3}$; set and reset by software	auxiliary ±2 mA push-pull output control (inverted output)

The on/off controller is used for activating or deactivating the card, for controlling the contact C2 (RST) manually through RSTIN or automatically, for forcing inverse parity (flow control or test purpose) and for controlling four independent push-pull output lines $\overline{K0}$ to $\overline{K3}$.

After having cleared the ISO 7816 UART reset bit (see UART configuration register) and checking the card presence within the status register, the software may initiate an activation sequence by setting bit CMDVCC HIGH. It may also initiate a deactivation sequence by resetting this bit (see activation and deactivation sequences).

The timings during the ATR may be either checked manually (using RSTIN and t_3/t_5 for counting clock pulses) or automatically by setting bit ATREN HIGH (see Section “Activation sequence”). In this case, RST is controlled by hardware and the count of CLK pulses is also done by hardware. Bit ATREN is reset by hardware when a start bit has been detected before 2×45000 CLK pulses, or when the card is declared as ‘mute’. Setting this bit HIGH again during a session will initiate a warm reset.

A warm reset may also be done manually by using RSTIN and t_3/t_5 again.

ISO 7816 UART

The ISO 7816 UART handles all specific requirements defined in ISO 7816 T = 0 and T = 1 protocol types. It is also able to deal with synchronous cards (in conjunction with C4 and C8). In addition, there is a possibility to force parity errors for test purposes or flow control. The count of CLK cycles during ATR is possible by hardware or by software.

The ISO 7816 UART is configurated with 2 registers: UART Configuration Register (UCR) and Guard Time Register (GTR).

When timings are given in terms of ETU (Elementary Time Unit as defined by ISO 7816), then the reference is the negative edge of the start bit of the character being received or transmitted, unless otherwise specified.

Table 9 UART Configuration Register (UCR; address 5; write-only; all bits cleared after reset)

BIT	NAME	DESCRIPTION
D0	Reset ISO 7816 UART (RIUN); set by software, reset by software	when LOW, this bit resets the UART; must be set by software before any use of the UART
D1	Start Session (SS); set by software, reset by software	when HIGH, this bit allows the detection of the convention during the initial character of the card; must be reset by software after correct reception of the first character and before complete reception of the next character
D2	Last Character to Transmit (LCT); set by software, reset by hardware or software	when HIGH, this bit allows automatic toggling from transmission to reception mode after successful transmission of the last character; in this case, TRN is also reset by hardware
D3	Transmit/Receive-N (TRN); set by software, reset by software or hardware	when LOW, the UART is in reception mode; when HIGH, it is in transmission mode; $\overline{INT}$ falls down when TRN is set
D4	not used	
D5	Protocol Selection (PS); set by software, reset by software	when LOW, the UART is in T = 0 mode; when HIGH, the UART is in T = 1 mode
D6	3 V/5 V-N (TFN); set by software, reset by software	when LOW, the card supply voltage V_{CC} = 5 V; when HIGH, V_{CC} = 3 V
D7	Synchrone/asynchrone-N (SAN); set by software, reset by software	when HIGH, this bit allows direct monitoring of I/O by bit D0 of SIR or SOR; when LOW, I/O is fed to the ISO 7816 UART

RECEPTION

In order to start a session with the card bit RIUN (which resets the ISO 7816 UART when LOW) must be set HIGH.

The UART recognizes the convention (direct or inverse) on the characters received while bit SS (Start Session) is HIGH. Then the UART automatically converts any transmitted or received character according to this convention, so the software only has to deal with characters written in direct convention. Indeed, bit SS must be reset by software after correct reception of the first character of the ATR (TS) and before complete reception of the next character.

Reception mode is selected when TRN is LOW. The bit FSD is set within USR, and an interrupt is generated if enabled at the start bit of the received character when SS is HIGH, allowing the manual CLK count during ATR.

The interrupt will be cleared on the rising edge of $\overline{EN}$ during the status read operation.

For the next characters, bit RBF is set at 10.5 ETU and an interrupt is generated if enabled for telling that a character has been received, with or without parity error, and that this character may be read within the reception register. The interrupt is cleared on the falling edge of $\overline{EN}$ during the read operation of the received character.

In protocol type T = 0 (bit PS LOW), the I/O line is automatically pulled LOW between 10.5 and 11.75 ETU if a parity error has been detected in the character (parity error handling at character level).

In protocol type T = 1 (bit PS HIGH), if a parity error is detected, bit PE is set in the status register, but the I/O line is not pulled LOW.

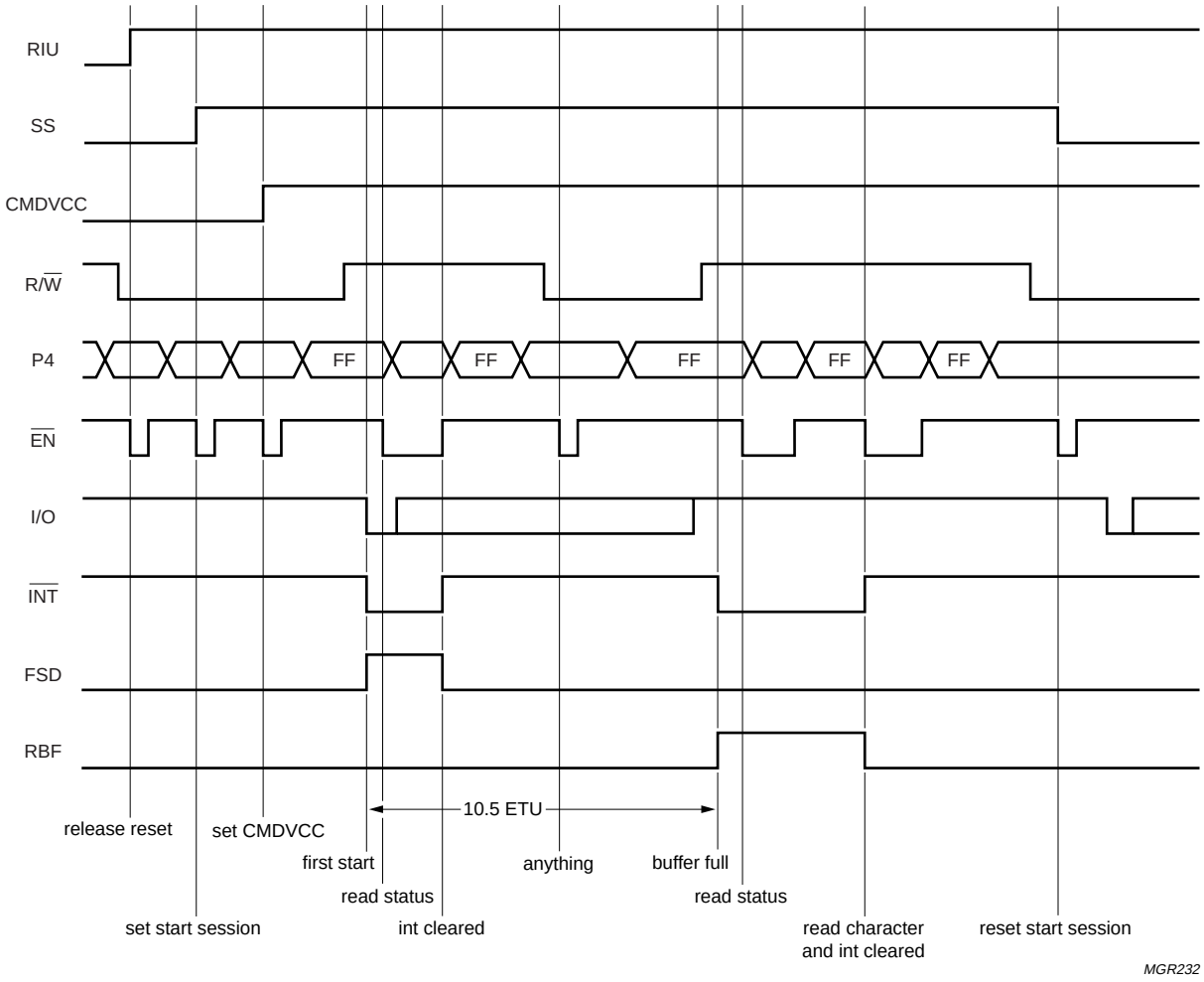


Fig.8 First character reception.

TRANSMISSION

Transmission mode is selected when TRN is HIGH.
If enabled, an interrupt is given on the rising edge of TRN, telling that the transmission buffer is empty, and may be written for transmitting a character. The interrupt is cleared during the read status operation.

The character is written in the UTR on the falling edge of $\overline{EN}$ during the write operation, and its transmission starts on the rising edge of $\overline{EN}$.

The I/O line is read at 10.84 ETU for checking if the card has detected a parity error or not. Bit TBE is set within the USR at the same time, and an interrupt is given if enabled to inform that the transmission buffer is empty, and that a new character may be written.

If the parity is correct, then the transmission of the next character will start at 12 ETU + GT +0.5 ETU after the start bit of the previous character (see Section “Extra guard time”).

If the parity was not correct, then the transmission will start at 13 ETU (the guard time GT must be programmed before starting to transmit). This assumes that a character has been written in the UTR.

It may be useful for some cards to change very fast from transmission to reception mode; bit LCT may be used for this purpose.

If LCT is set HIGH, then the UART automatically resets the bits TRN and LCT at 10.85 ETU if no parity error has occurred; the UART is ready to receive a character from the card at 12 ETU (T = 0) or 11 ETU (T = 1) after the previous start bit.

If a parity error has occurred during transmission of the last character, then the UART remains in transmission mode with LCT set, waiting for the software to rewrite the corrupted character.

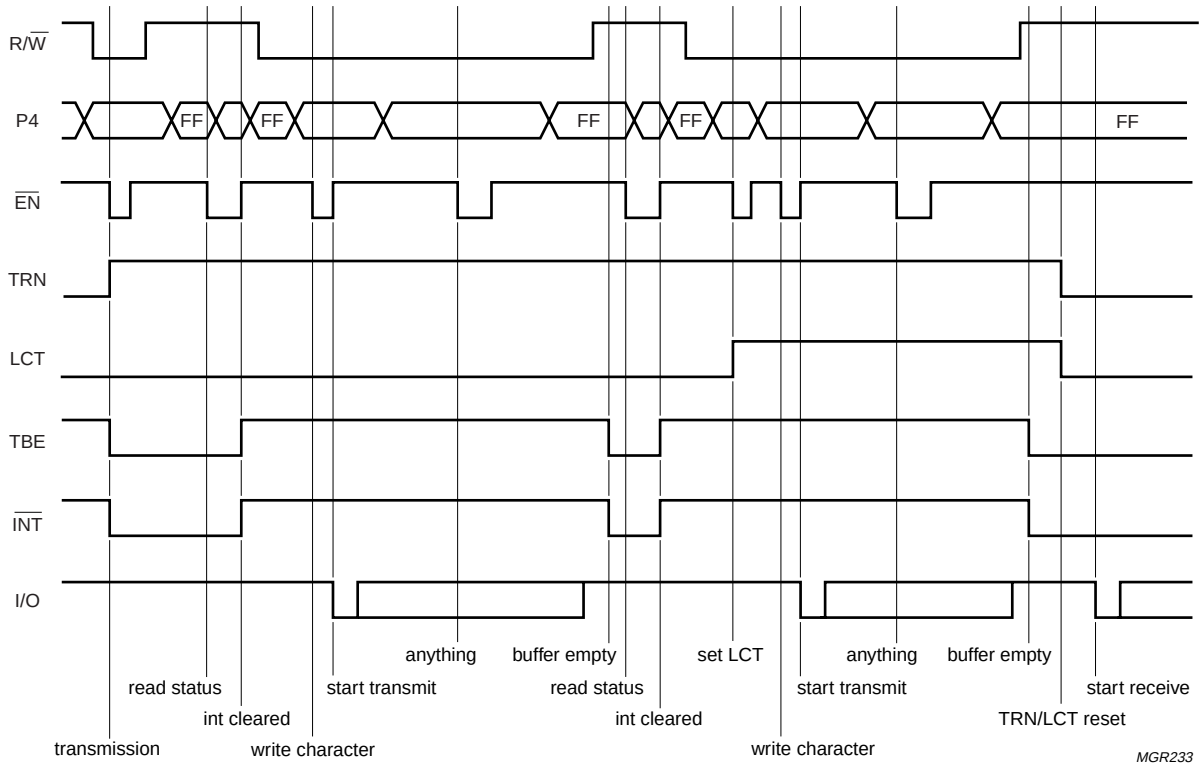


Fig.9 Character transmission without or with LCT.

SYNCHRONOUS CARDS

If bit SAN (Synchronous/Asynchronous-N) is set, then the software may deal with synchronous cards: the information available on the I/O line is copied on bit data 0 of the data bus when the SIR or SOR registers are selected, without entering the UART.

The synchronous clock may be controlled by selecting STOP HIGH or STOP LOW on CLK. C4 and C8 may be controlled by P34 and P35 (operation depending on synchronous card type).

Synchronous Input Register (SIR; address 3; read-only)

When this register is selected, then I/O is copied on data 0 (P40) and may be read by the controller.

Synchronous Output Register (SOR; address 3; write-only)

When this register is selected, then data 0 (P40) is copied on I/O on the falling edge of $\overline{EN}$.

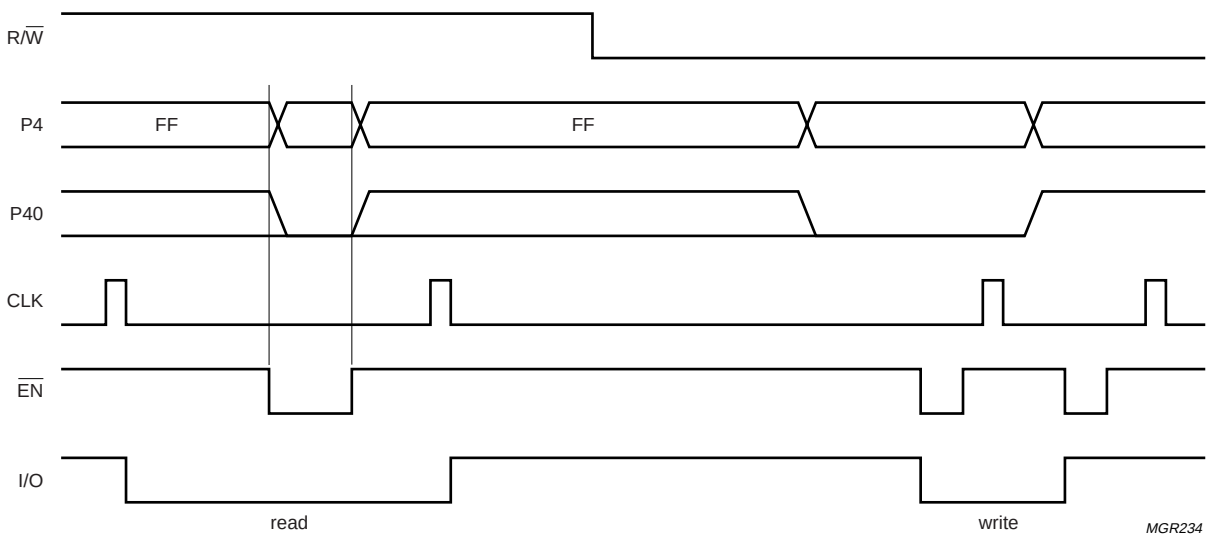


Fig.10 Synchronous cards use.

EXTRA GUARD TIME

Table 10 Guard Time Register (GTR; address 6; write-only; all bits cleared after reset)

D7	D6	D5	D4	D3	D2	D1	D0	GUARD TIME T = 0	GUARD TIME T = 1
x7	x6	x5	x4	x3	x2	x1	x0	x7x6x5x4x3x2x1x0H	x7x6x5x4x3x2x1x0H
1	1	1	1	1	1	1	1	0	–1

Between the transmission of two characters to the card, the ISO 7816 UART automatically inserts a number of guard ETUs equal to the value stored in the GTR (called GT). FFH has a special status: FFH means 0 ETU in protocol T0 and –1 ETU in protocol T1 (which means reception and transmission possible at 11 ETU).

Reception and transmission register

UART Receive Register (URR; address 4; read-only; all bits cleared after reset)

D7 to D0 are the bits of the data received from the card. Due to the fact that the UART automatically converts the characters according to the convention recognized during TS, all characters within the URR are in direct convention.

The received character is loaded in the URR 0.5 ETU after the shift of the parity, i.e. 10.5 ETU after the edge of the start bit; this implies that the previous character must have been read by the controller before, otherwise it is overwritten.

The UART checks the parity of the received characters; if the parity is wrong, then bit PE is set within the status at the same time than bit RBF (receive buffer full).

In protocol T = 0, I/O is pulled low between 10.5 and 11.75 ETU in case of error. Characters may be received from the card every 12 ETU, even after a transmission (see LCT use; Table 9). In protocol T = 1, the reception is possible at 11 ETU.

UART Transmit Register (UTR; address 4; write-only; all bits cleared after reset)

Bits D7 to D0 are the bits of the data to be transmitted to the card. Due to the automatic conversion performed by the UART according to convention detected during TS, the controller must write the characters to send to the card in direct convention.

The character to send may be written in the UTR as soon as bit TBE within the status register (transmit buffer empty) is set.

If the UCR writing occurs beyond 12.5 ETU + GT after the previous start bit, then the transmission starts on the rising edge of $\overline{EN}$ during the write operation. If this occurs before, then the UART will wait until 12.5 ETU + GT after the previous start bit for starting the transmission.

In protocol T = 0, in case of parity error signalled by the card, the previous character must be rewritten in UTR. Then the UART will wait 13 ETU after the start bit of the previous character before restarting the transmission.

STATUS REGISTER AND INTERRUPTS

The ISO 7816 UART reports its activity to the microcontroller by means of the UART status register, which acts upon the interrupt line $\overline{INT}$.

Table 11 UART Status Register (USR; address 5; read-only; all bits cleared after reset except for D5)

BIT	NAME	DESCRIPTION
D0	TX Buffer Empty (TBE)	this bit is set when the UART has finished transmitting the data written in the UTR (at 10.8 ETU) or on the rising edge of TRN; it is reset on the rising edge of $\overline{EN}$ during a read status operation
D1	RX Buffer Full (RBF)	this bit is set when the UART has finished receiving a character from the card (at 10.5 ETU); it is reset on the falling edge of $\overline{EN}$ during the read character operation
D2	First Start Detect (FSD)	this bit is set on the falling edge of the first start bit if SS = 1; it is reset on the rising edge of $\overline{EN}$ during a read status operation
D3	Parity Error (PE)	this bit is set when a parity error has been detected by the UART in transmission or in reception mode, at the same time as TBE and RBF; it is reset on the rising edge of $\overline{EN}$ during a read status operation
D4	Early Answer (EA)	this bit is set if a start bit has been detected on I/O between the 200 and the 400 first CLK pulses when the UART is configurated in automatic ATR processing; it is reset on the rising edge of $\overline{EN}$ during a read status operation
D5	OFF	this bit is set if the card is present and reset if the card is not present; if CMDVCC is set HIGH, it may also be reset if a hardware problem causing an emergency deactivation sequence has occurred
D6	Off Interrupt (OFFI)	this bit is set when OFF state has changed; it is reset on the rising edge of $\overline{EN}$ during a read status operation
D7	Mute Card (MC)	this bit is set if a card has not answered after 90000 CLK pulses when the ISO 7816 UART is configurated in automatic ATR processing; it is reset on the rising edge of $\overline{EN}$ during a read status operation

All bits except for D5 generate an interrupt on $\overline{INT}$ (if enabled) when they are set. D0, D2, D3, D4, D6 and D7 are cleared on the rising edge of $\overline{EN}$ after a read operation of USR. D1 is cleared when the data in the reception buffer has been read-out. D5 may be used to check the cards presence and also to determine that reason of an emergency deactivation during a cards session. In case of Early Answer (EA) or Mute Card (MC) during automatic ATR processing, the card is not automatically deactivated. An interrupt is generated if enabled, and it is up to the controller to deactivate or not.

Auxiliary RAM (MAR0, address C or D, write-only; MAR1, address E or F, write-only; MRR, MWR, address 8 or 9, read/write; all bits cleared after reset)

In order to store data, 1 kbytes of auxiliary RAM may be accessed through the peripheral interface. The content of the RAM is undefined after reset. It should be noted that only AD3, AD2 and AD1 must be programmed for addressing the RAM register, allowing faster operations if needed.

There are two ways for addressing this memory:

- Random way: the low order address is written in MAR0, and the high order address is written in MAR1. Then a write operation to MWR will write the data at the preselected address on the falling edge of $\overline{EN}$, and a read operation to MRR will load on P4 the data that is stored at the preselected address on the falling edge of $\overline{EN}$.
- Sequential way: once low order and high order addresses are written in MAR0 and MAR1, every read or write operation to MRR or MWR will increment the address that is stored in MAR0 and MAR1. Thus it is possible to read or write data strings within the auxiliary RAM without rewriting the addresses between 2 databyte. The autoincrement feature is operational on the whole length of the RAM. In case of overflow, the count starts again at address 00H.

Output Ports Extension Register (PER, address 7, write-only; all bits cleared after reset)

Within this register, the four low order bits are used for controlling the activation of the card. The four high order bits D4, D5, D6 and D7 control auxiliary ±2 mA push-pull output ports, which can be used for any purpose (LEDs, control signals, etc.). The electrical state of the ports is HIGH if the bit is LOW, and LOW if the bit is HIGH. The bits are cleared after reset, so the ports are HIGH.

Activation sequence

When the card is inactive, pins V_{CC}, CLK, RST and I/O are LOW, with low impedance with respect to GND.
The step-up converter is stopped. The I/O is configured in the reception mode with a high impedance path to the ISO 7816 UART, subsequently no spurious pulse from the card during power-up will be taken into account until I/O is enabled. When requirements are fulfilled (voltage supply, card present, no hardware problems), the microcontroller may initiate an activation sequence by setting bit CMDVCC HIGH (t_0).

- The step-up converter is started (t_1)
- V_{CC} starts rising from 0 to 5 V or 3 V with a controlled rise time of 0.16 V/µs typically (t_2)
- I/O, C4 and C8 buffers are enabled (t_3); integrated pull-up resistors of 10 kΩ are connected to V_{CC}
- CLK is sent to the card (t_4)
- RST buffer is enabled (t_5).

In order to allow a precise count of clock pulses during ATR in manual mode, a defined time window (t_3/t_5) is opened where the clock may be sent to the card by means of RSTIN. Beyond this window, RSTIN does not respond on a clock pulse, and only monitors the cards RST contact.

In automatic mode (ATREN set HIGH), RST is monitored by the TDA8006, RSTIN has no action and CLK is sent by the TDA8006 at t_3. RST is LOW until 45000 CLK pulses, if the card has not started to answer before, and is then set HIGH for again a maximum of 45000 CLK pulses.

It is also possible to make customized activation sequence by keeping CLK STOP LOW with RSTIN LOW beyond t_5, and then apply CLK by means of CLK configuration.

The sequencer is clocked by $\frac{1}{64}f_{INT}$ which leads to a time interval T of 25 µs typical. Thus $t_1 = 0$ to $\frac{1}{64}T$, $t_2 = t_1 + T$, $t_3 = t_1 + 4T$, $t_4 = t_3$ to t_5 and $t_5 = t_1 + 7T$.

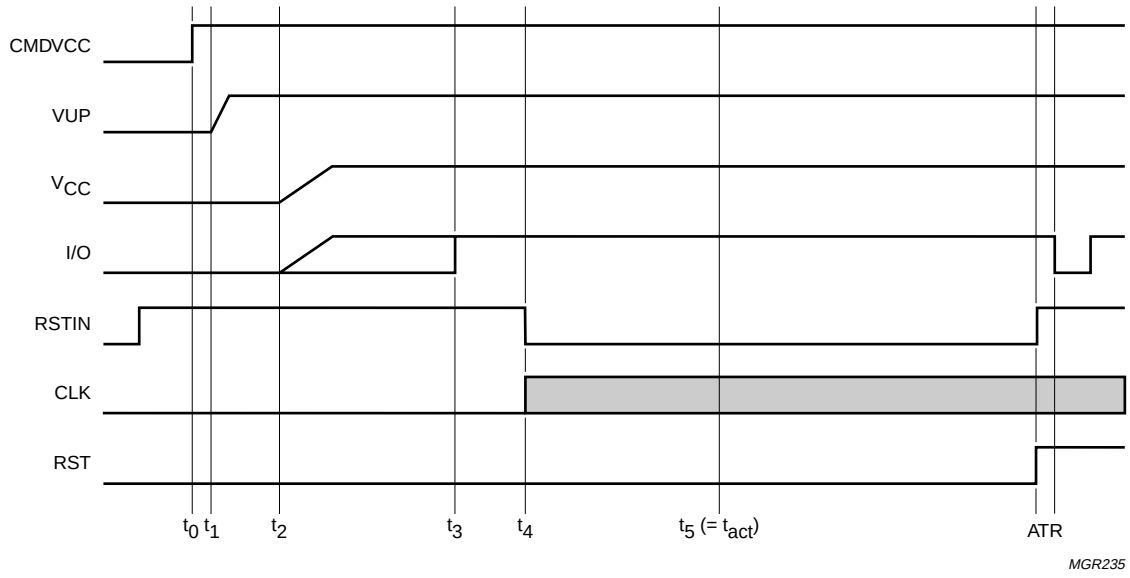


Fig.11 Manual activation sequence using t_3/t_5.

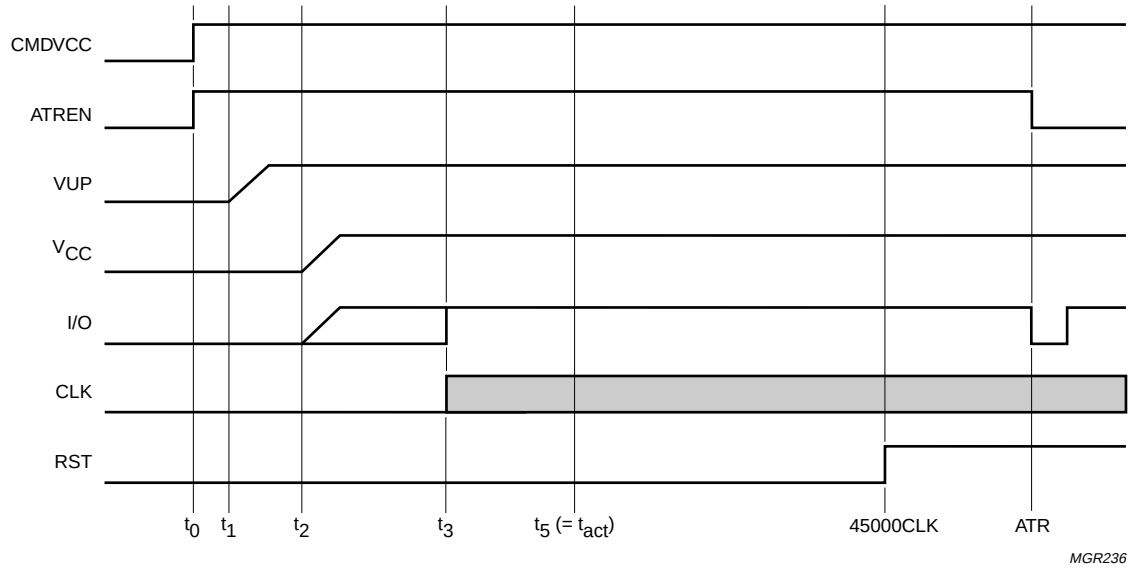


Fig.12 Automatic activation sequence.

Deactivation sequence

When the session is completed, the microcontroller sets CMDVCC LOW (t_{10}). The circuit then executes an automatic deactivation sequence:

- Card reset (RST goes LOW) (t_{11})
- Clock is stopped (t_{12})
- I/O becomes high impedance to the ISO 7816 UART (t_{13})
- V_{CC} falls to 0 V with typical 0.16 V/µs slew rate (t_{14})
- The step-up converter is stopped and CLK, RST, V_{CC} and I/O become low impedance to GND (t_{15}).

$t_{11} = t_{10} + 1/64T$, $t_{12} = t_{11} + 1/2T$, $t_{13} = t_{11} + T$, $t_{14} = t_{11} + 3/2T$, $t_{15} = t_{11} + 5T$.

t_{de} is the time that V_{CC} needs for going down to less than 0.3 V.

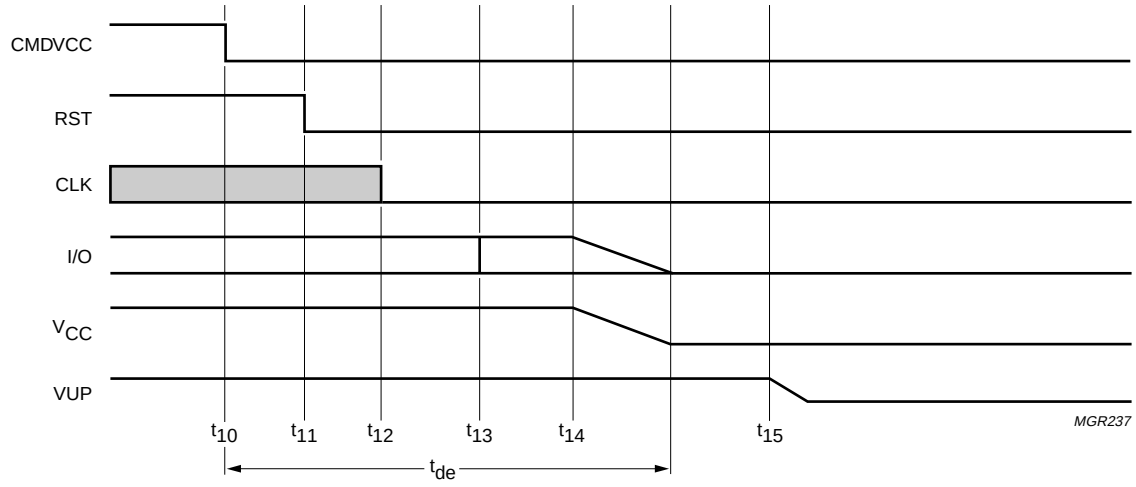


Fig.13 Deactivation sequence.

Protections

Main hardware fault conditions are monitored by the circuit:

- Overcurrent on V_{CC}
- Short-circuits between V_{CC} and other contacts
- Card take-off during transaction.

When one of these problems is detected, the security logic block sets the OFF bit LOW, which generates an interrupt in order to warn the microcontroller, and initiates an automatic deactivation of the contacts.

When the deactivation has been completed and CMDVCC has been set LOW, the OFF bit returns HIGH, except if the problem was due to a card extraction in which case it remains LOW until a card is inserted.

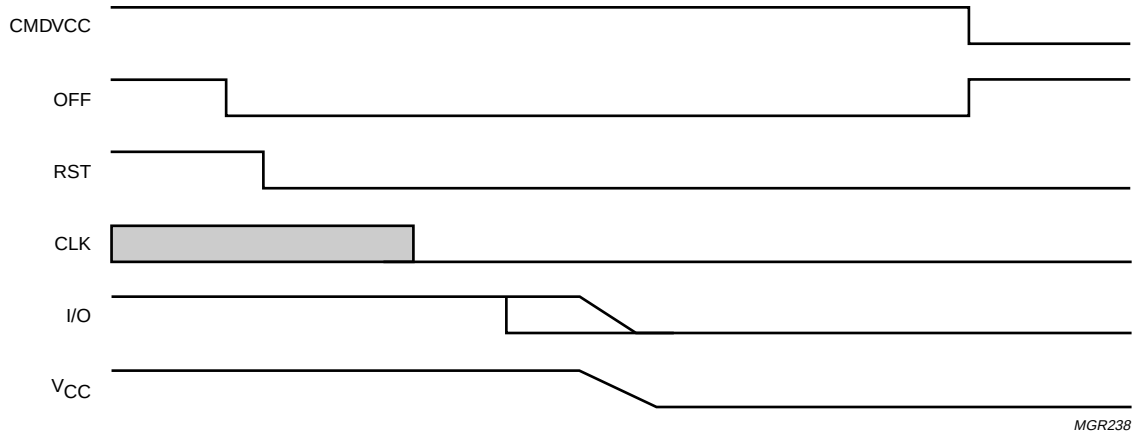


Fig.14 Emergency deactivation sequence after V_{CC} short-circuited to ground.

Auxiliary contacts C4 and C8

The auxiliary contacts C4 and C8 are controlled with P34 and P35 through two identical pseudo-bidirectional I/O lines.

In the Idle state P34 is pulled HIGH to V_{DD} through an integrated resistor of 20 kΩ and C4 is pulled HIGH to V_{CC} through an integrated resistor of 10 kΩ. This allows operation with a V_{CC} value of 3 V and a V_{DD} value of 5 V. The first side on which a falling edge occurs becomes the master. An anti-latch circuitry disables the detection of falling edge on the other side, which becomes the slave.

After a delay of approximately 200 ns (t_d), the N transistor on the slave side is turned on, thus transmitting the ‘0’ present on the master side. When the master side goes back to logic 1, the P transistor on the slave side is turned on during t_d, and then both sides return to their idle states.

The maximum frequency on the I/O lines is 1 MHz.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage		–0.5	+6.5	V
V_{DDD}	digital supply voltage		–0.5	+6.5	V
V_{n1}	all input voltages except S1, S2 and VUP		–0.5	V_{DD} + 0.5	V
V_{n2}	voltage on pins S1, S2 and VUP		–0.5	+7.5	V
I_{n1}	DC current into XTAL1, XTAL2, P30/RXD, P31/TXD, RESET, P33/INT1, P36/$\overline{WR}$, P37/$\overline{RD}$, P00 to P07, P20 to P27, P10/T2, P11/T2EX, $\overline{EA}$, ALE, $\overline{PSEN}$, CDELAY, PRES, INHIB, CLKOUT and TEST		–5	+5	mA
I_{n3}	DC current from or to pins S1, S2 and VUP		–200	+200	mA
I_{n6}	DC current from or to $\overline{K0}$ to $\overline{K3}$		–5	+5	mA
I_{n7}	DC current from or into pin ALARM (according to option choice)	see Table 12	–5	+5	mA
P_{tot}	total power dissipation	T_{amb} = –20 to +85 °C			
	QFP44		–	400	mW
	QFP64		–	500	mW
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–	140	°C
V_{esd}	electrostatic discharge	on pins I/O, V_{CC} RST, CLK, C4, C8 and PRES	–6	+6	kV
		on other pins	–2	+2	kV

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	QFP64		51	K/W
	QFP44		64	K/W

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C; for general purpose I/O ports refer to 80CE560 data sheet; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		4.2	–	6.0	V
V_{DDD}	digital supply voltage		4.2	–	6.0	V
$I_{DD(pd)}$	supply current in power-down mode	V_{DD} = 5 V; card inactive; note 1	–	–	250	µA
$I_{DD(sm)}$	supply current in sleep mode	card powered, microcontroller in power-down mode but with clock stopped; note 1	–	–	1500	µA
$I_{DD(om)}$	supply current operating mode	I_{CC} = 65 mA; f_{xtal} = 20 MHz; f_{clk} = 10 MHz; f_{osc} = 20 MHz; f_{CLKOUT} = 20 MHz; 5 V card; notes 1 and 2	130	–	180	mA
		I_{CC} = 65 mA; f_{xtal} = 20 MHz; f_{clk} = 10 MHz; f_{osc} = 20 MHz; f_{CLKOUT} = 20 MHz; 3 V card; notes 1 and 2	65	–	90	mA
		unloaded; f_{xtal} = 20 MHz; f_{clk} = 5 MHz; f_{osc} = 10 MHz; f_{CLKOUT} = 5 MHz; 5 V card; notes 1 and 2	1	–	6	mA
		unloaded; f_{xtal} = 20 MHz; f_{clk} = 5 MHz; f_{osc} = 10 MHz; f_{CLKOUT} = 5 MHz; 3 V card; notes 1 and 2	0.5	–	4	mA
$V_{th(VDD)}$	threshold voltage on V_{DD} (falling)		3.6	–	3.95	V
$V_{hys(VthVDD)}$	hysteresis on $V_{th(VDD)}$		50	–	250	mV
$V_{th(CDELAY)}$	threshold voltage on pin CDELAY		–	1.38	–	V
V_{CDELAY}	voltage on pin CDELAY		–	–	V_{DD}	V
I_{CDELAY}	output current at pin CDELAY	pin grounded (charge)	–	–1	–	µA
		V_{CDELAY} = V_{DD} (discharge)	–	2	–	mA
t_W	ALARM pulse width	C_{CDELAY} = 10 nF	–	10	–	ms
ALARM (open drain active HIGH or LOW output)						
I_{OH}	HIGH-level output current	active LOW option; V_{OH} = 5 V	–	–	10	µA
V_{OL}	LOW-level output voltage	active LOW option; I_{OL} = 2 mA	–0.3	–	+0.4	V
I_{OL}	LOW-level output current	active HIGH option; V_{OL} = 0 V	–	–	–10	µA
V_{OH}	HIGH-level output voltage	active HIGH option; I_{OH} = –2 mA	V_{DD} – 0.8	–	V_{DD} + 0.3	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal oscillator						
f_{xtal}	crystal frequency		4	–	25	MHz
f_{ext}	frequency of external signal applied on pin XTAL1		0	–	25	MHz
CLKOUT						
f_{CLKOUT}	frequency on pin CLKOUT		0	–	25	MHz
V_{OL}	LOW-level output voltage	I_{OL} = 5 mA	–	–	0.8	V
V_{OH}	HIGH-level output voltage	I_{OH} = –5 mA	V_{DD} – 1	–	–	V
$t_{o(r)}$	output rise time	C_L = 60 pF	–	–	10	ns
$t_{o(f)}$	output fall time	C_L = 60 pF	–	–	10	ns
δ	duty factor	C_L = 60 pF	40	–	60	%
Step-up converter						
f_{INT}	internal oscillation frequency		2	2.5	3	MHz
V_{VUP}	voltage on pin VUP		–	6.5	–	V
Reset output to the card (pin RST)						
$V_{o(RST)}$	output voltage	inactive mode; no load	0	–	0.1	V
		inactive mode; $I_{o(RST)}$ = 1 mA	0	–	0.3	V
$I_{o(RST)}$	output current	when inactive and pin grounded	0	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 μA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –200 μA	V_{CC} – 0.7	–	V_{CC}	V
t_r	rise time	C_L = 30 pF	–	–	0.1	μs
t_f	fall time	C_L = 30 pF	–	–	0.1	μs
Clock output to the card (pin CLK)						
$V_{o(CLK)}$	output voltage	inactive mode; no load	0	–	0.1	V
		inactive mode; $I_{o(CLK)}$ = 1 mA	0	–	0.3	V
$I_{o(CLK)}$	output current	when inactive and pin grounded	0	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 μA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –200 μA	V_{CC} – 0.5	–	V_{CC}	V
t_r	rise time	C_L = 30 pF	–	–	8	ns
t_f	fall time	C_L = 30 pF	–	–	8	ns
f_{CLK}	clock frequency	1.25 MHz idle configuration	1	1.25	1.5	MHz
		operational	0	–	10	MHz
δ	duty factor	C_L = 30 pF	45	–	55	%
SR	slew rate (rise and fall)	C_L = 30 pF	0.2	–	–	V/ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Card supply voltage (pin V_{CC}); note 3						
$V_{O(VCC)}$	card supply output voltage	inactive				
		no load	0	–	0.1	V
		$I_{O(VCC)}$ = 1 mA	0	–	0.3	V
		pin grounded	0	–	–1	mA
		active				
		I_{CC} < 65 mA; 5 V card	4.75	5	5.25	V
		I_{CC} < 65 mA; 3 V card	2.8	3	3.2	V
		current pulses of 40 nAs with I_{CC} < 200 mA; t < 400 ns; f < 20 MHz; 5 V card	4.6	–	5.4	V
		current pulses of 24 nAs with I_{CC} < 200 mA; t < 400 ns; f < 20 MHz; 3 V card	2.75	–	3.25	V
$I_{O(VCC)}$	card supply output current	from 0 to 3 or 5 V	–	–	65	mA
		V_{CC} short-circuited to GND	–	–	250	mA
$I_{CC(sd)}$	shutdown current at pin V_{CC}		–	–80	–	mA
SR	slew rate	up or down (capacitor = 100 to 300 nF)	0.10	0.16	0.22	V/µs
Data line (pin I/O); note 4						
$V_{o(I/O)}$	output voltage	inactive				
		no load	0	–	0.1	V
		$I_{o(I/O)}$ = 1 mA	–	–	0.3	V
$I_{o(I/O)}$	output current	inactive and pin grounded	0	–	–1	mA
V_{OL}	LOW-level output voltage	I/O configured as output; I_{OL} = 1 mA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I/O configured as output; I_{OH} < –50 µA	$0.8V_{CC}$	–	V_{CC} + 0.25	V
V_{IL}	LOW-level input voltage	I/O configured as input	–0.3	–	+0.8	V
V_{IH}	HIGH-level input voltage	I/O configured as input	1.5	–	V_{CC}	V
I_{IL}	LOW-level input current	V_{IL} = 0 V	–	–	–600	µA
I_{LIH}	HIGH-level input leakage current	$V_{IH} = V_{CC}$	–	–	20	µA
$t_{i(r)}$	input rise time	C_L = 30 pF	–	–	1	µs
$t_{i(f)}$	input fall time	C_L = 30 pF	–	–	1	µs
$t_{o(r)}$	output rise time	C_L = 30 pF	–	–	0.1	µs
$t_{o(f)}$	output fall time	C_L = 30 pF	–	–	0.1	µs
$R_{pu(int)}$	internal pull-up resistance between I/O and V_{CC}		8	10	13	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Auxiliary cards contacts (C4 and C8); note 5						
$V_{o(C4,C8)}$	output voltage	inactive				
		no load	0	–	0.1	V
		$I_{o(C4,C8)}$ = 1 mA	–	–	0.3	V
$I_{o(C4,C8)}$	output current	inactive and pin grounded	–	–	–1	mA
V_{OL}	LOW-level output voltage	C4 or C8 configured as output; I_{OL} = 1 mA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	C4 or C8 and I/O configured as output; I_{OH} < –50 µA	$0.8V_{CC}$	–	V_{CC} + 0.25	V
V_{IL}	LOW-level input voltage	C4 or C8 configured as input	–0.3	–	+0.8	V
V_{IH}	HIGH-level input voltage	C4 or C8 configured as input	1.5	–	V_{CC}	V
I_{IL}	LOW-level input current	V_{IL} = 0 V	–	–	–600	µA
I_{LIH}	HIGH-level input leakage current	$V_{IH} = V_{CC}$	–	–	±20	µA
$t_{i(r)}$	input rise time	C_L = 30 pF	–	–	1	µs
$t_{i(f)}$	input fall time	C_L = 30 pF	–	–	1	µs
$t_{o(r)}$	output rise time	C_L = 30 pF	–	–	0.1	µs
$t_{o(f)}$	output fall time	C_L = 30 pF	–	–	0.1	µs
t_d	delay between falling edge on P34 and C4 (or C4 and P34)		–	–	200	ns
$R_{pu(int)}$	internal pull-up resistance between C4 and V_{CC} and C8 and V_{CC}		8	10	13	kΩ
$f_{(max)}$	maximum frequency on C4 or C8		–	–	1	MHz
Timing						
t_{act}	activation sequence duration		–	–	225	µs
t_{de}	deactivation sequence duration		–	–	100	µs
$t_{3(start)}$	start of the window for sending clock to the card		–	–	130	µs
$t_{5(end)}$	end of the window for sending clock to the card		145	–	–	µs
Output ports from extension ($\overline{K0}$ to $\overline{K3}$)						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –2 mA	V_{DD} – 1	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Card presence input (pin PRES)						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	–	V
I_{LIL}	LOW-level input leakage current	V_i = 0 V	–	–	20	µA
I_{LIH}	HIGH-level input leakage current	$V_i = V_{DD}$	–	–	20	µA

Notes

1. I_{DD} in all configurations include the current at pins V_{DD}, V_{DDA} and V_{DDRAM}.
2. Values given for program execution out of internal ROM. If execution out of external ROM or charges connected to I/O ports, current consumption may be higher.
3. A ceramic multilayer capacitance with low ESR of minimum 100 nF should be used in order to meet these specifications.
4. The I/O line has an integrated pull-up resistor of 10 kΩ at pin V_{CC}.
5. Pins C4 and C8 have integrated pull-up resistors of 10 kΩ at pin V_{CC}; P34 and P35 have integrated pull-up resistors of 20 kΩ at pin V_{DD}.

OPTIONS

Table 12 Options table

FEATURES	OPTIONS	
Alarm	active HIGH	active LOW
Presence	active HIGH	active LOW
MOVEC protection	on	off

APPLICATION INFORMATION

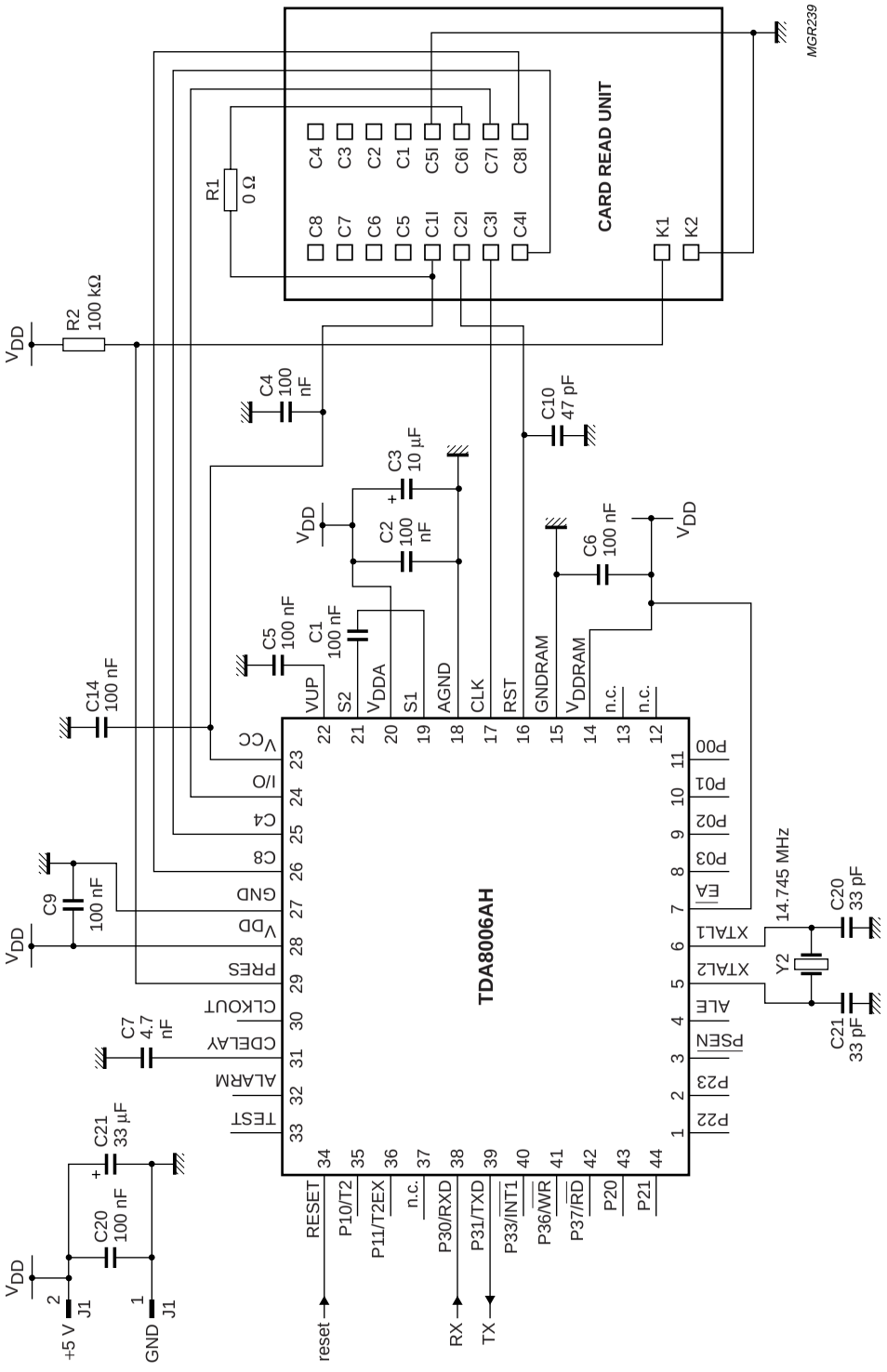
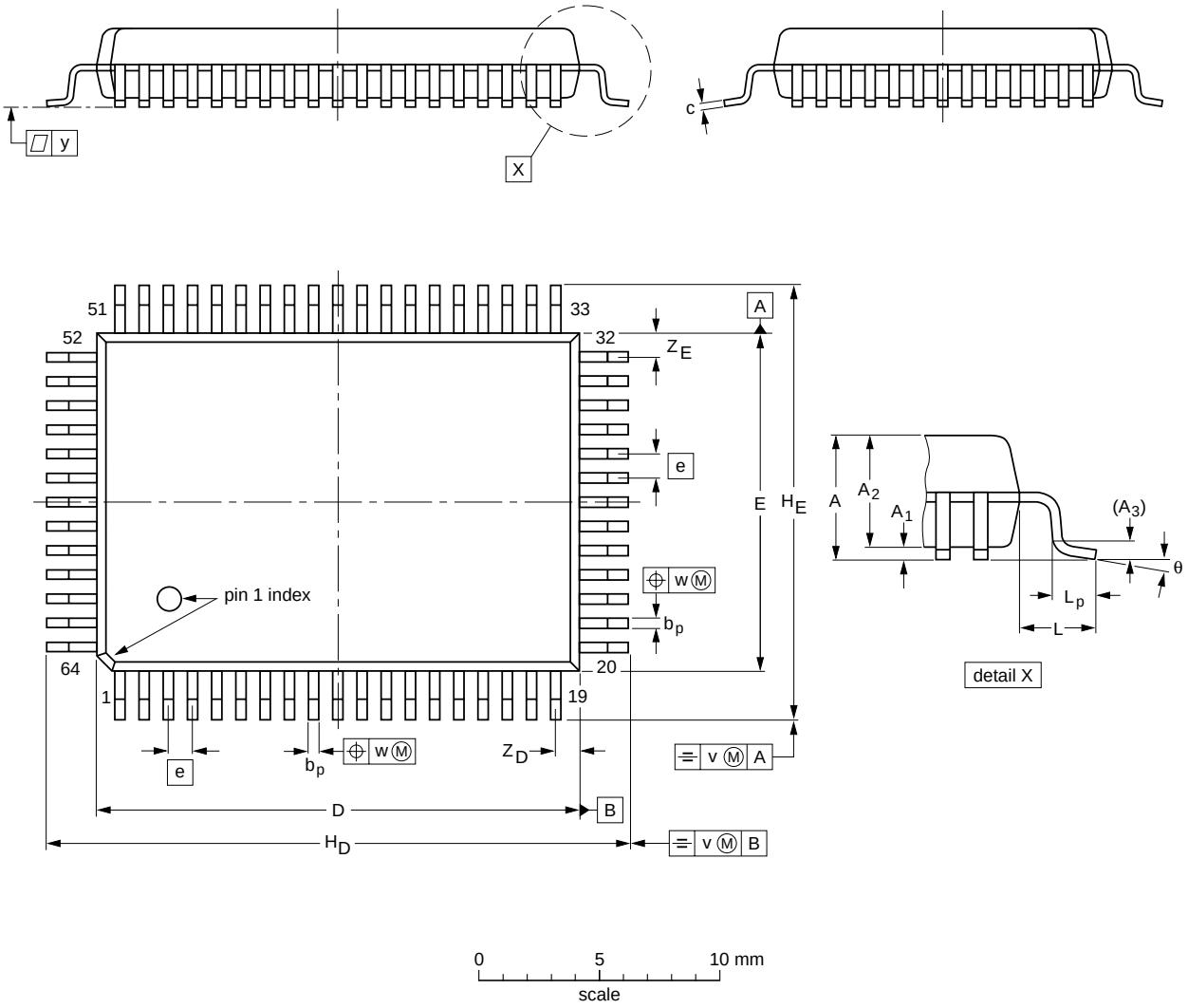


Fig.15 Application diagram.

PACKAGE OUTLINES

QFP64: plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT319-2**



DIMENSIONS (mm are the original dimensions)

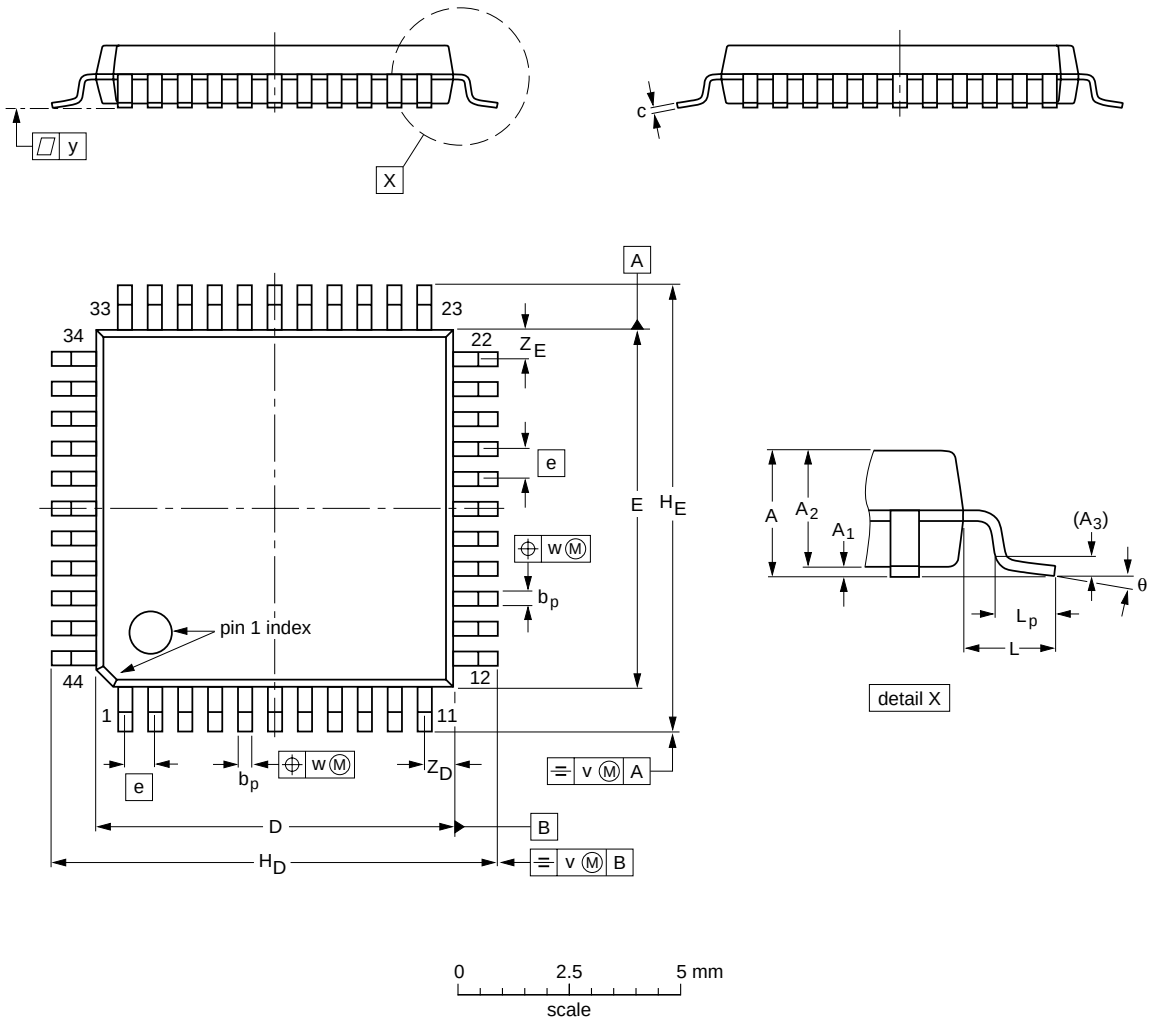
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.50 0.35	0.25 0.14	20.1 19.9	14.1 13.9	1	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-2						~~95-02-04~~ 97-08-01

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
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SOT307-2						~~95-02-04~~ 97-08-01

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION
Wave soldering is NOT applicable for all QFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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