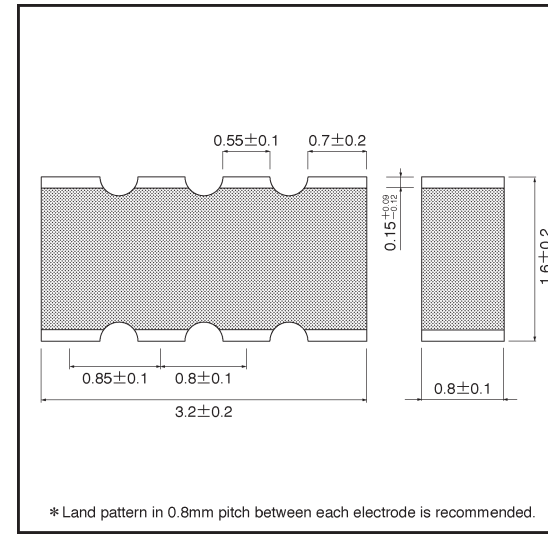
Multi–layer ceramic chip capacitor networks

MNA14 (1608 (0603) × 4 size, chip capaitor networks)

●Features

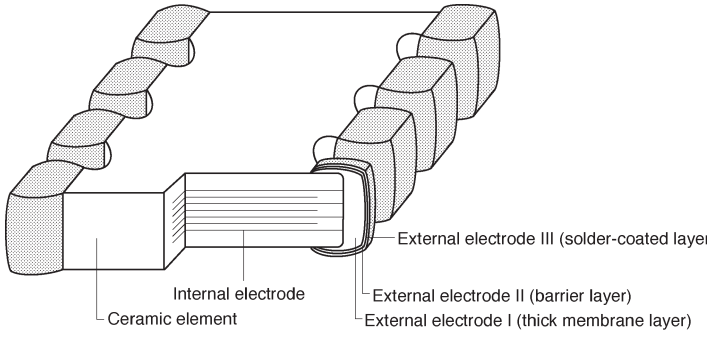
1) Area ratio is approximately 55% smaller than that of the MCH18, enabling high–density mounting.
2) Mounting costs are reduced.
3) Use of convex electrodes prevents solder bridging during mounting, and makes it easy to perform a visual inspection of the mounted piece. Also facilitates automatic inspection.
4) Solder–coated terminals offer superior solderbility and resistance to soldering heat.
5) Each element is independent to ensure a wide range of circuit applications.
6) Can be packed on tape.

●External dimensions (Units: mm)

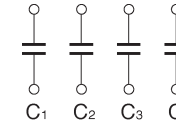


∗Land pattern in 0.8mm pitch between each electrode is recommended.

●Structure



●Equivalent circuits



$C_1 = C_2 = C_3 = C_4$

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●Product Designation

Code	Product thickness	Packaging specifications	Reel	Basic ordening unit (pcs.)
K	0.8mm	Paper tape (width 8 mm, pich 4 mm)	φ180mm (7in.)	4,000

Reel (φ180mm) : EIAJ ETX-7001

Part No. **Packaging style**

M	N	A	1	4	5	A	1	0	1	K	K

Rated voltage

Code	Voltage
2	25V
5	50V

Capacitance-temperature characteristics				Nominal capacitance	Capacitance tolerance	
Code	EIA code	Operating temperature range (°C)	Temp. coefficient or percent change		Code	tolerace
A	C0G	−55～+125	0±30ppm / °C	3-digit designation according IEC	K	±10%
C	X7R	−55～+125 (−25～+85)	±15% (±10%)		M	±20%

●Capacitance range

Product name		MNA 14	
Capacitance (pF)	Temperature characteristic	A (C0G)	C (X7R)
	Rated voltage	50V	25V
	Tolerance	K (±10%)	M (±20%)
10		▨	
22		▨	
47		▨	
100		▨	
220		▨	
470		▨	
1,000			▨
2,200			▨
4,700			▨
10,000			▨
22,000			▨

▨ Product thickness (mm) 0.8±0.1

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●Characteristics

Class 1 (For thermal compensation)

Item \ Temperature characteristics		A (C0G)	Test methods / conditions (based on JIS C 5102)
Operating temperature		−55℃～+125℃	————
Nominal capacitance (C)		Must be within the specified tolerance range.	Based on paragraph 7.8 and paragraph 9, Measured at room temperature and standard humidity. Measurement frequency : 1±0.1MHz Measurement voltage : 1±0.1Vrms.
Tan δ		100 / (400+20C)% or less: Less than 30 pF 0.1% or less: 30 pF or larger	
Insulation resistance (IR)		10,000 MΩ or larger, or 500 ΩF or larger, whichever is smaller	Based on paragraph 7.6. Measurement is made after rated voltage is applied for 60±5s.
Withstanding voltage		The insulation must not be damaged.	Based on paragraph 7.1. Apply 300% of the rated voltage for 1 to 5s then measure.
Temperature characteristics		Within 0±30ppm / ℃	The temperature coefficients in table 12, paragraph 7.12 are calculated at 20℃ and high temperature.
Terminal adherence		No detachment or signs of detachment.	Based on paragraph 8, 11, 2. Apply 5N (0.51 kg·f) for 10 ±1s in the direction indicated by the arrow. 
Resistance to vibration	Appearance	There must be no mechanical damage.	Chip is mounted to a board in the manner shown on the right, subjected to vibration (type A in paragraph 8.2), and measured 24±2 hours later. 
	Rate of capacitance change	Must be within initial tolerance.	
	Tan δ	Must satisfy initial specified value.	
Solderability		At least 3/4 of the surface of the two terminals must be covered with new solder.	Based on paragraph 8.13, Soldering temperature : 235±5℃ Soldering time : 2±0.5s
Resistance to soldering heat	Appearance	There must be no mechanical damage.	Based on paragraph 8.14. Soldering temperature : 260±5℃ Soldering time : 5±0.5s Preheating : 150±10℃ for 1 to 2 min.
	Rate of capacitance change	±2.5% or less, or ±0.25 pF or less, whichever is larger	
	Tan δ	Must satisfy initial specified value.	
	Insulation resistance	10,000 MΩ or larger, or 500 ΩF or larger, whichever is smaller	
	Withstanding voltage	The insulation must not be damaged.	
Temperature cycling	Appearance	There must be no mechanical damage.	Based on paragraph 9.3, Number of cycles: 10 Capacitance measured after 24±2 hrs.
	Rate of capacitance change	±2.5% or less, or ±0.25 pF or less, whichever is larger	
	Tan δ	Must satisfy initial specified value.	
	Insulation resistance	10,000 MΩ or larger, or 500 ΩF or larger, whichever is smaller	
Humidity load test	Appearance	There must be no mechanical damage.	Based on paragraph 9.9, Test temperature : 40±2℃ Relative humidity : 90% to 95% Applied voltage : rated voltage Test time : 500 to 524 hrs. Capacitance measured after 24±2 hrs.
	Rate of capacitance change	±7.5% or less, or ±0.75 pF or less, whichever is larger	
	Tan δ	0.5% or less	
	Insulation resistance	500 MΩ or larger, or 25 ΩF or larger, whichever is smaller	
High-temperature load test	Appearance	There must be no mechanical damage.	Based on paragraph 9.10, Test temperature : Max. operating temp. Applied voltage : rated voltage x 200% Test time : 1,000 to 1,048 hrs. Capacitance measured after 24±2 hrs.
	Rate of capacitance change	±3.0% or less, or ±0.3 pF or less, whichever is larger	
	Tan δ	0.3% or less	
	Insulation resistance	10,000 MΩ or larger, or 50 ΩF or larger, whichever is smaller	

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Class 2 (High dielectric constant)

Item \ Temperature characteristics		C (X7R)	Test methods/conditions (based on JIS C 5102)
Operating temperature		−55℃~+125℃	———
Nominal capacitance (C)		Must be within the specified tolerance range.	Based on paragraph 7.8 Measured at room temperature and standard humidity. Measurement frequency: 1 ±0.1 kHz Measurement voltage : 0.1 ±0.2 Vrms.
Tan δ		2.5% or less (when rated voltage is 16V: 3.5% or less)	
Insulation resistance (IR)		10,000 MΩ or larger, or 500 ΩF or larger, whichever is smaller	Based on paragraph 7.6 Measurement is made after rated voltage is applied for 60±5s.
Withstanding voltage		The insulation must not be damaged.	Based on paragraph 7.1 Apply 250% of the rated voltage for 1 to 5s then measure.
Temperature characteristics		Within ±15%	The temperature coefficients in paragraph 7.12, table 8, condition B, are based on measurements carried out at 20℃, with no voltage applied.
Terminal adherence		No peeling or sign of peeling on terminal.	Based on paragraph 8, 11, 2. Apply 5N (0.51 kg·f) for 10±1s in the direction indicated by the arrow. 
Resistance to vibration	Appearance	There must be no mechanical damage.	Chip is mounted to a board in the manner shown on the right, subjected to vibration (type A in paragraph 8.2), and measured 48±4 hrs. later. 
	Rate of capacitance change	Must be within initial tolerance.	
	Tan δ	Must satisfy initial specified value.	
Solderability		At least 3/4 of the surface of the two terminals must be covered with new solder.	Based on paragraph 8.13 Soldering temperature: 235 ±5℃ Soldering time : 2±0.5s
Resistance to soldering heat	Appearance	There must be no mechanical damage.	Based on paragraph 8.14. Soldering temperature: 260±5℃ Soldering time : 5±0.5s Preheating : 150±10℃ for 1 to 2 min.
	Rate of capacitance change	Within ±5.0%	
	Tan δ	Must satisfy initial specified value.	
	Insulation resistance	10,000 MΩ or larger, or 500 ΩF or larger, whichever is smaller	
	Withstanding voltage	The insulation must not be damaged.	
Temperature cycling	Appearance	There must be no mechanical damage.	Based on paragraph 9.3 Number of cycles: 10 Capacitance measured after 48 ±4 hrs.
	Rate of capacitance change	Within ±7.5%	
	Tan δ	Must satisfy initial specified value.	
	Insulation resistance	10,000 MΩ or larger, or 500 ΩF or larger, whichever is smaller	
Humidity load test	Appearance	There must be no mechanical damage.	Based on paragraph 9.9 Test temperature : 40 ±2℃ Relative humidity : 90% to 95% Applied voltage : rated voltage Test time : 500 to 524 hrs. Capacitance measured after 48 ±4 hrs.
	Rate of capacitance change	±12.5% or less	
	Tan δ	5.0%or less	
	Insulation resistance	500 MΩ or larger, or 25 ΩF or larger, whichever is smaller	
High-temperature load test	Appearance	There must be no mechanical damage.	Based on paragraph 9.10 Test temperature : Max. operating temp. Applied voltage : rated voltage x 200% Test time : 1,000 to 1,048 hrs. Capacitance measured after 48 ±4 hrs.
	Rate of capacitance change	Within ±10.0%	
	Tan δ	5.0% or less	
	Insulation resistance	1,000MΩ or larger, or 50 ΩF or larger, whichever is smaller	

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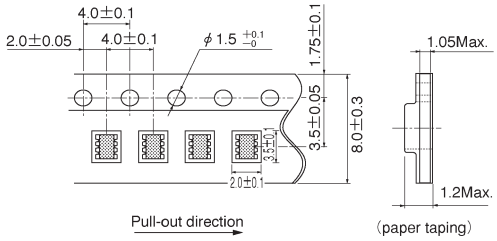
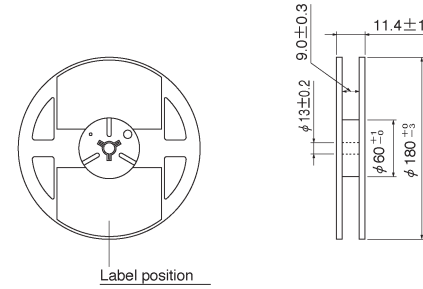
●Packaging

(Units: mm)

Taping	Reel
	

(φ180mm reel)

EIAJ ETX-7001 compliant

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●Electrical characteristics

■ A (C0G) characteristics

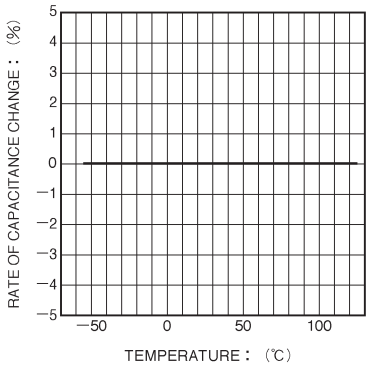

Fig.1 Capacitance-temperature characteristics

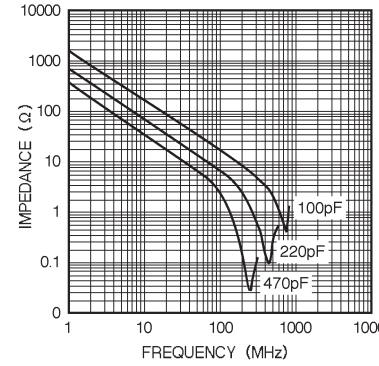

Fig.2 Impedance-frequency characteristics

■ C (X7R) characteristics

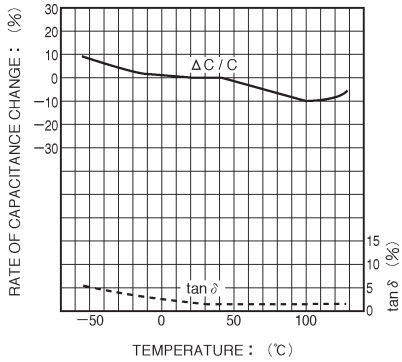

Fig.3 Capacitance-temperature characteristics

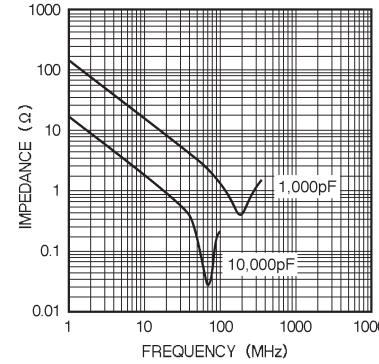

Fig.4 Impedance-frequency characteristics

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■ Temperature cycling test

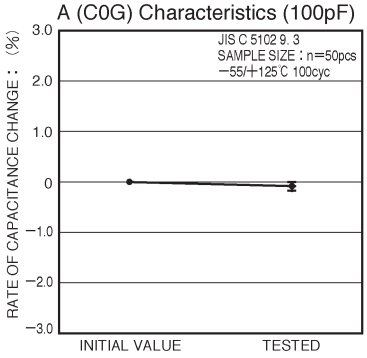

Fig.5 Rate of capacitance change

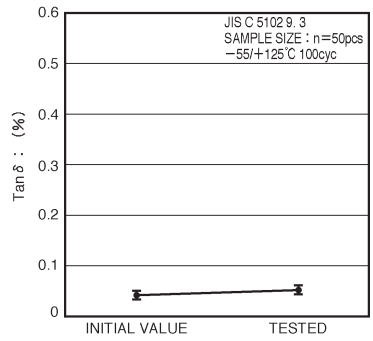

Fig.6 Tan δ

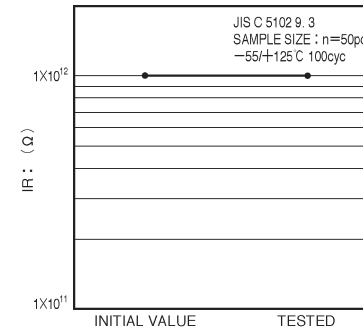

Fig.7 Insulation resistance

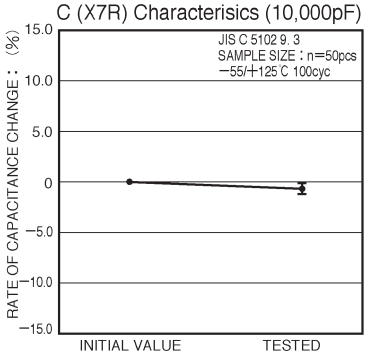

Fig.8 Rate of capacitance change

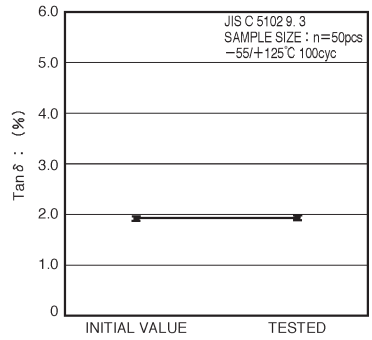

Fig.9 Tan δ

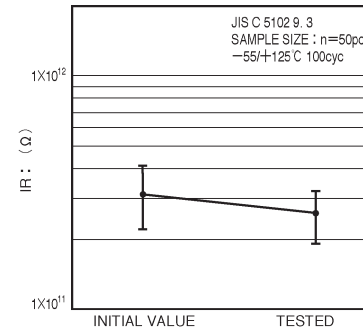

Fig.10 Insulation resistance

■ High–temperature load test

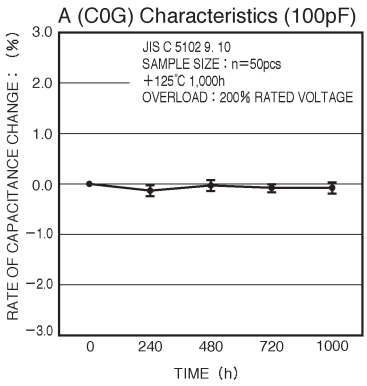

Fig.11 Rate of capacitance change

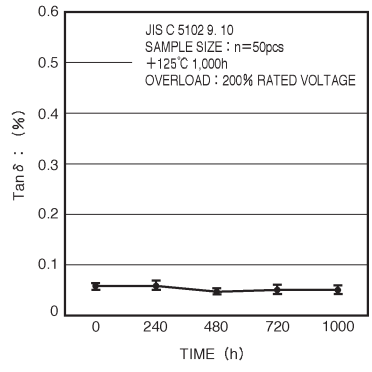

Fig.12 Tan δ

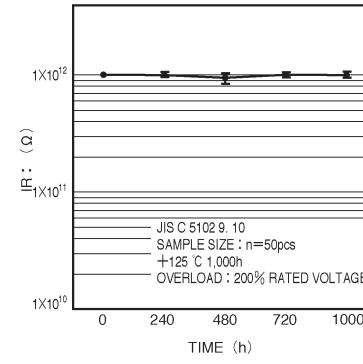

Fig.13 Insulation resistance

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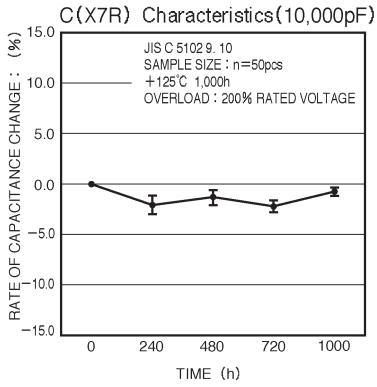

Fig.14 Rate of capacitance change

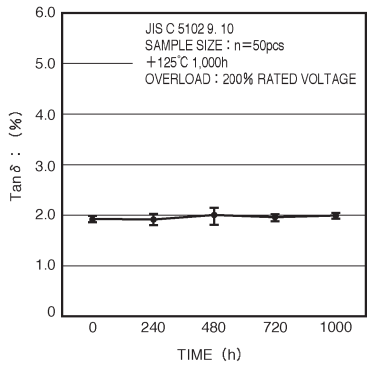

Fig.15 Tan δ

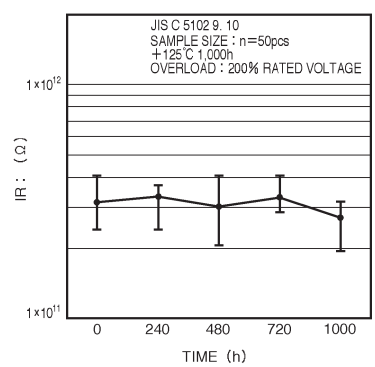

Fig.16 Insulation resistance

■ Humidity load test

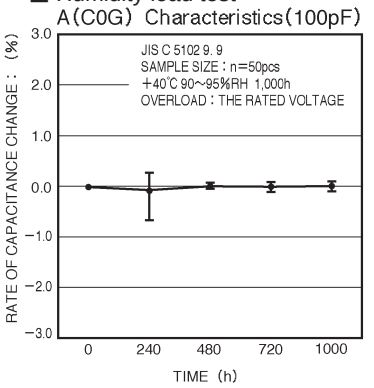

Fig.17 Rate of capacitance change

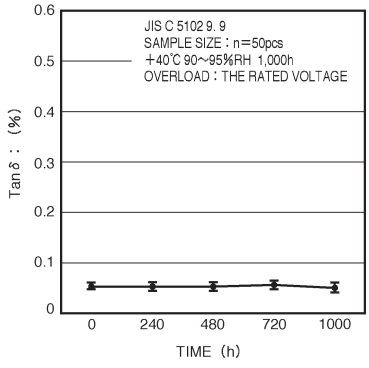

Fig.18 Tan δ

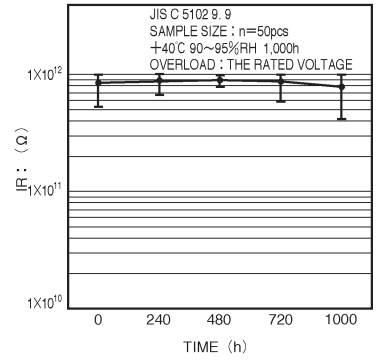

Fig.19 Insulation resistance

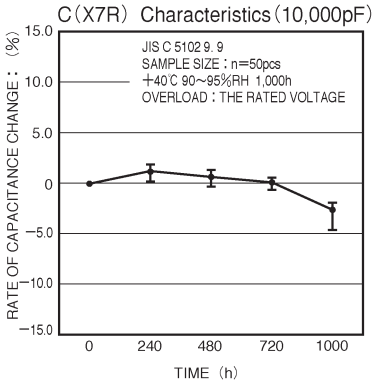

Fig.20 Rate of capacitance change

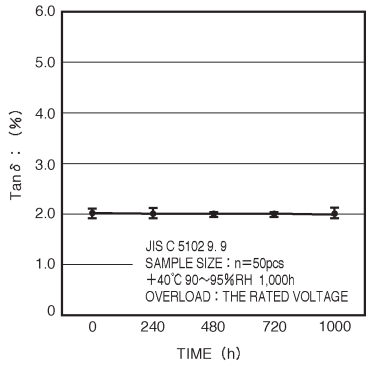

Fig.21 Tan δ

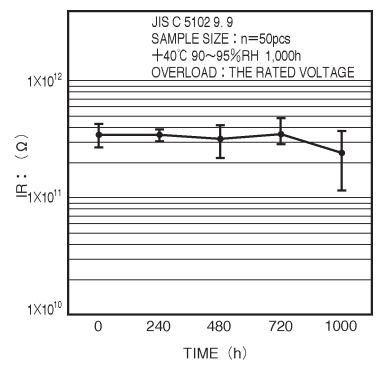

Fig.22 Insulation resistance

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