MG1RT Sea of Gates Series 0.6 Micron CMOS

Description

The MG1RT series is a 0.6 micron 3 metal layers, array based, CMOS product family offering a new frontier in integration and speed. Several arrays up to 500k cells cover all system integration needs. The MG1RT is manufactured using SCMOS 2/2 RT, a 0.6 micron drawn, radiation tolerant, 3 metal layers CMOS process.

The advanced feature size of the MG1RT translates into high performance with gate delays of 250 ps and toggle frequency of 350 MHz. Both 3V and 5V operation are possible for optimum speed/power trade off.

The MG1RT series base cell architecture provides high routability of logic with extremely dense compiled memories : ROM, RAM and DPRAM. For instance, the largest array is capable of integrating 128K bits of DPRAM with 128K bits of ROM and over 200,000 random gates.

Accurate control of clock distribution can be achieved by PLL hardware and CTS (Clock Tree Synthesis) software. New noise prevention techniques are applied in the array and in the periphery : three or more independent supplies, internal decoupling, customisation dependent supply routing, noise filtering, skew controlled I/Os, low swing differential I/Os, all contribute to improve the noise immunity and reduce the emission level.

The basic library is designed for optimum speed and area efficiency with logic synthesis software; for example, the register element is 25% smaller than in most competitors libraries. The new delay model included in the simulation libraries gives unprecedented accuracy of the pre-layout and post- layout simulations.

The high level function libraries include many common peripheral controllers and several complex circuits derived from the MHS image and network ASSPs offering.

The MG1RT is supported by an advanced software environment based on industry standards linking proprietary and commercial tools. Cadence, Mentor, Synopsys and VHDL are the reference front end tools. Floor planning associated with timing driven layout provides a short back end cycle.

The MG1RT family continues the MHS offering in array based for commercial, automotive, industrial, military and space circuits. Design compatibility with previous CMOS and BiCMOS series is assured.

Features

- Full Range of Matrices up to 480k Cells
- 0.6 µm Drawn CMOS, 3 Metal Layers, Sea of Gates
- High Integration Level : 1000k Equivalent Gates in Memory Intensive Applications
- RAM, DPRAM, FIFO Compilers
- Library Optimised for Synthesis, Floor Plan & Automatic Test Generation (ATG)
- High Speed Performances :
  – 250 ps Typical Gate Delay
  – 350 MHz Toggle Frequency
- High System Frequency Skew Control :
  – 250 MHz PLL for Clock Generation
  – Clock Tree Synthesis Software
- 3 & 5 Volts Operation; Single or Dual Supply Modes
- Low Power Consumption :
  – 0.9 µW/Gate/Mhz @3 V
  – 2.4 µW/Gate/Mhz @5 V
- Integrated Power on Reset
- Matrices With More than 500 Pads
- Versatile I/O Cell : Input, Output, I/O, Supply, Oscillator
- GTL & BTL Backplane Driver & Differential Receiver
- Configurable Drive Up To 48 mA
- ESD (4 kV) And Latch-up Protected I/O
- High Noise & EMC Immunity :
  – I/O with Slew Rate Control
  – Internal Decoupling
  – Signal Filtering between Periphery & Core
  – Application Dependent Supply Routing & Several Independent Supply Sources
- Wide Range of Packages
- Delivery in Die Form
- Advanced CAD Support : Floor Plan, Proprietary Delay Models, Timing Driven Layout, Power Management
- Cadence, Mentor & Synopsys Reference Platforms
- EDIF & VHDL Reference Formats
- Upward Compatibility With MC & MF Gate Arrays, MCM & MFM Composite Arrays.
- Available In Commercial, Industrial, Automotive, Military & Space Quality Grades

Product Outline

TYPE	TOTAL CELLS	USABLE RANDOM GATES**	USABLE MEMORY GATES**	MAXIMUM I/O ***	TOTAL PADS ****
MG1000E	798	600	1 600	24	43
MG1001E	1 566	1 100	3 100	32	51
MG1002E	2 046	1 400	4 100	36	55
MG1004E	3 608	2 500	7 200	48	67
MG1009E	8 970	6 300	17 900	72	91
MG1014E*	13 846	9 700	27 700	88	107
MG1020E	19 879	13 900	39 800	104	123
MG1033E	32 868	23 000	65 700	130	149
MG1042E*	41 869	29 300	83 700	146	165
MG1052E	51 958	36 400	103 900	162	181
MG1070E	70 059	49 000	140 100	188	207
MG1090E*	88 536	62 000	177 100	212	231
MG1120E	118 472	82 900	236 900	244	263
MG1140E*	140 049	98 000	280 000	264	283
MG1200E*	196 384	137 500	392 800	312	331
MG1265E*	264 375	185 100	528 800	360	379
MG1350E	346 203	242 300	692 400	412	431
MG1480E*	480 250	336 200	960 500	484	503

* to be used when hermetic packaged
** The maximum number of usable gates is application dependant
*** I/O pads may be configured as VDD or VSS supplies according to circuit requirements
**** This include I/O pads and dedicated pads for supply, PLL...

WARNING: MG1480E cannot be used for SCC 9000 level B or C, or MIL–STD–883 class S.

Array architecture

Core architecture

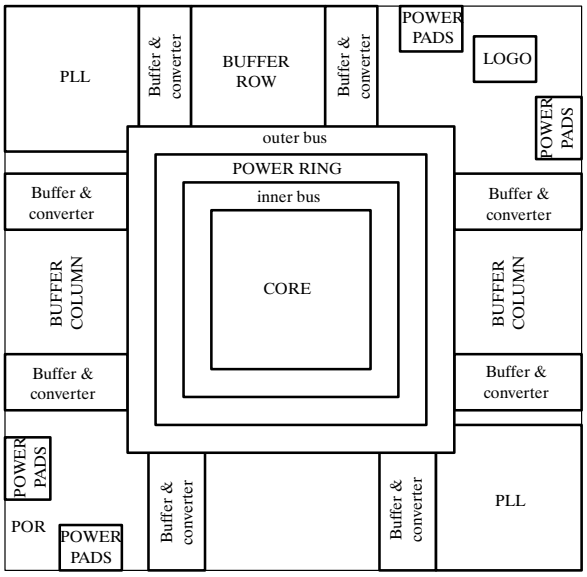
The core consists of a continuous array of logic cells without routing channels.

Each basic cell can implement a logic function such as a two input NAND gate, a memory element (one bit of RAM or DPRAM or 2 to 4 bits of ROM); a basic cell can also be a part of a more complex function such as a latch. The metallisation pattern of the logic functions mainly uses the first metal layer, this maximises routing resources for interconnections at the second and third levels of metal.

The core supply is implemented via a fixed vertical grid using the second metal layer and a layout dependent horizontal grid using the first and third metal layers.

The active core is surrounded by three busses : one interconnection bus close to the array core, one supply bus powering the core and one interconnection bus close to the periphery. The power bus consists of a VDDA ring

using the second metal layer and a VSSA ring using the third metal layer. Integrated decoupling capacitors are located below these buses.



Pad ring architecture

Each side of the die is filled with versatile I/O buffers. Two corners contains PLLs, one a power on reset and one technological devices. Corner pads can be used for PLL I/O's or buffer supplies.

Four power rings run above the buffers. The VSSN and VDDN rings supply the output drivers and the VSSQ and VDDQ rings supply the buffer logic.

The array core and buffers can have different supply voltages ; in this case the voltage difference is handled by level shifters located close to each I/O buffer. Buffers on different sides of the array can use different supply voltages.

Gate capacity

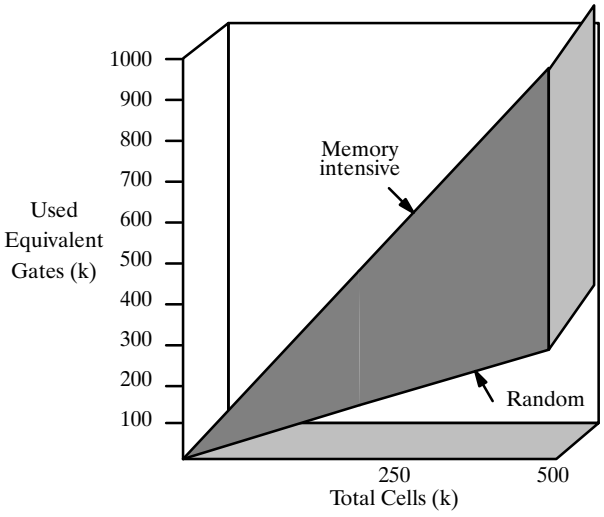
The gate utilisation is the number of equivalent used gates in a design divided by the total number of cells available in the array. The cell structure is designed to provide a gate utilisation of 70 % on average random logic designs and up to 200 % for dual port RAM.

The total number of equivalent gates used in an array is the product of gate utilisation by the total number of available cells. This value is design dependent and is influenced by several factors : complexity, operating speed and design structure.

As the cell structure is identical for each matrix of the MG1RT family, a better gate utilisation for the smaller arrays may be achieved.

Design structure is the dominant factor on gate utilisation ; indeed, as the array has limited routing resources, a higher connection/cell ration implies a lower gate utilisation. Alternatively, regular structures like memories will allow very high gate utilisation to be achieved.

The figure below summarises the relation between gate capacity and design style.



Libraries

The MG1RT cell library has been designed to take full advantage of the features offered by both logic and test synthesis tools.

Cell library

A cell is an optimised simple function having a unique metallisation pattern. Cell layout is mainly done using the first metal layer, thus freeing the second and third layers for supply and circuit interconnections.

A statistical study of several hundred designs showed that very few cells are intensively used ; therefore the design effort was focused on the optimisation of these cells rather than increasing the number of cells. The result is a library providing fast and dense designs. Storage elements (Flip-flops and latches) are available in normal and scan versions.

5 and 3 Volt libraries can be delivered.

Macros library

Macros are useful to define elements of greater complexity than cells. Macros are composed of cells or simpler macros.

A large selection of generic or 7400 functions is available : counters, decoders, adders, comparators, parity checkers... Compatibility with previous MC and MF libraries is assured at this level.

Design testability is assured by the full support of SCAN, JTAG (IEEE 1149) and BIST methodologies.

More complex macro functions are available, some of these are listed in the following table.

Communication		**µP Peripheral**	
M6402	UART	M8251	USART
M15530	Manchester coder	M8259	Interrupt controller
MI2C	Protocol controller	M8254	Timer
M6207	DPRAM controller	M82288	Bus Controller
Micro Slice		**Testability**	
M2901	ALU slice	JTAG	IEEE 1149 I/O and TAP
M2910	Sequencer	BIST	Autotest for memories

Block Generators

Block generators are used to create a customer specific simulation model and metallisation pattern for regular functions like RAM, DPRAM and FIFO. The basic cell architecture allows one bit per cell for RAM and DPRAM and 2 to 4 bits per cell for ROM. The main characteristics of these generators are summarised below.

Function	**Maximum Size (bits)**	**bits/word**	**Typical characteristics (16 k bits)**		
			access time (ns)	**consumption (mA/MHz)**	**Used cells**
RAM	72 k	1-144	8	1.6	20 k
DPRAM	72 k	1-144	8	3.3	23 k
FIFO	72 k	1-144	8	2.1	23 k

I/O buffer interfacing

I/O Fexibility

All I/O buffers may be configured as input, output, bi-directional, oscillator or supply. A level translator is located close to each buffer.

Inputs

Input buffers with CMOS or TTL thresholds are non inverting and feature versions with and without hysteresis. The CMOS and TTL input buffers may

incorporate pull-up or pull down terminators. For special purposes, a buffer allowing direct input to the matrix core is available. A differential input buffer is also available allowing resolution of data values on smal swing busses such as GTL or other proprietary solutions.

Differential input typical characteristics			
Supply (V)	**Differential voltage (mV)**	**Tphl (ns)**	**Tplh (ns)**
5	100	2,3	5,5
3	100	3,7	5,2

Outputs

Several kinds of CMOS and TTL output drivers are offered : fast buffers with 3, 6, 12 and 24 mA drive, low noise buffers with 12 mA drive. GTL and pseudo ECL bus drivers are also available.

Clock generation & PLL

Clock generation

MHS offers 4 different types of oscillators : low power 32KHz crystal oscillator, high frequency crystal oscillator and 2 RC oscillators. For all devices, the mark-space ratio is better than 40/60 and the start-up time less than 10 ms; the other characteristics are summarised below :

	Frequency (MHz)		**Typical consumption (µA)**
	Minimum	**Maximum**	
Xtal 32K	0.03	0.034	50
Xtal 50 M	2	50	1 000
RC 10M	0.02	10	600
RC 32 M	10	32	1 500

PLL

Two independent PLL devices are located in upper left and lower right corners. Each may be used for the following functions :

– Synchronisation of an internal clock on a reference system clock.

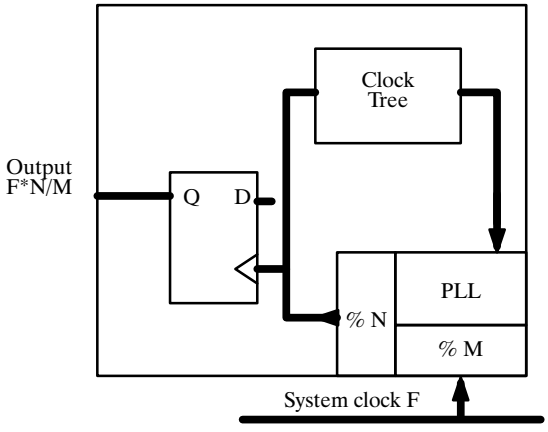
– Skew control : the internal clock transitions are synchronous with the reference clock whatever the load and the depth of logic in the clock tree.

– Frequency synthesis : two frequency dividers are included in each PLL. One divides the reference clock frequency F0 by a factor M and the other divides the internal clock frequency F by N. The internal clock frequency is :

$F = F0 * M / N$

Both M and N can take values from 1 to 16.

Typical PLL Usage



The maximum frequency at the PLL input after division by M is 70 MHz.

The maximum internal clock frequency is 250 MHz at 5 V and 150 MHz at 3 V ; the minimum frequency is 20 MHz.

Each PLL corner block has 6 dedicated pads : 2 VDD, 3 VSS and a filtering I/O connected to an RC network.

Propagation delays

Propagation delays for MG1RT cells and blocks are a function of several factors including fan out, signal slope, interconnection capacitance, supply voltage, junction temperature and processing tolerance and additionaly total irradiation dose for special operating conditions.

Propagation delays are provided for MG1RT cells under nominal conditions (Tj = 25°C, VDD = 5.0 or 3.0 V, typical process, no irradiation). Worst case values are obtained by applying derating coefficients for temperature, voltage, process and total dose irradiation : KT, KV KP and KD. These coefficients are also design dependent and in the design kits each cell has its individual set of parameters.

Worst case propagation delays can however be estimated by using the following formula and tables :

Worst case = Typical * KTmax * KVmax * KPmax (* KDmax)

Voltage	KV
4.5	1.1
5	1
5.5	0.93

Process	KP
Best	0.78
Typical	1
Worst	1.28

Voltage	KV
2.7	1.14
3	1
3.2	0.93
3.6	0.81

Temperature	KT
–55	0.74
–40	0.79
0	0.92
25	1
90	1.21
105	1.26
145	1.38

Dose (krad)	KD
0	1
50	1

Power supply & noise protection

The speed and density of the SCMOS 2/2 RT technology causes large switching current spikes for example either when :

16 high current output buffers switch simultaneously,

or

10% of the 500 000 gates are switching within a window of 1ns .

Sharp edges and high currents cause some parasitic elements in the packaging to become significant. In this frequency range, the package inductance and series resistance should be taken into account. It is known that an inductor slows down the settling time of the current and causes voltage drops on the power supply lines. These drops can affect the behaviour of the circuit itself or disturb the external application (ground bounce).

In order to improve the noise immunity of the MG core matrix, several mechanisms have been implemented inside the MG arrays. Two kinds of protection have been added : one to limit the I/O buffer switching noise and the other to protect the I/O buffers against the switching noise coming from the matrix.

I/O Buffers switching protection

Three features are implemented to limit the noise generated by the switching current :

The power supplies of the input and output buffers are separated.

The rise and fall times of the output buffers can be controlled by an internal regulator.

A design rule concerning the number of buffers connected on the same power supply line has been imposed.

Matrix switching current protection

This noise disturbance is caused by a large number of gates switching simultaneously. To allow this without impacting the functionality of the circuit, three new features have been added :

Some decoupling capacitors are integrated directly on the silicon to reduce the power supply drop.

A power supply network has been implemented in the matrix. This solution lessens the parasitic elements such as inductance and resistance and constitutes an artificial VDD and Ground plane. One mesh of the network supplies approximately 150 cells.

A low pass filter has been added between the matrix and the input to the output buffer. This limits the transmission of the noise coming from the ground or the VDD supply of the matrix to the external world via the output buffers.

Power consumption

The power consumption of an MG1RT array is due to three factors : leakage (P1), core (P2) and I/O (P3) consumption.

$P = P1 + P2 + P3$

Standby Power Consumption

The consumption due to leakage currents may be defined as :

$P1 = (VDD – VSS) * I_{CCSB} * N_{CELL}$

Where I_{CCSB} is the leakage current through a polarised basic gate and N_{CELL} is the number of used cells.

Core Power Consumption

The consumtion due to the switching of cells in the core of the matrix is bounded by :

$P2 = N_{CELL} * P_{GATE} * C_{ACTIVITY} * F$

Where N_{CELL} is the number of used cells, F the data toggling frequency is equal to half the clock frequency for random data and P_{GATE} is the power consumption per cell.

$P_{GATE} = P_{CA} + P_{CO}$

$C_{ACTIVITY}$ is the fraction of the total number of cells toggling per cycle.

Capacitance Power

$P_{CA} = C * (VDD – VSS)^2/2$

C is the total output capacitance and may be expressed as the sum of the drain capacitance of the driver, the wiring capacitance and the gate capacitance of the inputs.

Worst case value : PCA # 1.7 µW/gate/MHz @ 5 V

Commutation Power

$P_{CO} = (VDD – VSS) * I_{dsohm}$

Where I_{dsohm} is the current flowing into the driver between supply and ground during the commutation. I_{dsohm} is about 15 % of the Pmos saturation currrent.

Worst case value : Pco # 0.7 µW/gate/MHz @ 5 V

I/O Power Consumption

The power consumption due to the I/Os is :

$P3 = Ni * C_O * (VDD – VSS)^2 * Fi/2$

With Ni equals to the number of buffers running at Fi and C_O is the output capacitance.

Note:
If a signal is a clock, Fi = F, if it is a data with random values, Fi = F/4.

Power Consumption Example

Matrix	MG1RT265	
Used gates (70 %)	185 k	185 k
Voltage	5 V	3 V
Frequency	40 MHz	40 MHz
Standby Power		
Iccsb (125°C)	10 nA	10 nA
$P1 = (VDD – VSS) * I_{CCSB} * N_{CELL}$	10 mW	6 mW
Core Power		
Power Consumption per Cell	2.4 µW/Gate/MHz	0.9 µW/Gate/MHz
$C_{activity}$	20 %	20 %
$P2 = N_{CELL} * P_{GATE} * C_{activity} * F$	1776 mW	666 mW
I/O Power		
Number of Outputs and I/O Buffers	100	100
Output Capacitance	50 pF	50 pF
$P3 = Ni * C_O * (VDD – VSS)^2 * Fi/2$	625 mW	225 mW
Total Power		
P = P1 + P2 + P3	2.41 W	900 mW

Packaging

Allowed Matrice and Package Combinations

	MG1014E	MG1042E	MG1090E	MG1140E	MG1200E	MG1265E	MG1480E
MQFPL 196			Y	Y	Y	Y	Y
MQFPL 160		Y	Y	Y	Y	Y	
MQFPL 132		Y	Y	Y	Y	Y	
MQFPL 100	Y	Y	Y				
MQFPL 80	Y	Y	Y				
MQFPL 68	Y	Y					
MQFPF 352					Y	Y	Y
MQFPF 304				Y	Y	Y	Y
MQFPF 256				Y	Y	Y	Y
MQFPF 196			Y	Y	Y	Y	Y
MQFPF 172		Y	Y	Y	Y	Y	
MQFPF 160		Y	Y	Y	Y	Y	
MQFPF 132		Y	Y	Y	Y	Y	
MQFPF 100	Y	Y	Y	Y			
MQFPF 84	Y	Y	Y				
LCC 100	Y	Y	Y	Y			
LCC 84	Y	Y	Y				
LCC 68	Y	Y					
LCC 44	Y						
MQFPJ 84	Y	Y	Y				
MQFPJ 68	Y	Y					
MQFPJ 44	Y						
SB 64	Y	Y					
SB 48	Y						
SB 40	Y						

MHS offers also any product in die form (water or chip carriers).

MHS also can assist for TAB solutions.

Design flows & tools

Design Flows and modes

A generic design flow for an MG1RT array is sketched on next page.

A top down design methodology is proposed which starts with high level system description and is refined in successive design steps. At each step, structural verification is performed which includes the following tasks :

– Gate level logic simulation and comparison with high level simulation results.

– Design and test rule check.

– Power consumption analysis.

– Timing analysis (only after floor plan).

The main design steps are :

– System specification, preferably in VHDL form.

– Functional description at RTL level.

– Logic synthesis.

– Floor planning and bonding diagram generation.

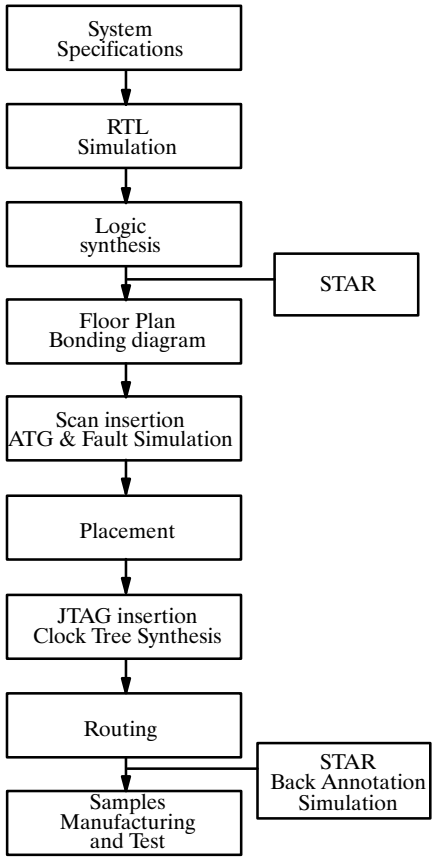
– Test insertion, ATG and/or fault simulation.

– Physical cell placement, JTAG insertion and clock tree synthesis.

– Routing

To meet the various requirements of designers, several interface levels between the customer and MHS are possible.

MG1RT Design Flow



For each of the possible design modes a review meeting is required for data transfer from the user to MHS. In all cases the final routing and verifications are performed by MHS.

The design acceptance is formalised by a design review which authorises MHS to proceed with sample manufacturing.

Design tool and design kits (DK)

The basic content of a design kit is described in the table on the right.

The interface formats to and from MHS rely on IEEE or industry standard :

– VHDL for functional descriptions

– VHDL or EDIF for netlists

– Tabular or .CAP for simulation results

– SDF (VITAL format) and SPF for backannotation

– LEF and DEF for physical floor plan information

The design kit level supported for several commercial tools is outlined in the table below.

Design Kit Support	VHDL	Gate
Cadence	*	*
Mentor	*	*
Synopsys	*	*
Compass	*	
Intergraph	*	
Viewlogic	*	

Design kit Description

Design Tool or library	MHS Software Name
Design manual & libraries	
VHDL library for blocks	
Synthesis library	
Gate level simulation library	
Design rules analyser	STAR
Power consumption analyser	COMET
Floor plan library	
Timing analyser library	
Package & bonding software	PIM
Scan path & JTAG insertion	ASIS/AJIS
ATG & fault simulation library	

Operating characteristics

Absolute Maximum Ratings

Ambient temperature under bias (TA)
Military . . . . . –55 to +125°C
Junction temperature . . . . . TJ < TA + 20°C
Storage temperature . . . . . –65 to +150°C

TTL/CMOS :
Supply voltage VDD . . . . . –0.5 V to +7 V
I/O voltage . . . . . –0.5 V to VDD + 0.5 V
Stresses above those listed may cause permanent damage to the device.

DC Characteristics

Specified at VDD = +5 V +/– 10 %

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIL	Input LOW voltage CMOS input TTL input	 0 0		 0.3 VDD 0.8	 V	
VIH	Input HIGH voltage CMOS input TTL input	 0.7 VDD 2.2		 VDD VDD	 V	
VOL	Output low voltage CMOS input TTL input			 0.1 VDD 0.4	V	IOL = –12, 6, 3 mA *
VOH	Output high voltage CMOS input TTL input	 0.9 VDD 2.4			V	IOH = +12, 6, 3 mA *
VT+	Schmitt trigger positive threshold CMOS input TTL input		 2.6 1.7	 3.2 1.9	V	
VT–	Schmitt trigger negative threshold CMOS input TTL input	 1.3 1.1	 1.4 1.2		V	
IL	Input leakage No pull up/down Pull up Pull down	 –250	 +/–1 –50 +180	 +/–5 +450	 µA µA µA	
IOZ	3-State Output Leakage current		+/–1	+/–5	µA	
IOS	Output Short circuit current IOSN IOSP			 48 36	 mA mA	VOUT = VDD VOUT = VSS
ISSDP	Leakage current per cell		0.3	1	nA	
ISSOP	Operating current per cell		0.3	0.5	µA/MHz	

* For each of the following buffers: Bout12, Bout6, Bout3

DC Characteristics

Specified at VDD = +3 V +/– 10 % or 3.3 +/– 10%

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIL	Input LOW voltage CMOS input TTL input	 0 0		 0.3 VDD 0.8	 V	
VIH	Input HIGH voltage CMOS input TTL input	 0.7 VDD 2.2		 VDD VDD	 V	
VOL	Output low voltage CMOS input TTL input			 0.1 VDD 0.4	V	IOL = –6, 3, 1.5 mA *
VOH	Output high voltage CMOS input TTL input	 0.9 VDD 2.4			V	IOH = +4, 2, 1 mA *
VT+	Schmitt trigger positive threshold CMOS input TTL input		 1.8 1.3	 2.0 1.4	 V	
VT–	Schmitt trigger negative threshold CMOS input TTL input	 0.9 0.9	 1.0 1.0		 V	
IL	Input leakage No pull up/down Pull up Pull down	 –50 –50	 –10 20	 +/–1 +100	 µA µA µA	
IOZ	3-State Output Leakage current			+/–1	µA	
IOS	Output Short circuit current IOSN IOSP			 24 12	 mA mA	VOUT = VDD VOUT = VSS
ISSDP	Leakage current per cell		0.1		nA	
ISSOP	Operating current per cell		0.2	0.3	µA/MHz	

* For each of the following buffers: Bout12, Bout6, Bout3

AC Characteristics

TJ = 25°C, Process typical (all values in ns)

Buffer	Description	Transition	Load (40 pF)	
			5V	3V
BOUT3	Output buffer with 3 mA drive	Tplh	5.04	8.88
		Tphl	6.16	9.80
BOUT12	Output buffer with 12 mA drive	Tplh	2.94*	5.10
		Tphl	2.99*	4.77
BOUTQ	Low noise output buffer with 12 mA drive	Tplh	3.57*	6.10
		Tphl	6.96*	12.10
B3STA3	3-state output buffer with 3 mA drive	Tplh	5.15	9.06
		Tphl	6.20	9.90
B3STA12	3-state output buffer with 12 mA drive	Tplh	3.09*	5.31*
		Tphl	3.02*	4.88*
B3STAQ	Low noise 3-state output buffer with 12 mA drive	Tplh	3.68*	6.40
		Tphl	7.04*	12.30

* 60 pF

	Description	Transition	FO		
BINCMOS	CMOS input buffer	Tplh	15	1.38	2.11
		Tphl		1.31	1.93
BINTTL	TTL input buffer	Tplh	16	1.55	2.27
		Tphl		1.70	1.89
INV	Inverter	Tplh	12	0.91	1.47
		Tphl		0.45	0.70
BUF4X	High drive internal buffer	Tplh	51	1.02	1.73
		Tphl		0.86	1.34
NAND2	2-Input NAND gate	Tplh	16	1.11	1.76
		Tphl		0.80	1.24
NOR2	2-Input NOR gate	Tplh	8	1.10	1.66
		Tphl		0.33	0.55
OAI22	4-input OR AND INVERT gate	Tplh	8	1.28	1.83
		Tphl		0.42	0.66
FDFF	D flip-flop, Clk to Q	Tplh	8	1.15	1.96
		Tphl		0.94	1.59
		Ts		0.50	1.20
		Th		0.10	0.23
SFF	D flip-flop with scan input, Clk to Q	Tplh	7	1.12	1.92
		Tphl		0.92	1.57
		Ts		0.78	1.88
		Th		–0.16	–0.39

Design Offering

Five different ASIC design offerings are available : ULC, Gate Arrays, Composite Arrays, Cell Based and Full Custom, each physical implementation giving an answer to the compromise : flexibility/unit price and integration/development cost.

Design Modes

Three different design modes can be agreed between Customer and MHS, depending on system and integration skills requirements.

Mode	Logic Design	Physical Layout	Design Tools
Customer Design	Customer	Customer	Customer tools
Customer and TEMIC Design	Customer	MHS	MHS supported tools (Netlist and simulation)
TEMIC Design	MHS	MHS	MHS supported tools (Netlist and simulation)

Supported tools are currently CADENCE, COMPASS, MENTOR, SYNOPSYS and VHDL/VITAL.

Design Modes versus Design Offering

Mode / Offering	Customer Design	Customer and MHS Design	MHS Design
ULC			□
Gate Array		x	□
Composite Array		x	□
Cell Based	x	○	□
Full Custom	x		

x : standard offer.
○ : depending on human and hardware ressources needed and/or available.
□ : specific development using MHS own expertise.

Design Phases and Meetings

The design of a circuit is separated into four main phases, separated by three major meetings between MHS and the Customer, as shown in Figure 1.

The design phases and meetings.