FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-50103-2E

MCP (Multi-Chip Package) FLASH MEMORY & SRAM

CMOS

16M (× 8) FLASH MEMORY & 2M (× 8) STATIC RAM

MB84VA2100-10/MB84VA2101-10

■ FEATURES

- **Power supply voltage of 2.7 to 3.6 V**
- **High performance**
  100 ns maximum access time
- **Operating Temperature**
  –20 to +85°C

— FLASH MEMORY

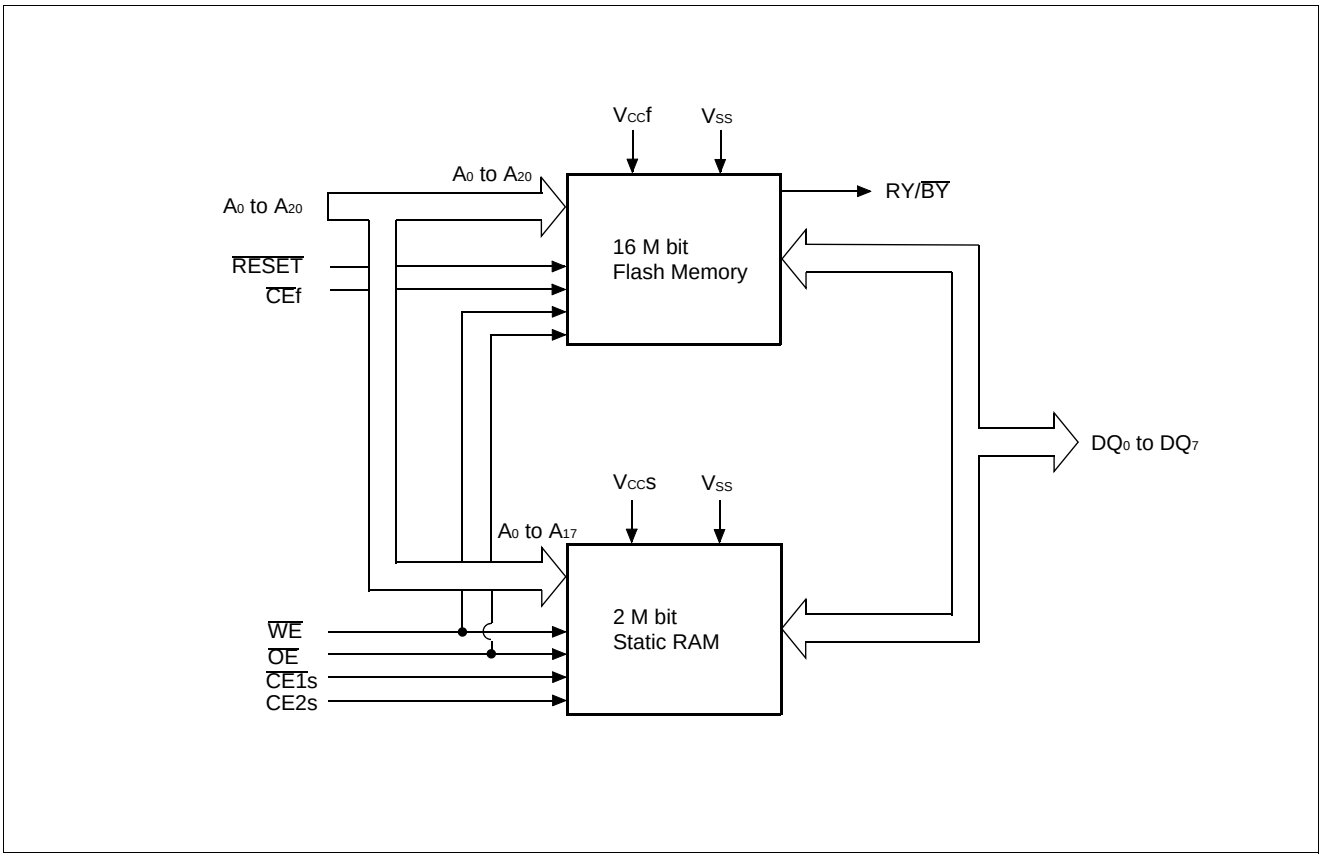
- **Minimum 100,000 write/erase cycles**
- **Sector erase architecture**
  One 16 K byte, two 8 K bytes, one 32 K byte, and thirty one 64 K bytes.
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Boot Code Sector Architecture**
  MB84VA2100: Top sector
  MB84VA2101: Bottom sector
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready-Busy output (RY/$\overline{\text{BY}}$)**
  Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
  When addresses remain stable, automatically switch themselves to low power mode.
- **Low V_{CC} write inhibit ≤ 2.5 V**
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read in another sector within the same device
  Please refer to "MBM29LV160T/B" data sheet in detailed function

— SRAM

- **Power dissipation**
  Operating : 35 mA max.
  Standby : 50 µA max.
- **Power down features using $\overline{\text{CE1}}$s and CE2s**
- **Data retention supply voltage: 2.0 V to 3.6 V**

MB84VA2100-10/MB84VA2101-10

■ BLOCK DIAGRAM



■ PIN ASSIGNMENTS

(Top View)

	A	B	C	D	E	F	G	H
6	$\overline{CE1}$s	V_{SS}	DQ_1	A_1	A_2	A_4	CE2s	A_9
5	A_{10}	DQ_5	DQ_2	A_0	A_3	A_7	RY/$\overline{BY}$	A_{15}
4	$\overline{OE}$	DQ_7	DQ_4	DQ_0	A_6	A_{19}	$\overline{RESET}$	A_{16}
3	A_{11}	A_8	A_5	N.C.	DQ_3	N.C.	A_{13}	A_{20}
2	A_{14}	A_{18}	N.C.	$\overline{CE}$f	N.C.	V_{CC}f	DQ_6	A_{12}
1	$\overline{WE}$	V_{CC}s	A_{17}	V_{SS}	N.C.	N.C.	N.C.	N.C.

Table 1 Pin Configuration

Pin	Function	Input/ Output
A_0 to A_{17}	Address Inputs (Common)	I
A_{18} to A_{20}	Address Input (Flash)	I
DQ_0 to DQ_7	Data Inputs/Outputs (Common)	I/O
$\overline{CE}$f	Chip Enable (Flash)	I
$\overline{CE1}$s	Chip Enable (SRAM)	I
CE2s	Chip Enable (SRAM)	I
$\overline{OE}$	Output Enable (Common)	I
$\overline{WE}$	Write Enable (Common)	I
RY/$\overline{BY}$	Ready/Busy Outputs (Flash)	O
$\overline{RESET}$	Hardware Reset Pin/Sector Protection Unlock (Flash)	I
N.C.	No Internal Connection	—
V_{SS}	Device Ground (Common)	Power
V_{CC}f	Device Power Supply (Flash)	Power
V_{CC}s	Device Power Supply (SRAM)	Power

MB84VA2100-10/MB84VA2101-10

■ PRODUCT LINE UP

		Flash Memory	SRAM
Ordering Part No.	V_{CC} = 3.0 V $^{+0.6\ V}_{-0.3\ V}$	MB84VA2100-10/MB84VA2101-10	
Max. Address Access Time (ns)		100	100
Max. $\overline{CE}$ Access Time (ns)		100	100
Max. $\overline{OE}$ Access Time (ns)		40	50

■ BUS OPERATIONS

Table 2 User Bus Operations

Operation (1), (3)	$\overline{CEf}$	$\overline{CE1s}$	CE2s	$\overline{OE}$	$\overline{WE}$	DQ_0 to DQ_7	$\overline{RESET}$
Full Standby	H	H	X	X	X	HIGH-Z	H
		X	L				
Output Disable	X	X	X	H	H	HIGH-Z	H
Read from Flash (2)	L	H	X	L	H	D_{OUT}	H
		X	L				
Write to Flash	L	H	X	H	L	D_{IN}	H
		X	L				
Read from SRAM	H	L	H	L	H	D_{OUT}	H
Write to SRAM	H	L	H	X	L	D_{IN}	H
Flash Hardware Reset	X	H	X	X	X	HIGH-Z	L
		X	L				

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

Notes: 1. Other operations except for indicated this column are inhibited.
2. $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.
3. Do not apply $\overline{CEf}$ = V_{IL}, $\overline{CE1s}$ = V_{IL} and CE2s = V_{IH} at a time.

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE on FLASH MEMORY

- One 16 K byte, two 8 K bytes, one 32 K byte, and thirty one 64 K bytes.

  Individual-sector, multiple-sector, or bulk-erase capability.

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Sector Size	Address Range
64 Kbytes	00000H to 0FFFFH
64 Kbytes	10000H to 1FFFFH
64 Kbytes	20000H to 2FFFFH
64 Kbytes	30000H to 3FFFFH
64 Kbytes	40000H to 4FFFFH
64 Kbytes	50000H to 5FFFFH
64 Kbytes	60000H to 6FFFFH
64 Kbytes	70000H to 7FFFFH
64 Kbytes	80000H to 8FFFFH
64 Kbytes	90000H to 9FFFFH
64 Kbytes	A0000H to AFFFFH
64 Kbytes	B0000H to BFFFFH
64 Kbytes	C0000H to CFFFFH
64 Kbytes	D0000H to DFFFFH
64 Kbytes	E0000H to EFFFFH
64 Kbytes	F0000H to FFFFFH
64 Kbytes	100000H to 10FFFFH
64 Kbytes	110000H to 11FFFFH
64 Kbytes	120000H to 12FFFFH
64 Kbytes	130000H to 13FFFFH
64 Kbytes	140000H to 14FFFFH
64 Kbytes	150000H to 15FFFFH
64 Kbytes	160000H to 16FFFFH
64 Kbytes	170000H to 17FFFFH
64 Kbytes	180000H to 18FFFFH
64 Kbytes	190000H to 19FFFFH
64 Kbytes	1A0000H to 1AFFFFH
64 Kbytes	1B0000H to 1BFFFFH
64 Kbytes	1C0000H to 1CFFFFH
64 Kbytes	1D0000H to 1DFFFFH
64 Kbytes	1E0000H to 1EFFFFH
32 Kbytes	1F0000H to 1F7FFFH
8 Kbytes	1F8000H to 1F9FFFH
8 Kbytes	1FA000H to 1FBFFFH
16 Kbytes	1FC000H to 1FFFFFH

MB84VA2100 Sector Architecture

Sector Size	Address Range
16 Kbytes	00000H to 03FFFH
8 Kbytes	04000H to 05FFFH
8 Kbytes	06000H to 07FFFH
32 Kbytes	08000H to 0FFFFH
64 Kbytes	10000H to 1FFFFH
64 Kbytes	20000H to 2FFFFH
64 Kbytes	30000H to 3FFFFH
64 Kbytes	40000H to 4FFFFH
64 Kbytes	50000H to 5FFFFH
64 Kbytes	60000H to 6FFFFH
64 Kbytes	70000H to 7FFFFH
64 Kbytes	80000H to 8FFFFH
64 Kbytes	90000H to 9FFFFH
64 Kbytes	A0000H to AFFFFH
64 Kbytes	B0000H to BFFFFH
64 Kbytes	C0000H to CFFFFH
64 Kbytes	D0000H to DFFFFH
64 Kbytes	E0000H to EFFFFH
64 Kbytes	F0000H to FFFFFH
64 Kbytes	100000H to 10FFFFH
64 Kbytes	110000H to 11FFFFH
64 Kbytes	120000H to 12FFFFH
64 Kbytes	130000H to 13FFFFH
64 Kbytes	140000H to 14FFFFH
64 Kbytes	150000H to 15FFFFH
64 Kbytes	160000H to 16FFFFH
64 Kbytes	170000H to 17FFFFH
64 Kbytes	180000H to 18FFFFH
64 Kbytes	190000H to 19FFFFH
64 Kbytes	1A0000H to 1AFFFFH
64 Kbytes	1B0000H to 1BFFFFH
64 Kbytes	1C0000H to 1CFFFFH
64 Kbytes	1D0000H to 1DFFFFH
64 Kbytes	1E0000H to 1EFFFFH
64 Kbytes	1F0000H to 1FFFFFH

MB84VA2101 Sector Architecture

Table 3 Sector Address Tables (MB84VA2100)

Sector Address	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	Address Range
SA0	0	0	0	0	0	X	X	X	00000H to 0FFFFH
SA1	0	0	0	0	1	X	X	X	10000H to 1FFFFH
SA2	0	0	0	1	0	X	X	X	20000H to 2FFFFH
SA3	0	0	0	1	1	X	X	X	30000H to 3FFFFH
SA4	0	0	1	0	0	X	X	X	40000H to 4FFFFH
SA5	0	0	1	0	1	X	X	X	50000H to 5FFFFH
SA6	0	0	1	1	0	X	X	X	60000H to 6FFFFH
SA7	0	0	1	1	1	X	X	X	70000H to 7FFFFH
SA8	0	1	0	0	0	X	X	X	80000H to 8FFFFH
SA9	0	1	0	0	1	X	X	X	90000H to 9FFFFH
SA10	0	1	0	1	0	X	X	X	A0000H to AFFFFH
SA11	0	1	0	1	1	X	X	X	B0000H to BFFFFH
SA12	0	1	1	0	0	X	X	X	C0000H to CFFFFH
SA13	0	1	1	0	1	X	X	X	D0000H to DFFFFH
SA14	0	1	1	1	0	X	X	X	E0000H to EFFFFH
SA15	0	1	1	1	1	X	X	X	F0000H to FFFFFH
SA16	1	0	0	0	0	X	X	X	100000H to 10FFFFH
SA17	1	0	0	0	1	X	X	X	110000H to 11FFFFH
SA18	1	0	0	1	0	X	X	X	120000H to 12FFFFH
SA19	1	0	0	1	1	X	X	X	130000H to 13FFFFH
SA20	1	0	1	0	0	X	X	X	140000H to 14FFFFH
SA21	1	0	1	0	1	X	X	X	150000H to 15FFFFH
SA22	1	0	1	1	0	X	X	X	160000H to 16FFFFH
SA23	1	0	1	1	1	X	X	X	170000H to 17FFFFH
SA24	1	1	0	0	0	X	X	X	180000H to 18FFFFH
SA25	1	1	0	0	1	X	X	X	190000H to 19FFFFH
SA26	1	1	0	1	0	X	X	X	1A0000H to 1AFFFFH
SA27	1	1	0	1	1	X	X	X	1B0000H to 1BFFFFH
SA28	1	1	1	0	0	X	X	X	1C0000H to 1CFFFFH
SA29	1	1	1	0	1	X	X	X	1D0000H to 1DFFFFH
SA30	1	1	1	1	0	X	X	X	1E0000H to 1EFFFFH
SA31	1	1	1	1	1	0	X	X	1F0000H to 1F7FFFH
SA32	1	1	1	1	1	1	0	0	1F8000H to 1F9FFFH
SA33	1	1	1	1	1	1	0	1	1FA000H to 1FBFFFH
SA34	1	1	1	1	1	1	1	X	1FC000H to 1FFFFFH

Table 4 Sector Address Tables (MB84VA2101)

Sector Address	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	Address Range
SA0	0	0	0	0	0	0	0	X	00000H to 03FFFH
SA1	0	0	0	0	0	0	1	0	04000H to 05FFFH
SA2	0	0	0	0	0	0	1	1	06000H to 07FFFH
SA3	0	0	0	0	0	1	0	X	08000H to 0FFFFH
SA4	0	0	0	0	1	X	X	X	10000H to 1FFFFH
SA5	0	0	0	1	0	X	X	X	20000H to 2FFFFH
SA6	0	0	0	1	1	X	X	X	30000H to 3FFFFH
SA7	0	0	1	0	0	X	X	X	40000H to 4FFFFH
SA8	0	0	1	0	1	X	X	X	50000H to 5FFFFH
SA9	0	0	1	1	0	X	X	X	60000H to 6FFFFH
SA10	0	0	1	1	1	X	X	X	70000H to 7FFFFH
SA11	0	1	0	0	0	X	X	X	80000H to 8FFFFH
SA12	0	1	0	0	1	X	X	X	90000H to 9FFFFH
SA13	0	1	0	1	0	X	X	X	A0000H to AFFFFH
SA14	0	1	0	1	1	X	X	X	B0000H to BFFFFH
SA15	0	1	1	0	0	X	X	X	C0000H to CFFFFH
SA16	0	1	1	0	1	X	X	X	D0000H to DFFFFH
SA17	0	1	1	1	0	X	X	X	E0000H to EFFFFH
SA18	0	1	1	1	1	X	X	X	F0000H to FFFFFH
SA19	1	0	0	0	0	X	X	X	100000H to 10FFFFH
SA20	1	0	0	0	1	X	X	X	110000H to 11FFFFH
SA21	1	0	0	1	0	X	X	X	120000H to 12FFFFH
SA22	1	0	0	1	1	X	X	X	130000H to 13FFFFH
SA23	1	0	1	0	0	X	X	X	140000H to 14FFFFH
SA24	1	0	1	0	1	X	X	X	150000H to 15FFFFH
SA25	1	0	1	1	0	X	X	X	160000H to 16FFFFH
SA26	1	0	1	1	1	X	X	X	170000H to 17FFFFH
SA27	1	1	0	0	0	X	X	X	180000H to 18FFFFH
SA28	1	1	0	0	1	X	X	X	190000H to 19FFFFH
SA29	1	1	0	1	0	X	X	X	1A0000H to 1AFFFFH
SA30	1	1	0	1	1	X	X	X	1B0000H to 1BFFFFH
SA31	1	1	1	0	0	X	X	X	1C0000H to 1CFFFFH
SA32	1	1	1	0	1	X	X	X	1D0000H to 1DFFFFH
SA33	1	1	1	1	0	X	X	X	1E0000H to 1EFFFFH
SA34	1	1	1	1	1	X	X	X	1F0000H to 1FFFFFH

Table 5. 1 Flash Memory Autoselect Code

Type		A_{12}	A_6	A_1	A_0	Code (HEX)
Manufacturer's Code		V_{IL}	V_{IL}	V_{IL}	V_{IL}	04H
Device Code	MB84VA2100	V_{IL}	V_{IL}	V_{IL}	V_{IH}	C4H
	MB84VA2101	V_{IL}	V_{IL}	V_{IL}	V_{IH}	49H

Table 5. 2 Expanded Autoselect Code Table

Type		Code	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer's Code		04H	0	0	0	0	0	1	0	0
Device Code	MB84VA2100	C4H	1	1	0	0	0	1	0	0
	MB84VA2101	49H	0	1	0	0	1	0	0	1

Table 6 Flash Memory Command Definitions

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	1	XXXH	F0H	—	—	—	—	—	—	—	—	—	—
Read/Reset	3	555H	AAH	2AAH	55H	555H	F0H	RA	RD	—	—	—	—
Autoselect	3	555H	AAH	2AAH	55H	555H	90H	—	—	—	—	—	—
Program	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD	—	—	—	—
Chip Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Sector Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
Sector Erase Suspend	Erase can be suspended during sector erase with Addr ("H" or "L"). Data (B0H)												
Sector Erase Resume	Erase can be resumed after suspend with Addr ("H" or "L"). Data (30H)												
Set to Fast Mode	3	555H	AAH	2AAH	55H	555H	20H	—	—	—	—	—	—
Fast Program (Note)	2	XXXH	A0H	PA	PD	—	—	—	—	—	—	—	—
Reset from Fast Mode (Note)	2	XXXH	90H	XXXH	F0H	—	—	—	—	—	—	—	—
Extended Sector Protect	4	XXXH	60H	SPA	60H	SPA	40H	SPA	SD	—	—	—	—

Address bits A_{11} to A_{20} = X = "H" or "L" for all address commands except for Program Address (PA) and Sector Address (SA).
Bus operations are defined in Table 2.
Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

RA =Address of the memory location to be read.
PA =Address of the memory location to be programmed. Addresses are latched on the falling edge of the write pulse.
SA =Address of the sector to be erased. The combination of A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, and A_{13} will uniquely select any sector.
RD =Data read from location RA during read operation.
PD =Data to be programmed at location PA.
SPA =Sector address to be protected. Set sector address (SA) and (A_6, A_1, A_0) = (0, 1, 0).
SD =Sector protection verify data. Output 01H at protected sector addresses and output 00H at unprotected sector addresses.

Note: This command is valid while Fast Mode.

■ ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–55°C to +125°C
Ambient Temperature with Power Applied	–25°C to +85°C
Voltage with Respect to Ground All pins (Note)	–0.3 V to $V_{CC}f$ +0.5 V
	–0.3 V to $V_{CC}s$ +0.5 V
$V_{CC}f$/$V_{CC}s$ Supply (Note)	–0.3 V to +4.6 V

Note: Minimum DC voltage on input or I/O pins are –0.5 V. During voltage transitions, inputs may negativeovershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins are $V_{CC}f$ +0.5 V or $V_{CC}s$ +0.5 V. During voltage transitions, outputs may positive overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum rating conditions. Do not exceed these ratings.

■ RECOMMENDED OPERATING RANGES

Commercial Devices

Ambient Temperature (T_A)	–20°C to +85°C
$V_{CC}f$/$V_{CC}s$ Supply Voltages	+2.7 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ DC CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	—			–1.0	—	+1.0	µA
I_{LO}	Output Leakage Current	—			–1.0	—	+1.0	µA
$I_{CC1}f$	Flash V_{CC} Active Current (Read)	V_{CCf} = V_{CC} Max., $\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}		t_{CYCLE} = 10 MHz	—	—	30	mA
				t_{CYCLE} = 5 MHz	—	—	15	
$I_{CC2}f$	Flash V_{CC} Active Current (Program/Erase)	V_{CCf} = V_{CC} Max., $\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}			—	—	35	mA
$I_{CC1}s$	SRAM V_{CC} Active Current	V_{CCs} = V_{CC} Max., $\overline{CE1}s$ = V_{IL}, CE2s = V_{IH}		ttCYCLE =10 MHz	—	—	40	mA
				t_{CYCLE} = 1 MHz	—	—	12	mA
$I_{CC2}s$	SRAM V_{CC} Active Current	$\overline{CE1}s$ = 0.2 V, CE2s = V_{CCs} – 0.2 V, $\overline{WE}$ = V_{CCs} – 0.2 V		t_{CYCLE} = 10 MHz	—	—	35	mA
				t_{CYCLE} = 1 MHz	—	—	6	mA
$I_{SB1}f$	Flash V_{CC} Standby Current	V_{CCf} = V_{CC} Max., $\overline{CE}f$ = V_{CCf} ± 0.3 V, $\overline{RESET}$ = V_{CCf} ± 0.3 V			—	—	5	µA
$I_{SB2}f$	Flash V_{CC} Standby Current ($\overline{RESET}$)	V_{CCf} = V_{CC} Max., $\overline{RESET}$ = V_{SS} ± 0.3 V			—	—	5	µA
$I_{SB1}s$	SRAM V_{CC} Standby Current	$\overline{CE1}s$ = V_{IH} or CE2s = V_{IL}			—	—	2	mA
$I_{SB2}s$**	SRAM V_{CC} Standby Current	$\overline{CE1}s$ = V_{CC} – 0.2 V or CE2s = 0.2 V	V_{CCs} = 3.0 V ±10%	T_A = 25°C	—	1	2.5	µA
				T_A = –20 to +85°C	—	—	55	µA
			V_{CCs} = 3.3 V ±0.3 V	T_A = 25°C	—	1.5	3	µA
				T_A = –20 to +85°C	—	—	60	µA
			V_{CCs} = 3.0 V	T_A = 25°C	—	1	2	µA
				T_A = –20 to +40°C	—	—	5	µA
				T_A = –20 to +85°C	—	—	50	µA
V_{IL}	Input Low Level	—			–0.3	—	0.6	V
V_{IH}	Input High Level	—			2.2	—	V_{CC}+0.3*	V
V_{OL}	Output Low Voltage Level	I_{OL} = 2.1 mA, V_{CCf} = V_{CCs} = V_{CC} Min.			—	—	0.4	V
V_{OH}	Output High Voltage Level	I_{OH} = –500 µA, V_{CCf} = V_{CCs} = V_{CC} Min.			V_{CC} – 0.5	—	—	V
V_{LKO}	Flash Low V_{CC} Lock-Out Voltage	—			2.3	—	2.5	V

* : V_{CC} indicate lower of V_{CCf} or V_{CCs}

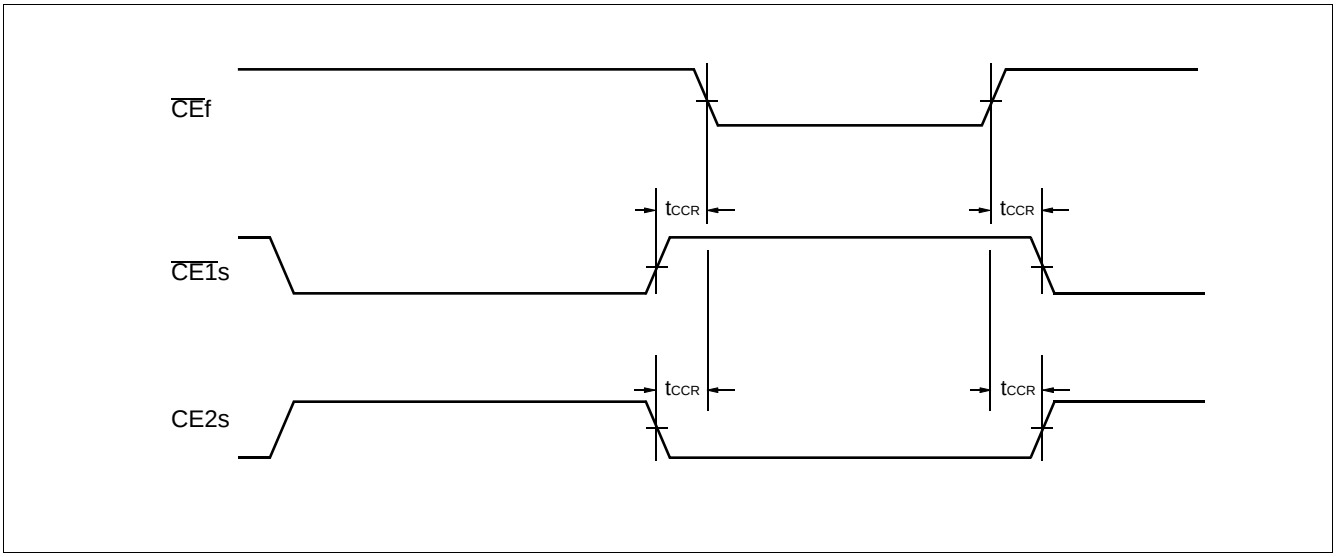
** :During standby mode with $\overline{CE1}s$ = V_{CCS} – 0.2 V, CE2s should be CE2s < 0.2V or CE2s > V_{CCS} – 0.2V

■ AC CHARACTERISTICS

- **$\overline{CE}$ Timing**

Parameter Symbols		Description	Test Setup		-10	Unit
JEDEC	Standard					
—	t_{CCR}	$\overline{CE}$ Recover Time	—	Min.	0	ns

- **Timing Diagram for alternating SRAM to Flash**



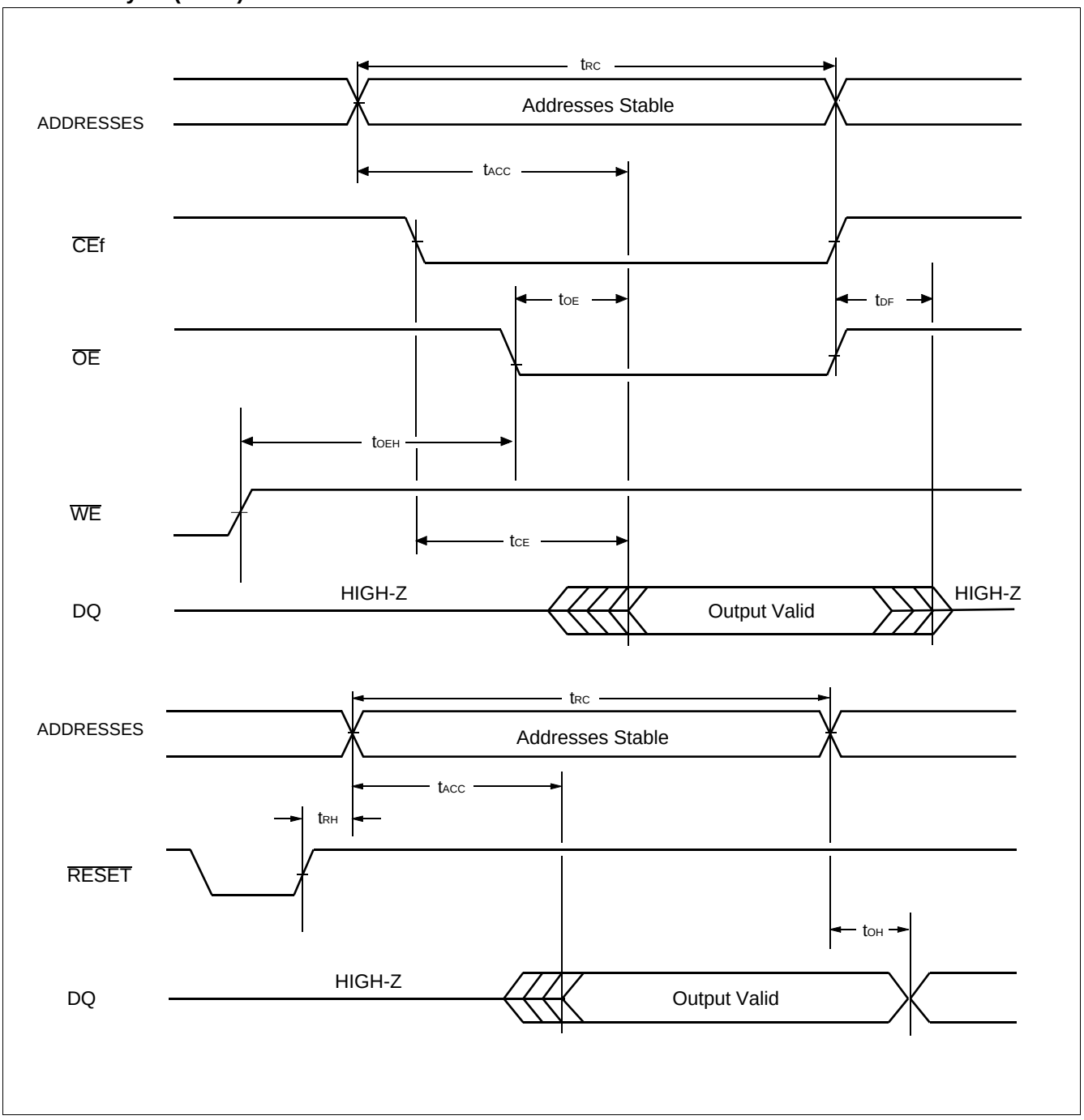
- **Read Only Operations Characteristics (Flash)**

Parameter Symbols		Description	Test Setup	-10 (Note)		Unit
JEDEC	Standard			Min.	Max.	
t_{AVAV}	t_{RC}	Read Cycle Time	—	100	—	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}f = V_{IL}$ $\overline{OE} = V_{IL}$	—	100	ns
t_{ELQV}	$t_{CE}f$	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	—	100	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	—	—	40	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z	—	—	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z	—	—	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}f$ or $\overline{OE}$, Whichever Occurs First	—	0	—	ns
—	t_{READY}	$\overline{RESET}$ Pin Low to Read Mode	—	—	20	µs

Note: Test Conditions–Output Load: 1 TTL gate and 30 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to 3.0 V
Timing measurement reference level
Input: 1.5 V
Output: 1.5 V

MB84VA2100-10/MB84VA2101-10

- **Read Cycle (Flash)**



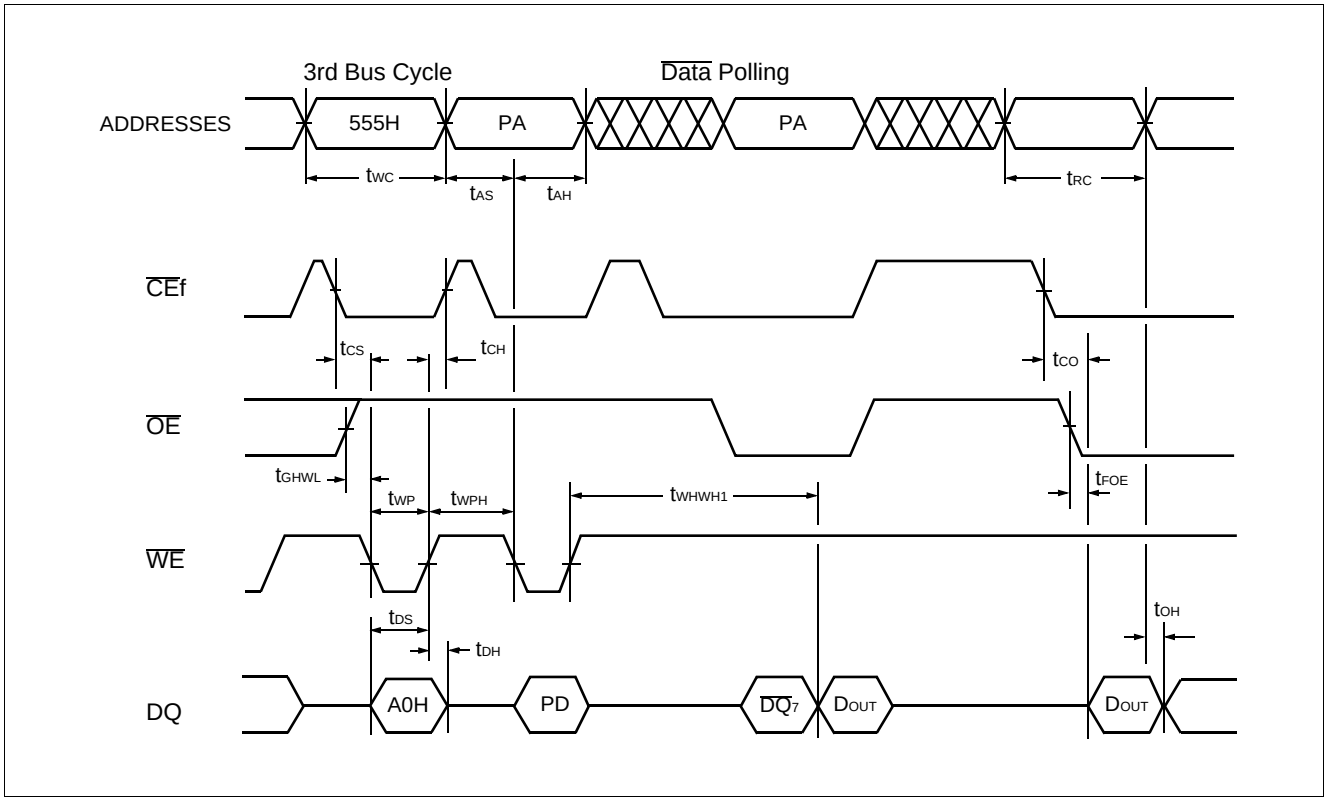
• **Erase/Program Operations (Flash)**

Parameter Symbols		Description		-10			Unit
JEDEC	Standard			Min.	Typ.	Max.	
t_{AVAV}	t_{WC}	Write Cycle Time		100	—	—	ns
t_{AVWL}	t_{AS}	Address Setup Time ($\overline{WE}$ to Addr.)		0	—	—	ns
t_{AVEL}	t_{AS}	Address Setup Time ($\overline{CE}$f to Addr.)		0	—	—	ns
t_{WLAX}	t_{AH}	Address Hold Time ($\overline{WE}$ to Addr.)		50	—	—	ns
t_{ELAX}	t_{AH}	Address Hold Time ($\overline{CE}$f to Addr.)		50	—	—	ns
t_{DVWH}	t_{DS}	Data Setup Time		50	—	—	ns
t_{WHDX}	t_{DH}	Data Hold Time		0	—	—	ns
—	t_{OES}	Output Enable Setup Time		0	—	—	ns
—	t_{OEH}	Output Enable Hold Time	Read	0	—	—	ns
			Toggle and $\overline{Data}$ Polling	10	—	—	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write ($\overline{OE}$ to $\overline{CE}$f)		0	—	—	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write ($\overline{OE}$ to $\overline{WE}$)		0	—	—	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time ($\overline{CE}$f to $\overline{WE}$)		0	—	—	ns
t_{ELWL}	t_{CS}	$\overline{CE}$f Setup Time ($\overline{WE}$ to $\overline{CE}$f)		0	—	—	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time ($\overline{CE}$f to $\overline{WE}$)		0	—	—	ns
t_{WHEH}	t_{CH}	$\overline{CE}$f Hold Time ($\overline{WE}$ to $\overline{CE}$f)		0	—	—	ns
t_{WLWH}	t_{WP}	Write Pulse Width		50	—	—	ns
t_{ELEH}	t_{CP}	$\overline{CE}$f Pulse Width		50	—	—	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		30	—	—	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$f Pulse Width High		30	—	—	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		—	8	—	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)		—	1	—	sec
				—	—	15	sec
—	t_{VCS}	V_{CC}f Setup Time		50	—	—	µs
—	t_{VLHT}	Voltage Transition Time (Note 2)		4	—	—	µs
—	t_{VIDR}	Rise Time to V_{ID} (Note 2)		500	—	—	ns
—	t_{RB}	Recover Time from RY/$\overline{BY}$		0	—	—	ns
—	t_{RP}	$\overline{RESET}$ Pulse Width		500	—	—	ns
—	t_{RH}	$\overline{RESET}$ Hold Time Before Read		200	—	—	ns
—	t_{EOE}	Delay Time from Embedded Output Enable		—	—	100	ns
—	t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay		—	—	90	ns

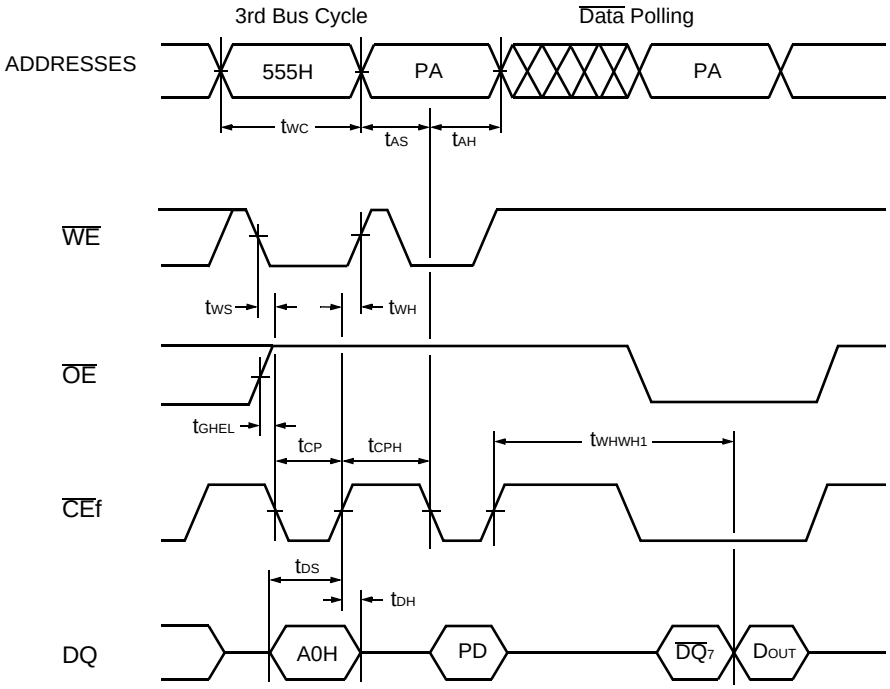
Note : 1. This does not include the preprogramming time.

2. This timing is for Sector Protection Operation.

- **Write Cycle ($\overline{WE}$ control) (Flash)**

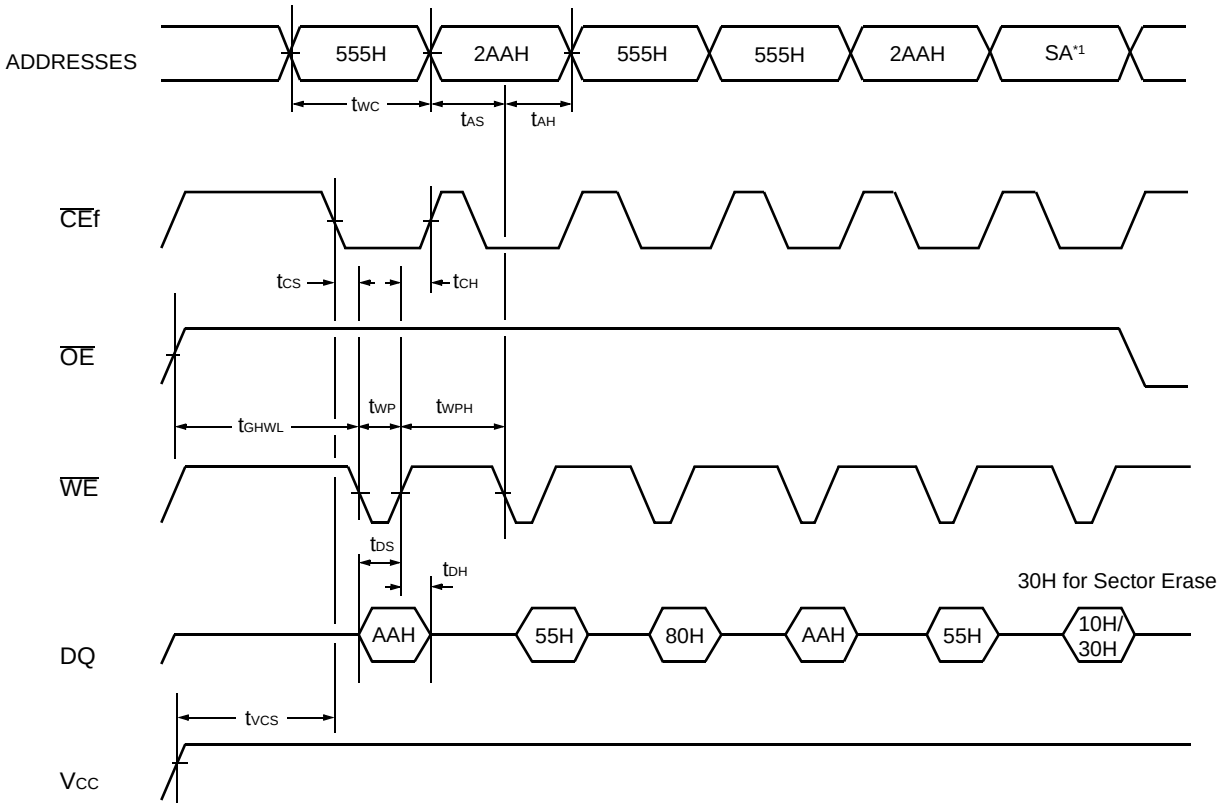


- **Write Cycle ($\overline{CE}$f control) (Flash)**



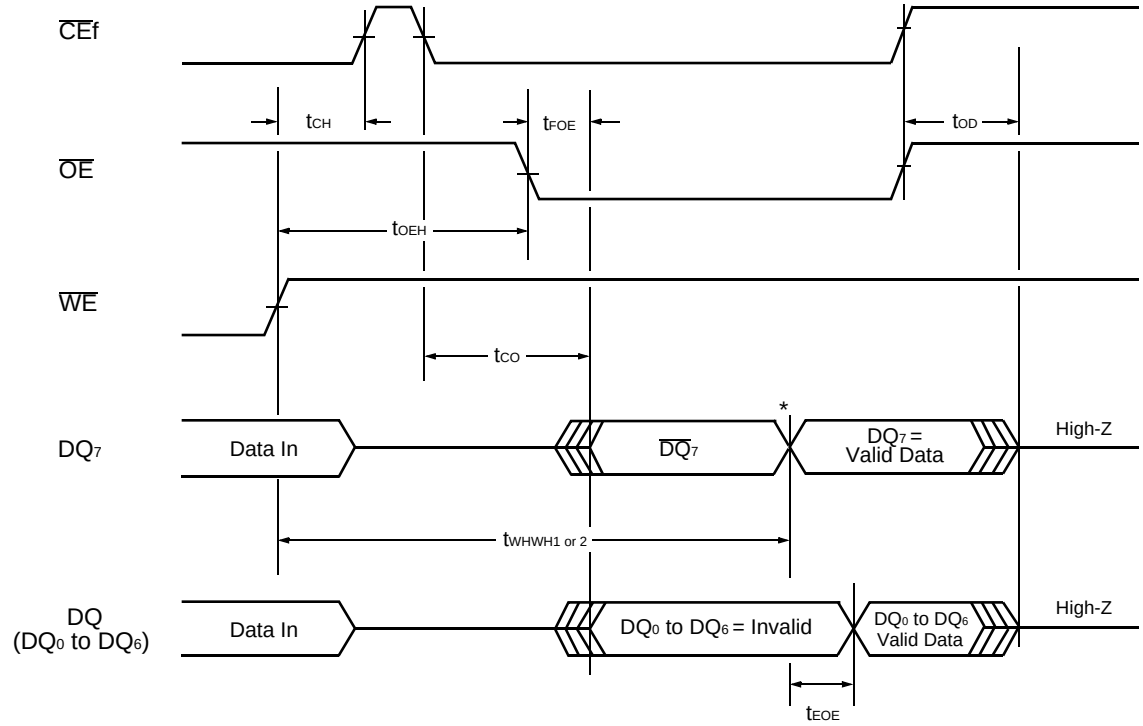
Notes: 1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ}_7$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.

- **AC Waveforms Chip/Sector Erase Operations (Flash)**



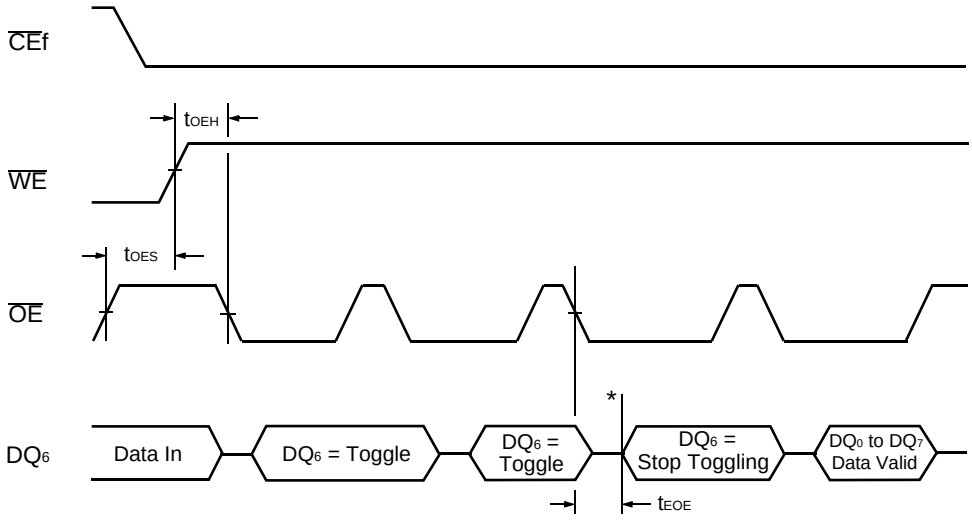
Note: 1. SA is the sector address for Sector Erase. Addresses = 555H for Chip Erase.

- **AC Waveforms for $\overline{\text{Data}}$ Polling during Embedded Algorithm Operations (Flash)**



*DQ_7 = Valid Data (The device has completed the Embedded operation.)

- **AC Waveforms for Taggle Bit during Embedded Algorithm Operations (Flash)**



*DQ_6 = Stops toggling. (The device has completed the Embedded operation.)

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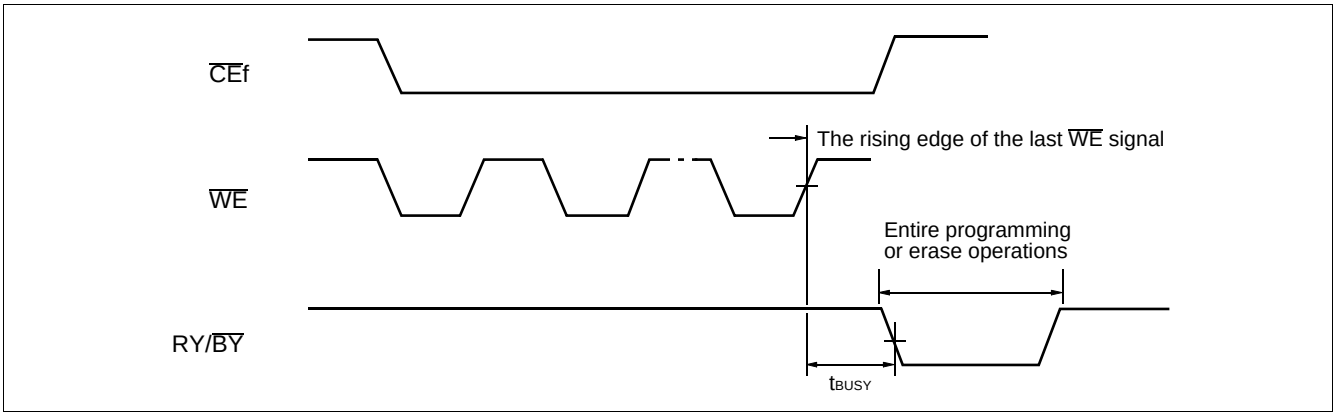
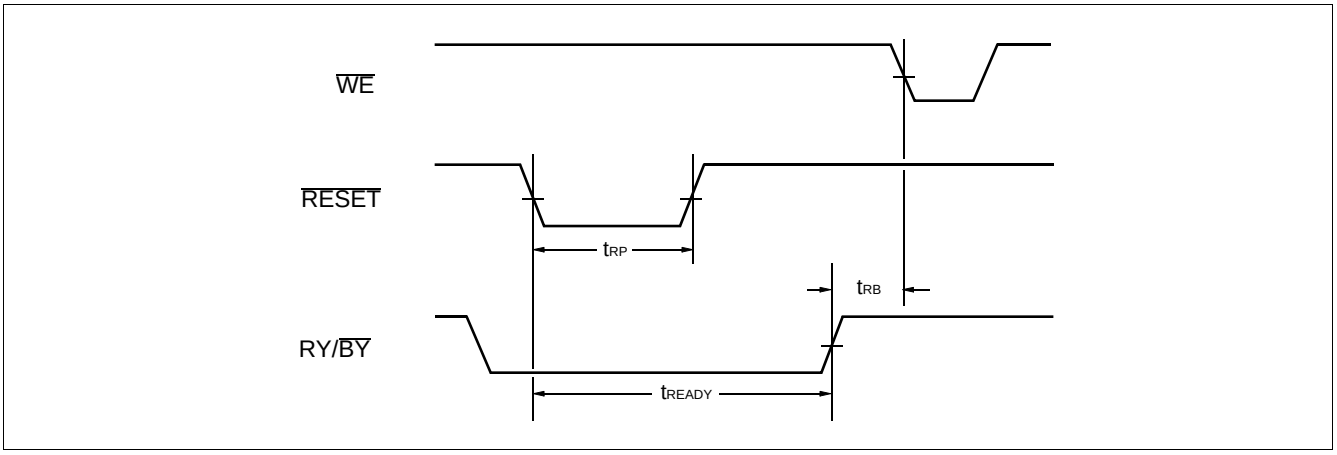
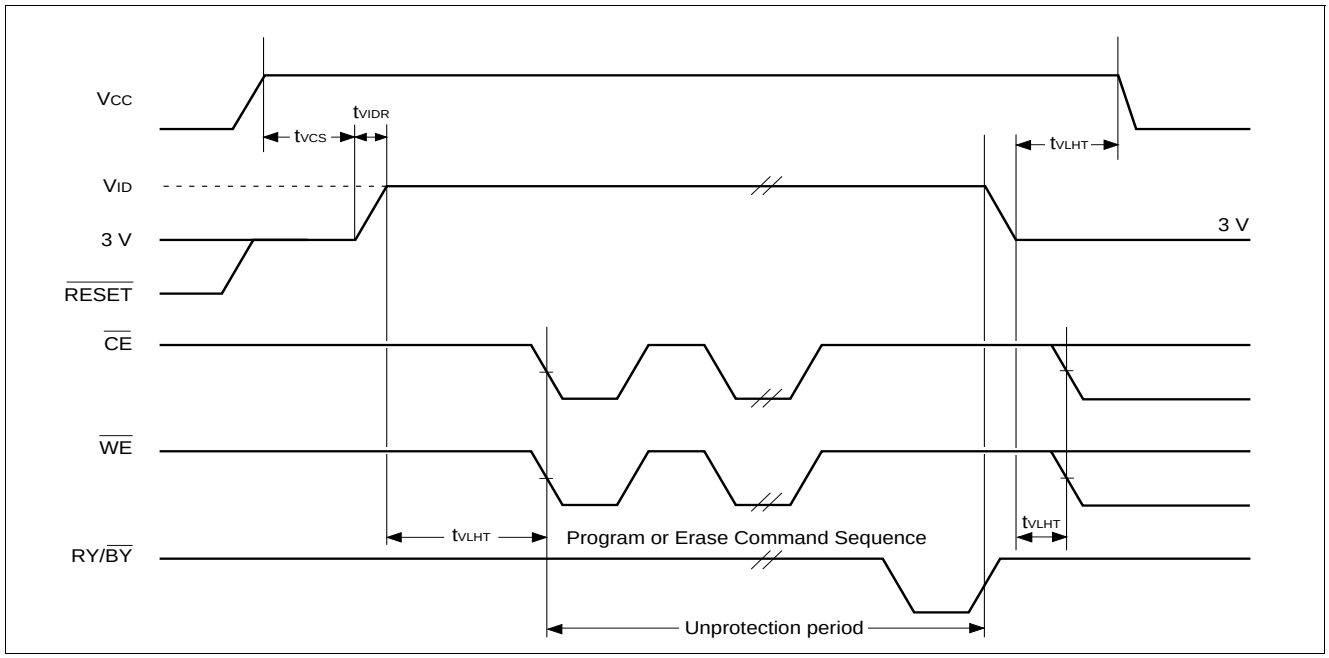
- **RY/$\overline{BY}$ Timing Diagram during Write/Erase Operations (Flash)**



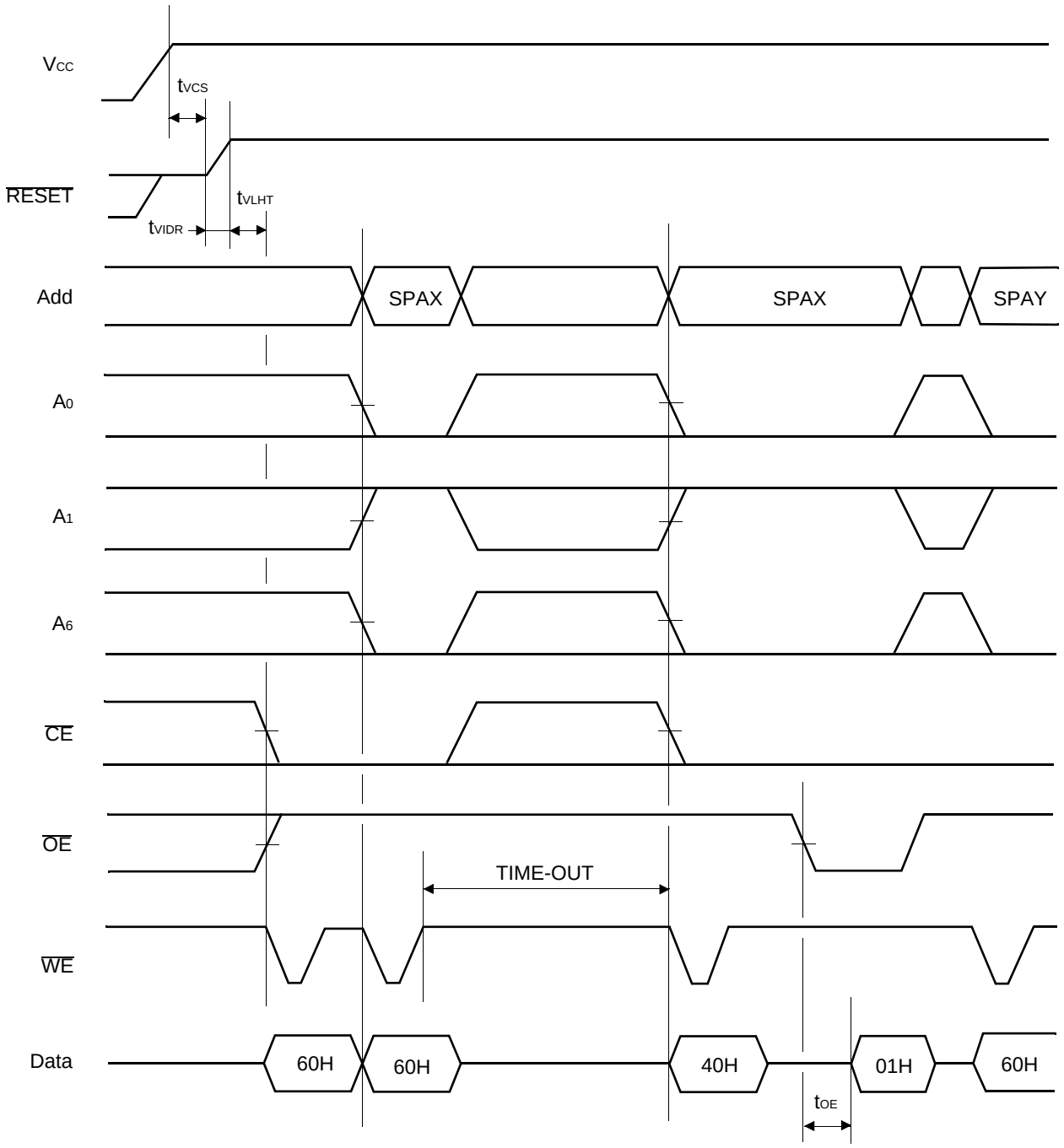
- **$\overline{RESET}$, RY/$\overline{BY}$ Timing Diagram (Flash)**



- **Temporary Sector Unprotection (Flash)**



- **Extended Sector Protection (Flash)**



SPAX : Sector Address to be protected
SPAY : Next Sector Address to be protected
TIME-OUT : Time-Out window = 150 μs (min)

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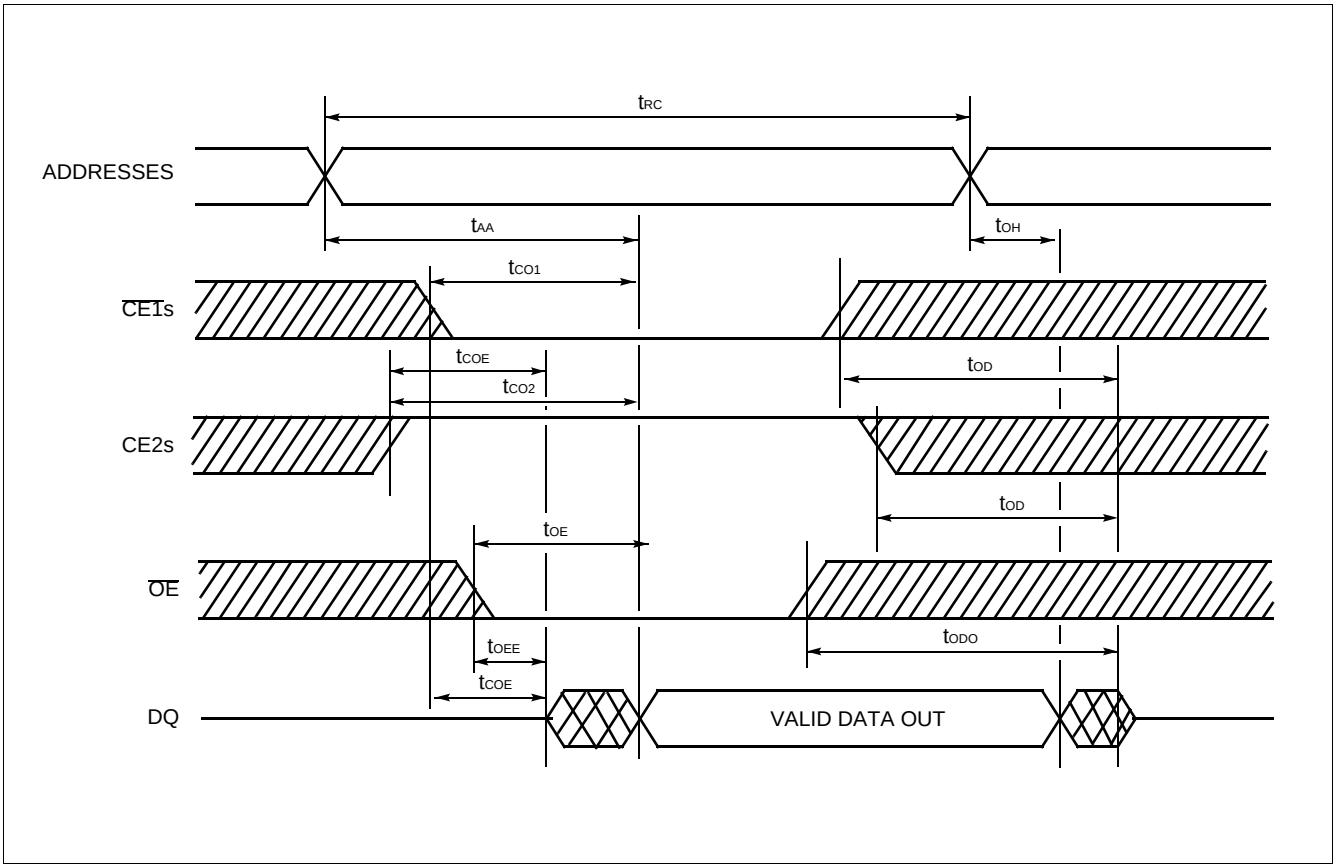
- **Read Cycle (SRAM)**

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{RC}	Read Cycle Time	100	—	ns
t_{AA}	Address Access Time	—	100	ns
t_{CO1}	Chip Enable ($\overline{CE1}$s) Access Time	—	100	ns
t_{CO2}	Chip Enable (CE2s) Access Time	—	100	ns
t_{OE}	Output Enable Access Time	—	50	ns
t_{COE}	Chip Enable ($\overline{CE1}$s Low and CE2s High) to Output Active	5	—	ns
t_{OEE}	Output Enable Low to Output Active	0	—	ns
t_{OD}	Chip Enable ($\overline{CE1}$s High or CE2s Low) to Output High-Z	—	40	ns
t_{ODO}	Output Enable High to Output High-Z	—	40	ns
t_{OH}	Output Data Hold Time	10	—	ns

- **Read Cycle (Note 1) (SRAM)**

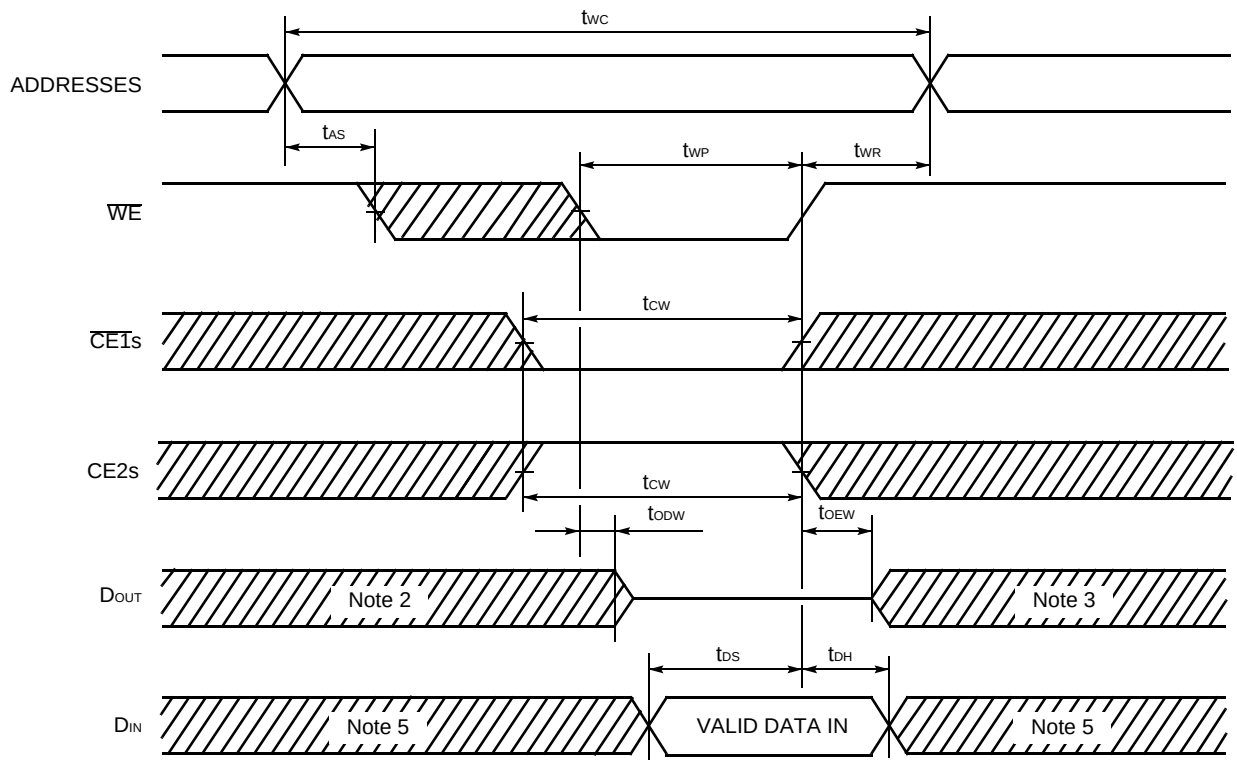


Note: 1. $\overline{WE}$ remains HIGH for the read cycle.

- **Write Cycle (SRAM)**

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{WC}	Write Cycle Time	100	—	ns
t_{WP}	Write Pulse Width	60	—	ns
t_{CW}	Chip Enable to End of Write	80	—	ns
t_{AS}	Address Setup Time	0	—	ns
t_{WR}	Write Recovery Time	0	—	ns
t_{ODW}	$\overline{WE}$ Low to Output High-Z	—	40	ns
t_{OEW}	$\overline{WE}$ High to Output Active	0	—	ns
t_{DS}	Data Setup Time	40	—	ns
t_{DH}	Data Hold Time	0	—	ns

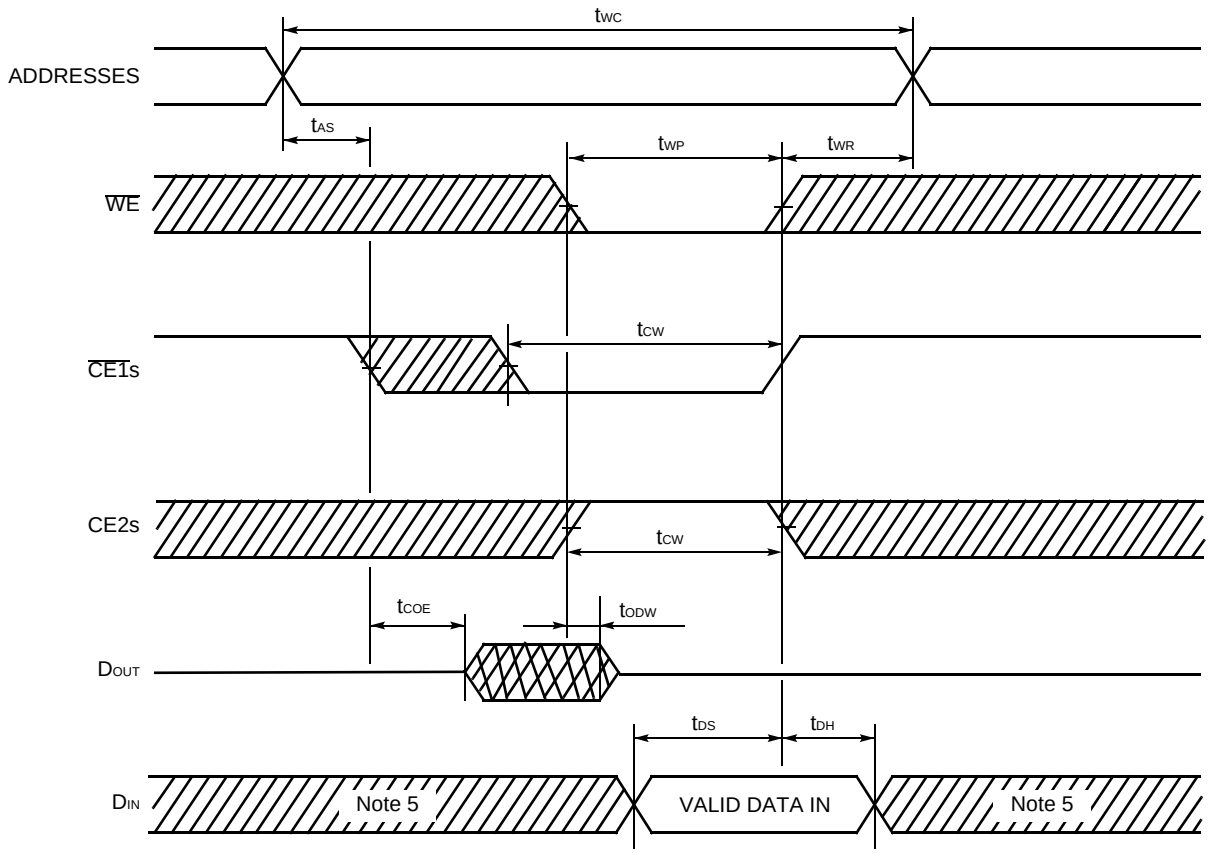
- **Write Cycle (Note 4) ($\overline{WE}$ control) (SRAM)**



Notes: 2. If $\overline{CE1}$s goes LOW (or CE2s goes HIGH) coincident with or after $\overline{WE}$ goes LOW, the output will remain at high impedance.

3. If $\overline{CE1}$s goes HIGH (or CE2s goes LOW) coincident with or before $\overline{WE}$ goes HIGH, the output will remain at high impedance.
4. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
5. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

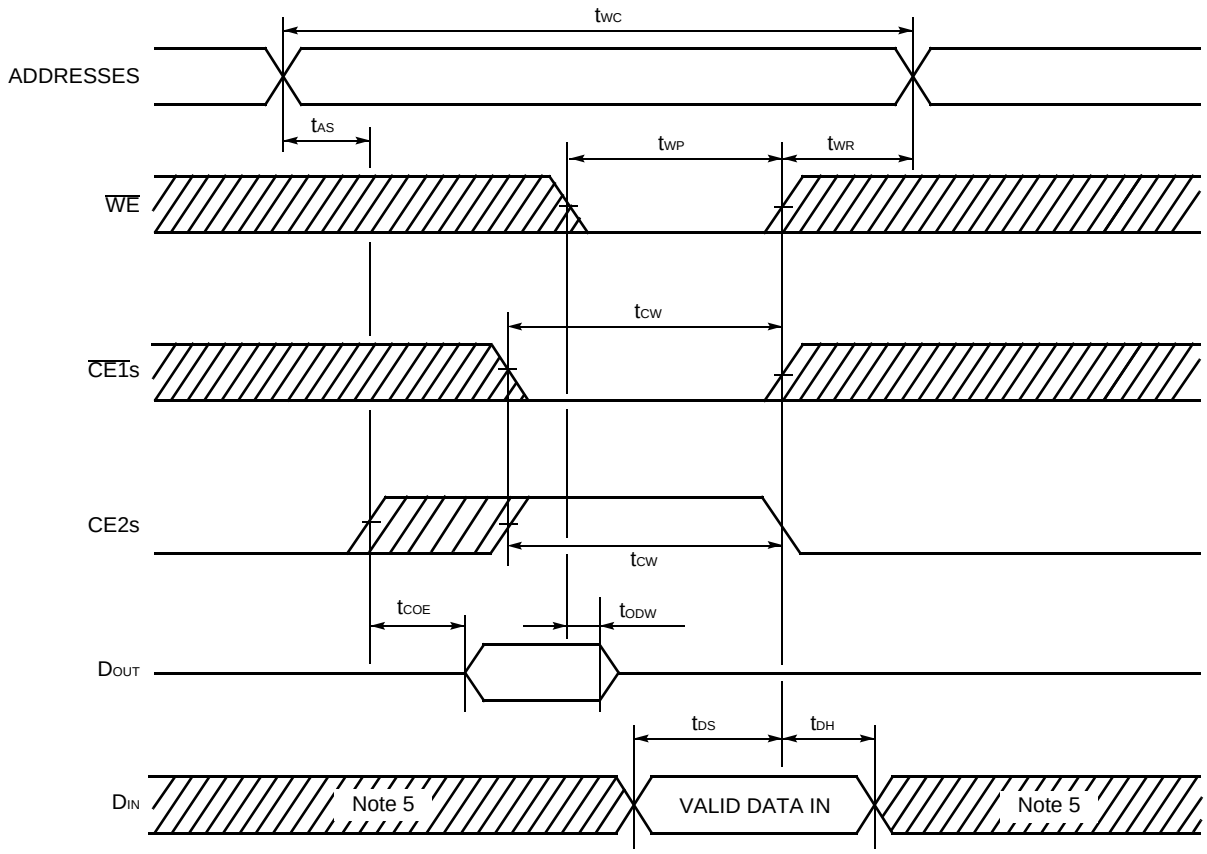
- **Write Cycle (Note 4) ($\overline{CE1}$s control) (SRAM)**



Notes: 2. If $\overline{CE1}$s goes LOW (or CE2s goes HIGH) coincident with or after $\overline{WE}$ goes LOW, the output will remain at high impedance.

3. If $\overline{CE1}$s goes HIGH (or CE2s goes LOW) coincident with or before $\overline{WE}$ goes HIGH, the output will remain at high impedance.
4. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
5. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

- **Write Cycle (Note 4) (CE2s Control) (SRAM)**



Notes: 2. If $\overline{CE1}$s goes LOW (or CE2s goes HIGH) coincident with or after $\overline{WE}$ goes LOW, the output will remain at high impedance.

3. If $\overline{CE1}$s goes HIGH (or CE2s goes LOW) coincident with or before $\overline{WE}$ goes HIGH, the output will remain at high impedance.
4. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
5. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

■ ERASE AND PROGRAMMING PERFORMANCE (Flash)

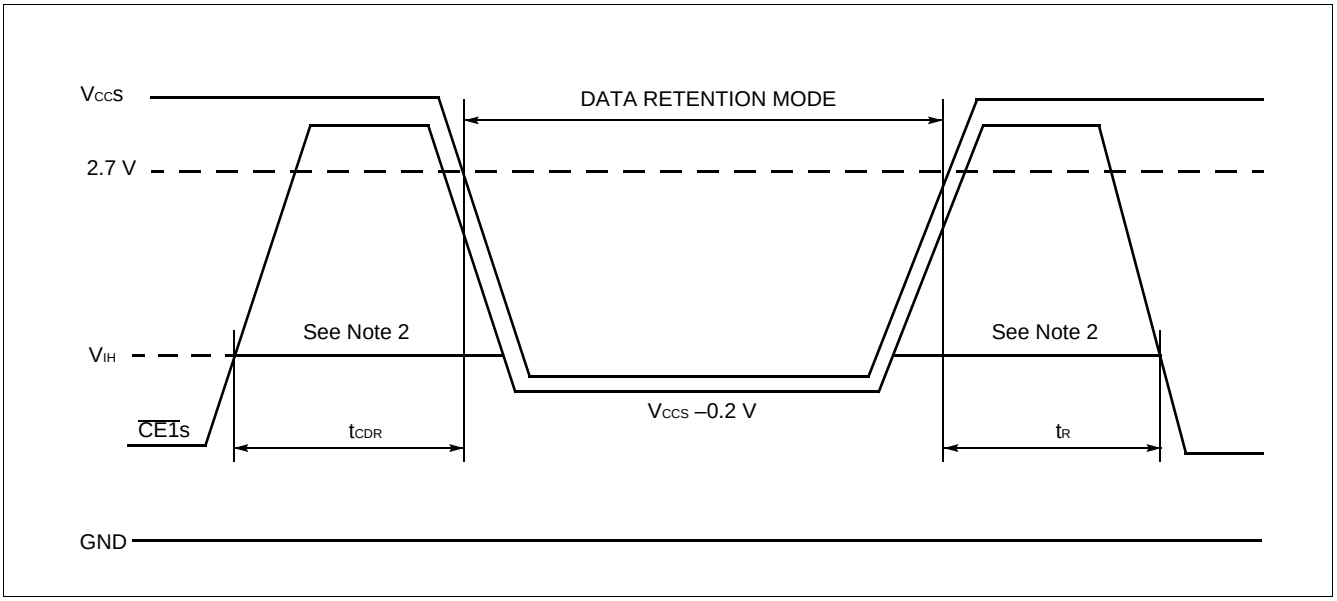
Parameter	Limits			Unit	Comment
	Min.	Typ.	Max.		
Sector Erase Time	—	1	15	sec	Excludes programming time prior to erasure
Byte Programming Time	—	8	3,600	µs	Excludes system-level overhead
Chip Programming Time	—	16.8	100	sec	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycles	

■ DATA RETENTION CHARACTERISTICS (SRAM)

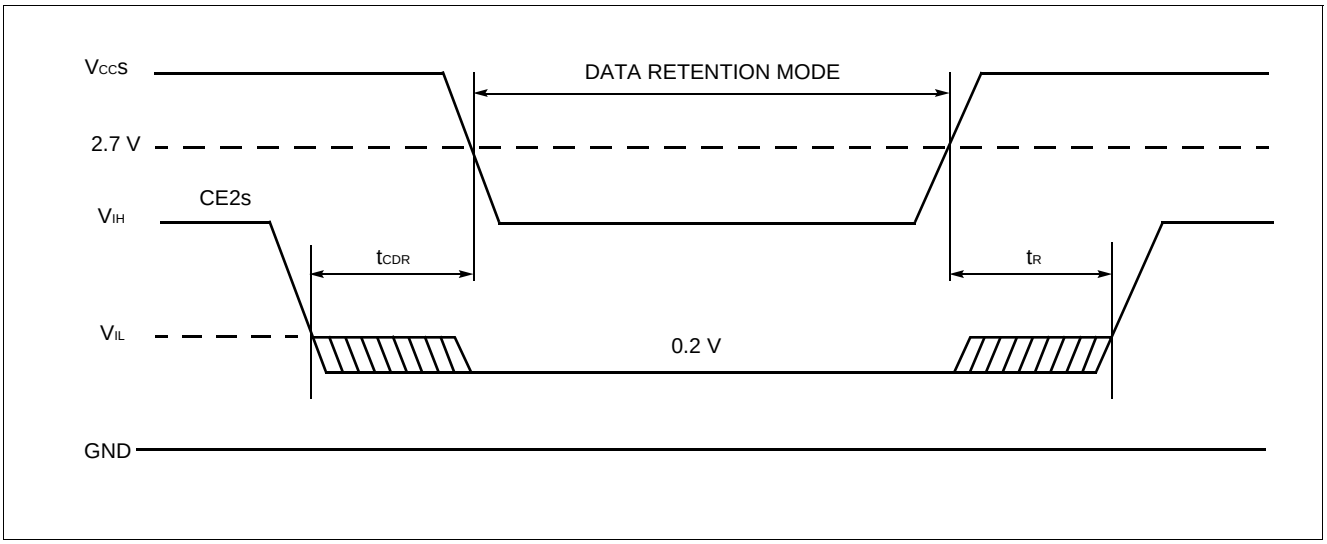
Parameter Symbol	Parameter Description		Min.	Typ.	Max.	Unit
V_{DH}	Data Retention Supply Voltage		2.0	—	3.6	V
I_{DDS2}	Standby Current	V_{DH} = 3.0 V	—	—	50*	µA
		V_{DH} = 3.6 V	—	—	60	µA
t_{CDR}	Chip Deselect to Data Retention Mode Time		0	—	—	ns
t_R	Recovery Time		5	—	—	ms

* : 5 µA (Max.) at T_A = –20°C to +40°C

- **$\overline{CE1}$s Controlled Data Retention Mode (Note 1)**



- **CE2s Controlled Data Retention Mode (Note 3)**



Notes:
1. In $\overline{CE1}$s controlled data retention mode, input level of CE2s should be fixed Vccs to Vccs-0.2V or Vss to 0.2V during data retention mode. Other input and input/output pins can be used between -0.3V to Vccs+0.3V.
2. When $\overline{CE1}$s is operating at the V_{IH} min. level (2.2 V), the standby current is given by I_{SB1}s during the transition of V_{CC}s from 3.6 to 2.2 V.
3. In CE2s controlled data retention mode, input and input/output pins can be used between between -0.3V to Vccs+0.3V.

■ PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	T.B.D	T.B.D	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	T.B.D	T.B.D	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	T.B.D	T.B.D	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ HANDLING OF PACKAGE

Please handle this package carefully since the sides of packages are right angle.

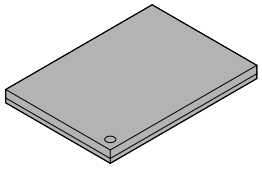
■ CAUTION

1.)The high voltage (VID) can not apply to address pins and control pins except $\overline{RESET}$. Therefore, it can not use autoselect and sector protect function by applying the high voltage (VID) to specific pins.
2.)For the sector protection, since the high voltage (VID) can be applied to the $\overline{RESET}$, it can be protected the sector useing "Extended sector protect" command.

MB84VA2100-10/MB84VA2101-10

■ PACKAGE

48-pin plastic FBGA

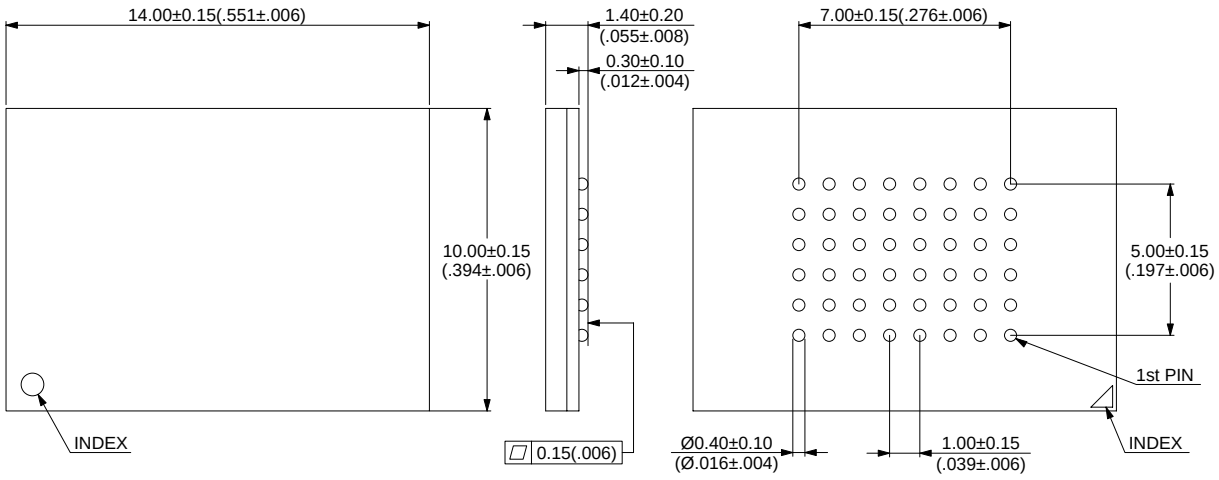


(BGA-48P-M10)

■ PACKAGE DIMENSIONS

48-pin plastic BGA
(BGA-48P-M10)

Note: The actual shape of coners may differ from the dimension.



Dimension in mm (inches).

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