

| | | |
|--------------|------------|--|
| SANYO | No. ※ 4663 | LC36256AL, AML-70W/85W/10W/12W |
| | | 256 K (32768 words × 8 bits) SRAM |

Preliminary

Overview

The LC36256AL, AML-70W/85W/10W/12W are fully asynchronous silicon gate CMOS static RAMs with an 32768 words × 8 bits.

This series has \overline{CE} chip enable pin for device select/nonselect control and an \overline{OE} output enable pin for output control, and features high speed, a wide temperature operating range, as well as low power dissipation.

For these reasons, the series is especially suited for use in systems requiring high speed, low power, and battery backup, and it is easy to expand memory capacity.

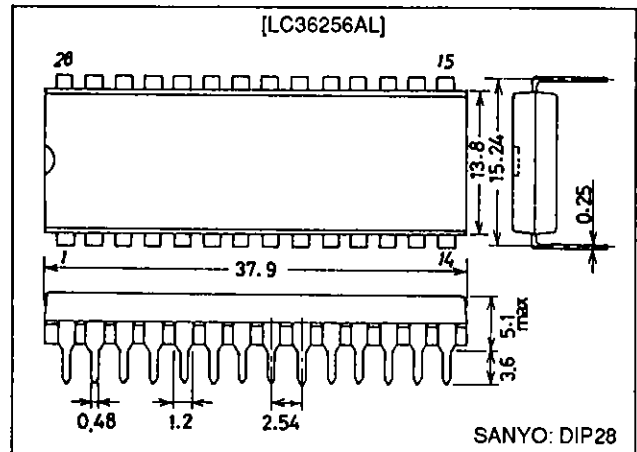
Features

- Access time
 - 70 ns (max.) : LC36256AL-70W, LC36256AML-70W
 - 85 ns (max.) : LC36256AL-85W, LC36256AML-85W
 - 100 ns (max.) : LC36256AL-10W, LC36256AML-10W
 - 120 ns (max.) : LC36256AL-12W, LC36256AML-12W
- Low current dissipation
 - During standby
 - 2 μ A (max.) / Ta = 25°C
 - 5 μ A (max.) / Ta = -10 to +40°C
 - 25 μ A (max.) / Ta = -10 to +70°C
 - During data retention
 - 1 μ A (max.) / Ta = 25°C
 - 2 μ A (max.) / Ta = -10 to +40°C
 - 10 μ A (max.) / Ta = -10 to +70°C
 - During operation (DC)
 - 10 mA (max.)
- Single 5 V power supply: 5 V \pm 10%
- Data retention power supply voltage: 2.0 to 5.5 V
- No clock required (Fully static memory)
- All input/output levels are TTL compatible
- Common input/output pins, with three output states
- Packages
 - DIP 28-pin plastic package : LC36256AL
 - SOP 28-pin plastic package : LC36256AML

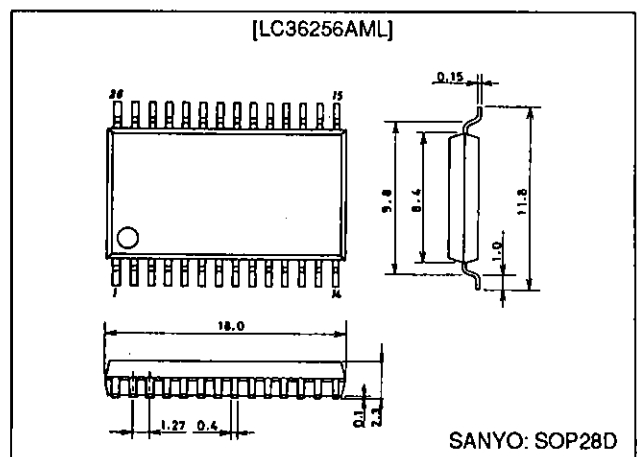
Package Dimensions

unit: mm

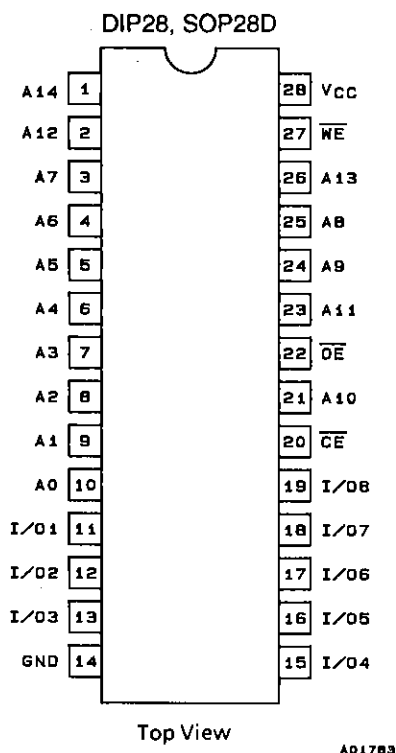
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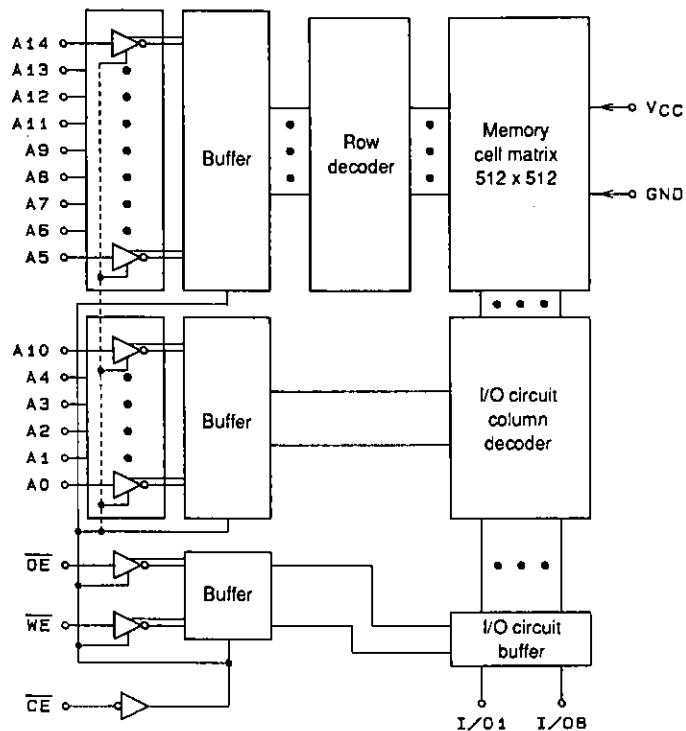
3187-SOP28D



Pin Assignment



Block Diagram



Pin Functions

| | |
|--------------------------------------|--------------------------|
| A ₀ to A ₁₄ | Address input |
| \overline{WE} | Read/write control input |
| \overline{OE} | Output enable input |
| \overline{CE} | Chip enable input |
| I/O ₁ to I/O ₈ | Data input/output |
| V _{CC} , GND | Power supply pins |

Functions

| Mode | \overline{CE} | \overline{OE} | \overline{WE} | I/O | Supply current |
|----------------|-----------------|-----------------|-----------------|----------------|------------------|
| Read cycle | L | L | H | Data output | I _{CCA} |
| Write cycle | L | X | L | Data input | I _{CCA} |
| Output disable | L | H | H | High impedance | I _{CCA} |
| Nonselect | H | X | X | High impedance | I _{CCS} |

X: H or L

Specifications

Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|---------------------|------------|--------------------------------|------|
| Maximum supply voltage | V _{CC} max | | 7.0 | V |
| Input pin voltage | V _{IN} | | -0.5* to V _{CC} + 0.5 | V |
| I/O pin voltage | V _{I/O} | | -0.5* to V _{CC} + 0.5 | V |
| Allowable power dissipation | Pd max | LC36256AL | 1.0 | W |
| | | LC36256AML | 0.7 | W |
| Operating temperature range | T _{opr} | | -10 to +70 | °C |
| Storage temperature range | T _{stg} | | -55 to +150 | °C |

* -3.0 V when pulse width is less than 50 ns

DC Recommended Operating Ranges at Ta = -10 to +70°C

| Parameter | Symbol | min | typ | max | Unit |
|--------------------------|-----------------|-------|-----|-----------------------|------|
| Power supply voltage | V _{CC} | 4.5 | 5.0 | 5.5 | V |
| Input high level voltage | V _{IH} | 2.2 | | V _{CC} + 0.3 | V |
| Input low level voltage | V _{IL} | -0.3* | | +0.8 | V |

* -3.0 V when pulse width is less than 50 ns

DC Electrical Characteristics at Ta = -10 to +70°C, V_{CC} = 5 V ±10%

| Parameter | Symbol | Conditions | min | typ* | max | Unit | |
|----------------------------------|-------------------|--|----------------|--------|------|------|----|
| Input leakage current | I _{LI} | V _{IN} = 0 to V _{CC} | -0.5 | | +0.5 | μA | |
| I/O leakage current | I _{LO} | V _{OE} = V _{IH} or V _{OE} = V _{IH} , V _{I/O} = 0 to V _{CC} | -0.5 | | +0.5 | μA | |
| Output high level voltage | V _{OH} | I _{OH} = -1.0 mA | 2.4 | | | V | |
| Output low level voltage | V _{OL} | I _{OL} = 2.1 mA | | | 0.4 | V | |
| Operating supply current (DC) | I _{CCA1} | V _{OE} ≤ 0.2 V, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V | | 1 | 5 | mA | |
| | I _{CCA2} | V _{OE} = V _{IL} , I _{I/O} = 0 mA | | 3 | 10 | mA | |
| Average operating supply current | I _{CCA3} | min cycle Duty = 100% I _{I/O} = 0 mA | Access time | 70 ns | 30 | 50 | mA |
| | | | | 85 ns | 25 | 50 | |
| | | | | 100 ns | 23 | 50 | |
| | | | | 120 ns | 20 | 50 | |
| Standby supply current | I _{CCS1} | V _{OE} ≥ V _{CC} - 0.2 V | -10 to +70°C | | 25 | μA | |
| | | | -10 to +40°C | | 5 | | |
| | | | 25°C | 0.5 | 2 | | |
| | I _{CCS2} | V _{OE} = V _{IH} | | 0.4 | 2 | mA | |

* Reference values at V_{CC} = 5 V, Ta = 25°C

Input/Output Capacitance at Ta = 25°C, f = 1 MHz

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|--------------------------|------------------|------------------------|-----|-----|-----|------|
| Input/output capacitance | C _{I/O} | V _{I/O} = 0 V | | | 8 | pF |
| Input capacitance | C _{IN} | V _{IN} = 0 V | | | 6 | pF |

Note: These parameters were obtained through sampling, and not full-lot measurement.

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LC36256AL, AML-70W/85W/10W/12W

AC Electrical Characteristics at Ta = -10 to +70°C, V_{CC} = 5 V ±10%

AC testing conditions

| | | |
|-----------------------------|---|--|
| Input pulse voltage level | : | 0.8 V, 2.2 V |
| Input rise and fall time | : | 5 ns |
| Input - output timing level | : | 1.5 V |
| Output load | : | 1 TTL gate + C _L = 100 pF (85 ns/100 ns/120 ns) |
| | | 1 TTL gate + C _L = 30 pF (70 ns) |
| | | (including scope and jig capacitance) |

Read Cycle

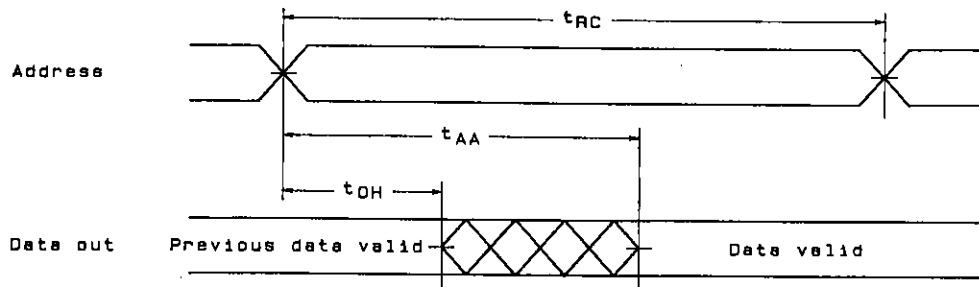
| Parameter | Symbol | LC36256AL-70W LC36256AML-70W | | LC36256AL-85W LC36256AML-85W | | LC36256AL-10W LC36256AML-10W | | LC36256AL-12W LC36256AML-12W | | Unit |
|--|------------------|---------------------------------|-----------------|---------------------------------|-----|---------------------------------|-----|---------------------------------|-----|------|
| | | min | max | min | max | min | max | min | max | |
| | | Read cycle time | t _{RC} | 70 | | 85 | | 100 | | |
| Address access time | t _{AA} | | 70 | | 85 | | 100 | | 120 | ns |
| $\overline{\text{CE}}$ access time | t _{CA} | | 70 | | 85 | | 100 | | 120 | ns |
| $\overline{\text{OE}}$ access time | t _{OA} | | 35 | | 45 | | 50 | | 60 | ns |
| Output hold time | t _{OH} | 20 | | 20 | | 20 | | 20 | | ns |
| $\overline{\text{CE}}$ output enable time | t _{COE} | 10 | | 10 | | 10 | | 10 | | ns |
| $\overline{\text{OE}}$ output enable time | t _{OOE} | 5 | | 5 | | 5 | | 5 | | ns |
| $\overline{\text{CE}}$ output disable time | t _{COD} | 0 | 30 | 0 | 30 | 0 | 30 | 0 | 30 | ns |
| $\overline{\text{OE}}$ output disable time | t _{OOD} | 0 | 30 | 0 | 30 | 0 | 30 | 0 | 30 | ns |

Write Cycle

| Parameter | Symbol | LC36256AL-70W LC36256AML-70W | | LC36256AL-85W LC36256AML-85W | | LC36256AL-10W LC36256AML-10W | | LC36256AL-12W LC36256AML-12W | | Unit |
|--|------------------|---------------------------------|-----------------|---------------------------------|-----|---------------------------------|-----|---------------------------------|-----|------|
| | | min | max | min | max | min | max | min | max | |
| | | Write cycle time | t _{WC} | 70 | | 85 | | 100 | | |
| Address valid to end of write | t _{AW} | 65 | | 75 | | 80 | | 100 | | ns |
| Address setup time | t _{AS} | 0 | | 0 | | 0 | | 0 | | ns |
| Write pulse width | t _{WP} | 50 | | 50 | | 60 | | 70 | | ns |
| $\overline{\text{CE}}$ setup time | t _{CW} | 65 | | 75 | | 80 | | 100 | | ns |
| Write recovery time ($\overline{\text{WE}}$) | t _{WR} | 0 | | 0 | | 0 | | 0 | | ns |
| Write recovery time ($\overline{\text{CE}}$) | t _{WRI} | 0 | | 0 | | 0 | | 0 | | ns |
| Data setup time | t _{DS} | 30 | | 30 | | 35 | | 40 | | ns |
| Data hold time | t _{DH} | 0 | | 0 | | 0 | | 0 | | ns |
| $\overline{\text{WE}}$ output enable time | t _{WOE} | 10 | | 10 | | 10 | | 10 | | ns |
| $\overline{\text{WE}}$ output disable time | t _{WOD} | 0 | 25 | 0 | 25 | 0 | 25 | 0 | 25 | ns |

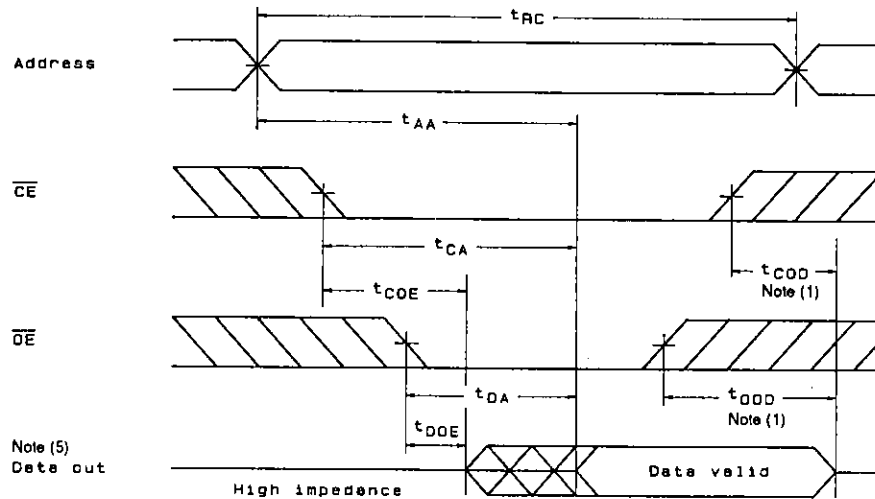
Timing Chart

- Read Cycle (1): $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$



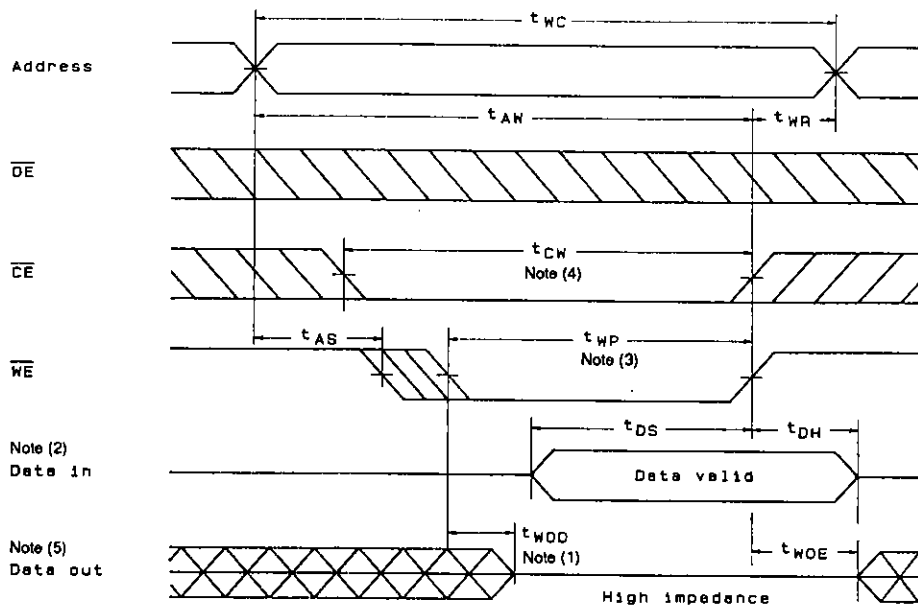
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- Read Cycle (2): $\overline{WE} = V_{IH}$



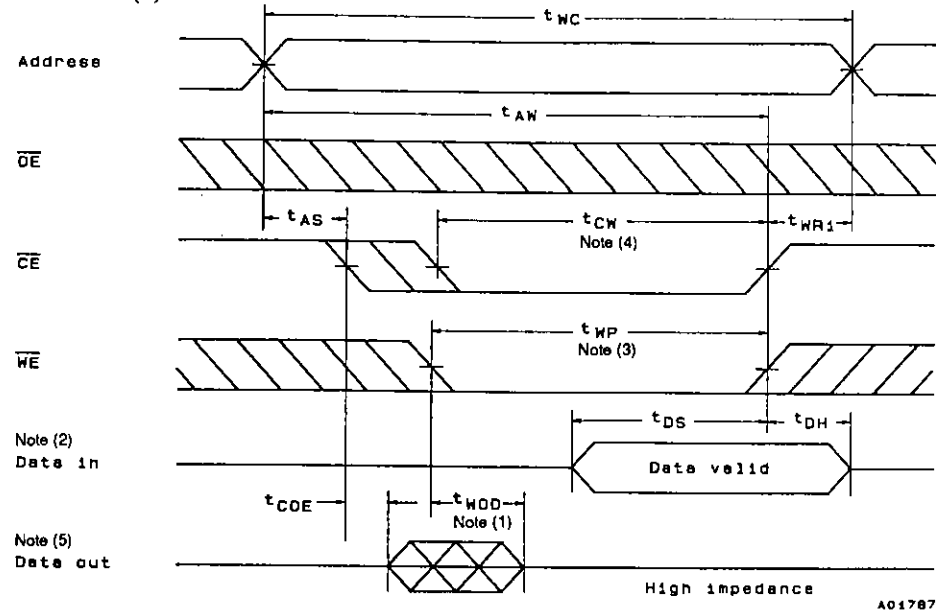
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- Write Cycle (1): \overline{WE} Control Note (6)



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• Write Cycle (2): \overline{CE} Control Note (6)



- Notes: (1) t_{COD} , t_{OOD} , and t_{WOD} are defined as the time at which the outputs becomes the high impedance state and are not referred to output voltage levels.
 (2) An external antiphase signal must not be applied when D_{OUT} is in the output state.
 (3) t_{WP} is the time interval that \overline{CE} and \overline{WE} are low-level and is defined as the interval from the falling of \overline{WE} to the rising of \overline{CE} or \overline{WE} whichever is earlier.
 (4) t_{CW} is the time interval that \overline{CE} and \overline{WE} are low-level and is defined as the time from the falling of \overline{CE} to the rising of \overline{CE} or \overline{WE} whichever is earlier.
 (5) D_{OUT} goes to the high-impedance state when either \overline{OE} is high-level, \overline{CE} is high-level, or \overline{WE} is low-level.
 (6) When \overline{OE} is high-level during the write cycle, D_{OUT} goes to the high-impedance state.

Data Retention Characteristics at $T_a = -10$ to $+70^\circ\text{C}$

| Parameter | Symbol | Conditions | min | typ* | max | Unit |
|-------------------------------|-------------|--|----------------------------|------|------|---------------|
| Data retention supply voltage | V_{DR} | $V_{CE} \geq V_{CC} - 0.2\text{ V}$ | 2.0 | | 5.5 | V |
| Data retention supply current | I_{CCDR1} | $V_{CC} = 3.0\text{ V}$, $V_{CE} \geq 2.8\text{ V}$ | -10 to $+70^\circ\text{C}$ | | 10 | μA |
| | | | -10 to $+40^\circ\text{C}$ | | 2 | |
| | | | 25 $^\circ\text{C}$ | | 0.25 | |
| | I_{CCDR2} | $V_{CC} = 2.0$ to 5.5 V , $V_{CE} \geq V_{CC} - 0.2\text{ V}$ | | 0.5 | 25 | μA |
| \overline{CE} setup time | t_{CDR} | | 0 | | | ns |
| \overline{CE} hold time | t_R | | t_{RC}^{**} | | | ns |

* Reference values at $T_a = 25^\circ\text{C}$
 ** t_{RC} = read cycle time

Data Retention Waveform

