Ordering number : EN4430C

CMOS LSI

LC33832P, S, M, PL, SL, ML-70/80/10

256 K (32768 words × 8 bits) Pseudo-SRAM

Overview

The LC33832 series is composed of pseudo static RAM that operates on a single 5 V power supply and is organized as 32768 words × 8 bits. By using memory cells each composed of a single transistor and capacitor, together with peripheral CMOS circuitry, this series achieves ease of use with high density, high speed, and low power dissipation. The LC33832 series can easily accomplish auto-refresh and self-refresh by means of $\overline{OE}$/RFSH input. As with asynchronous static RAM, $\overline{WE}$ input uses a system for incorporating input data at the $\overline{WE}$ rise, thereby facilitating interfacing with a microcomputer.

The LC33832 series features pin compatibility with 256 K static RAM (the LC36256A series), and available packages are the standard 28-pin DIP with widths of 600 mil or 300 mil, and the SOP with a width of 450 mil.

$\overline{CE}$-only refresh can be accomplished by selecting address 256 (A0 to A7) within 4 ms.

Features

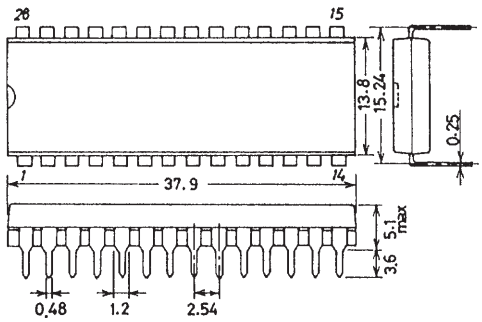
- 32768 words × 8 bits configuration
- Single 5 V ±10% power supply
- All input and output (I/O) TTL compatible
- Fast access times and low power dissipation
- 4 ms refresh using 256 refresh cycle
- $\overline{CE}$-only refresh, auto-refresh, and self-refresh
- Low-power version: 100 µA self-refresh current
- Package
  DIP28-pin (600 mil) plastic package: LC33832P, PL
  DIP28-pin (300 mil) plastic package: LC33832S, SL
  SOP28-pin (450 mil) plastic package: LC33832M, ML

Package Dimensions

unit: mm

3012A-DIP28

[LC33832P, PL]

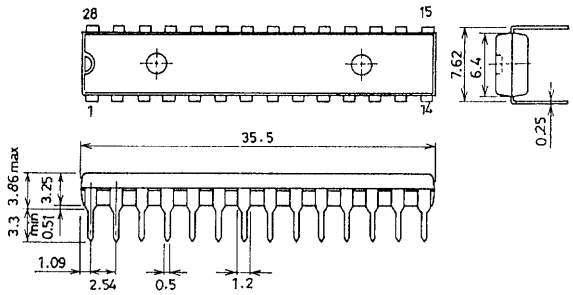


SANYO: DIP28

unit: mm

3133-DIP28

[LC33832S, SL]



SANYO: DIP28

• $\overline{CE}$ access time/$\overline{OE}$ access time/Cycle time/Current drain

Parameter		LC33832P, S, M, PL, SL, ML		
		-70	-80	-10
$\overline{CE}$ access time		70 ns	80 ns	100 ns
$\overline{OE}$ access time		30 ns	35 ns	40 ns
Cycle time		115 ns	130 ns	160 ns
Current drain	Operating	65 mA	60 mA	50 mA
	Standby	1 mA/100 µA (L version)		

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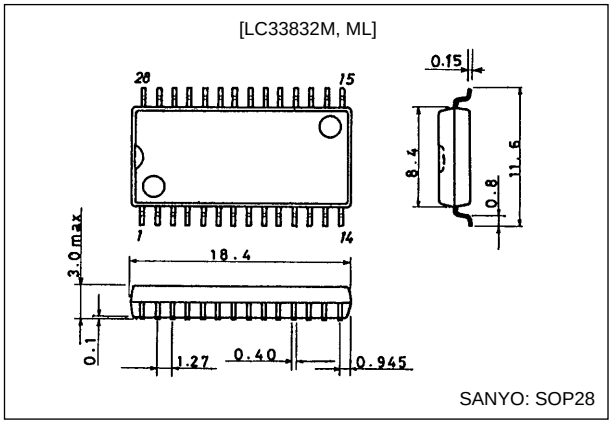
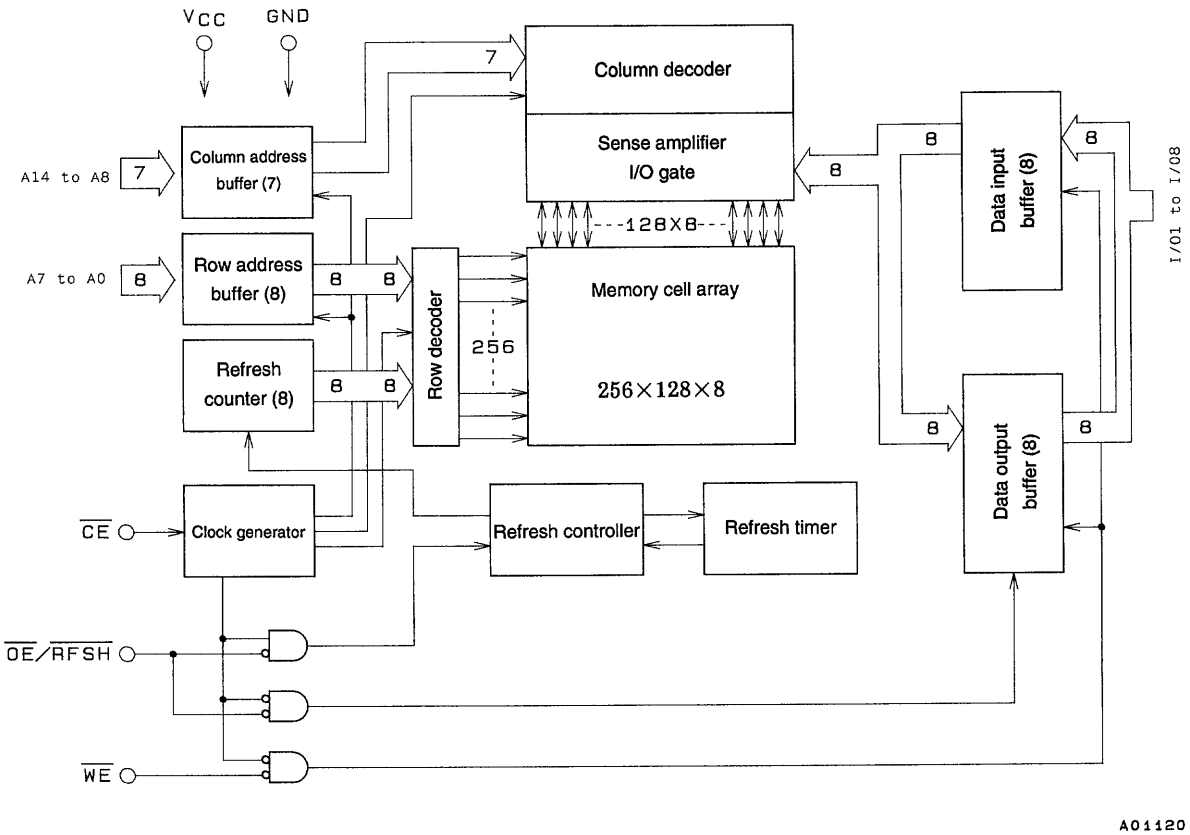
unit : mm

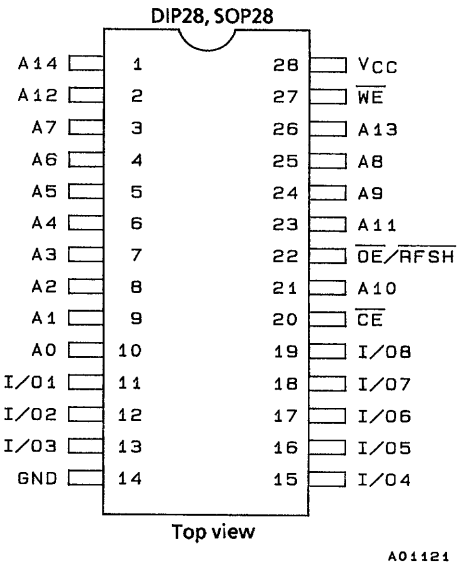
3158-SOP28



Block Diagram



Pin Assignment



Pin Functions

A0 to A14	Address input
$\overline{WE}$	Read/Write input
$\overline{OE}$/$\overline{RFSH}$	Output-enable input/ refresh input
$\overline{CE}$	Chip-enable input
I/O1 to I/O8	Data input/output
V_{CC}	Power supply
GND	Ground

Functional Logic

$\overline{CE}$	$\overline{OE}$ /$\overline{RFSH}$	WE	A0 to A7	A8 to A14	I/O1 to I/O8	State
H	H	X	X	X	HZ	Standby
L	L	H	VX	VX	OUT	Read
L	H	L	VX	VX	IN	Write
L	H	H	VX	X	HZ	$\overline{CE}$-only refresh
H	L	X	X	X	HZ	Self-refresh
H	NP	X	X	X	HZ	Auto-refresh

H .....High-level input of V_{IN} = 6.5 V to V_{IH} (min)
L .....Low-level input of V_{IN} = V_{IL} (max) to –1.0 V
X.....High- or low-level input
NP.....Negative-polarity pulse input
VX.....“IN” when $\overline{CE}$ = L is confirmed, then “X”
HZ.....High impedance
IN .....Input state
OUT.....Output state

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Maximum supply voltage	V_{CC} max	–1.0 to +7.0	V	1
Input voltage	V_{IN}	–1.0 to +7.0	V	1
Output voltage	V_{OUT}	–1.0 to +7.0	V	1
Allowable power dissipation	Pd max	600	mW	1
Output short-circuit current	I_{OUT}	50	mA	1
Operating temperature	Topr	0 to +70	°C	1
Storage temperature	Tstg	–55 to +150	°C	1

Note: 1) Stresses greater than the above listed maximum values may result in damage to the device.

DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	min	typ	max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	2
Input high level voltage	V_{IH}	2.4		6.5	V	2
Input low level voltage	V_{IL}	–1.0		+0.8	V	2

Note: 2) All voltages are referenced to GND.

DC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 5V±10%

Parameter	Symbol	Conditions			min	max	Unit	Note
Operating current	I_{CCA}	Average current during operation	Access time	70ns		65	mA	3,4
				80ns		60		
				100ns		50		
Standby current 1	I_{CCS1}	$\overline{CE}$ = $\overline{OE}$/$\overline{RFSH}$ = V_{IH}				1	mA	
Standby current 2	I_{CCS2}	$\overline{CE}$ = $\overline{OE}$/$\overline{RFSH}$ = V_{CC} –0.2V	LC33832P, S, M		1	mA		
			LC33832PL, SL, ML			100	µA	
Self-refresh current	I_{CCSR}	$\overline{CE}$ = V_{CC}–0.2V, $\overline{OE}$/$\overline{RFSH}$ = 0.2V	LC33832P, S, M		1	mA		
			LC33832PL, SL, ML			100	µA	
Input leakage current	I_{IL}	0V≤V_{IN}≤V_{CC}, pins other than test pin = 0V			–10	+10	µA	
Output leakage current	I_{OL}	D_{OUT} disable, 0V≤V_{OUT}≤V_{CC}			–10	+10	µA	
Output high level voltage	V_{OH}	I_{OUT} = –5mA			2.4		V	
Output low level voltage	V_{OL}	I_{OUT} = 4.2mA				0.4	V	

Note: 3) All current values are measured at minimal cycle rate. Since current flows immoderately, cycle times may become longer and shorter than shown here.

4) Dependent on output load. Maximum value is value during free state.

Input/Output Capacitance Characteristics at Ta = 25°C, f = 1MHz, V_{CC} = 5V±10%

Parameter	Symbol	min	max	Unit	Test conditions
Input capacitance (A0 to A14)	C_{IN1}		5	pF	V_{IN1} = 0 V
Input capacitance ($\overline{CE}$, $\overline{OE}$/$\overline{RFSH}$, $\overline{WE}$)	C_{IN2}		7	pF	V_{IN2} = 0 V
Input/output capacitance	$C_{I/O}$		10	pF	$V_{I/O}$ = 0 V

Sampling inspections, and not full-lot inspections, are carried out for these parameters.

AC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} 5V±10% (Notes 5, 6, 7, 8, 9)

Parameter	Symbol	LC33832P, S, M, PL, SL, ML						Unit	Note
		-70		-80		-10			
		min	max	min	max	min	max		
Random read, write cycle time	t_{RC}	115		130		160		ns	
Read-write cycle time	t_{RMW}	165		195		240		ns	
$\overline{CE}$ pulse width	t_{CE}	70	10000	80	10000	100	10000	ns	
$\overline{CE}$ precharge time	t_P	35		40		50		ns	
$\overline{CE}$ access time	t_{CEA}		70		80		100	ns	
$\overline{OE}$ access time	t_{OEA}		30		35		40	ns	
$\overline{CE}$ output enable time	t_{CLZ}	10		10		10		ns	
$\overline{OE}$ output enable time	t_{OLZ}	0		0		0		ns	
$\overline{WE}$ output enable time	t_{WLZ}	0		0		0		ns	
$\overline{CE}$ output disable time	t_{CHZ}	0	20	0	25	0	30	ns	10
$\overline{OE}$ output disable time	t_{OHZ}	0	20	0	25	0	30	ns	10
$\overline{WE}$ output disable time	t_{WHZ}	0	20	0	25	0	30	ns	10
$\overline{OE}$ hold time for $\overline{CE}$	t_{OHC}	0		0		0		ns	
$\overline{OE}$ setup time for $\overline{CE}$	t_{OSC}	10		10		10		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		ns	
Write pulse width	t_{WP}	55		60		70		ns	
Write command hold time	t_{WCH}	55		60		70		ns	
Write command lead time	t_{CWL}	55		60		70		ns	
Input data setup time for $\overline{WE}$	t_{DSW}	30		35		40		ns	11
Input data setup time for $\overline{CE}$	t_{DSC}	30		35		40		ns	11
Input data hold time for $\overline{WE}$	t_{DHW}	0		0		0		ns	11
Input data hold time for $\overline{CE}$	t_{DHC}	0		0		0		ns	11
Address setup time for $\overline{CE}$	t_{ASC}	0		0		0		ns	12
Address hold time for $\overline{CE}$	t_{AHC}	15		20		25		ns	12
Auto-refresh cycle time	t_{FC}	115		130		160		ns	
$\overline{RFSH}$ delay time for $\overline{CE}$	t_{RFD}	35		40		50		ns	
$\overline{RFSH}$ pulse width (auto-refresh)	t_{FAP}	75	8000	80	8000	80	8000	ns	13
$\overline{RFSH}$ precharge time (auto-refresh)	t_{FP}	30		30		30		ns	13
$\overline{RFSH}$ active $\overline{CE}$ delay time (auto-refresh)	t_{FCE}	135		160		190		ns	13
$\overline{RFSH}$ pulse width (self-refresh)	t_{FAS}	8000		8000		8000		ns	13
$\overline{RFSH}$ precharge $\overline{CE}$ delay time (self-refresh)	t_{FRS}	135		160		190		ns	13
Refresh time	t_{REF}		4		4		4	ms	
Rise and fall time	t_T	3	50	3	50	3	50	ns	

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Note : 5) To accomplish internal initialization, $\overline{CE}$ and $\overline{OE}/\overline{RFSH}$ are fixed at V_{IH} for an interval of 1 ms when V_{CC} reaches the specified voltage after power is switched on.

6) Measured at t_T = 5 ns.

7) When measuring input signal timing, V_{IH} (min) and V_{IL} (max) are reference levels.

8) Measured using an equivalent of 100 pF and two standard TTL loads.

9) $\overline{OE}/\overline{RFSH}$ input functions as output-enable input ($\overline{OE}$) when $\overline{CE}$ = V_{IL}, and as refresh input ($\overline{RFSH}$) when $\overline{CE}$ = V_{IH}.

10) t_{CHZ}, t_{OHZ}, and t_{WHZ} are defined as the time until output enters the open circuit state and the output voltage level becomes immeasurable.

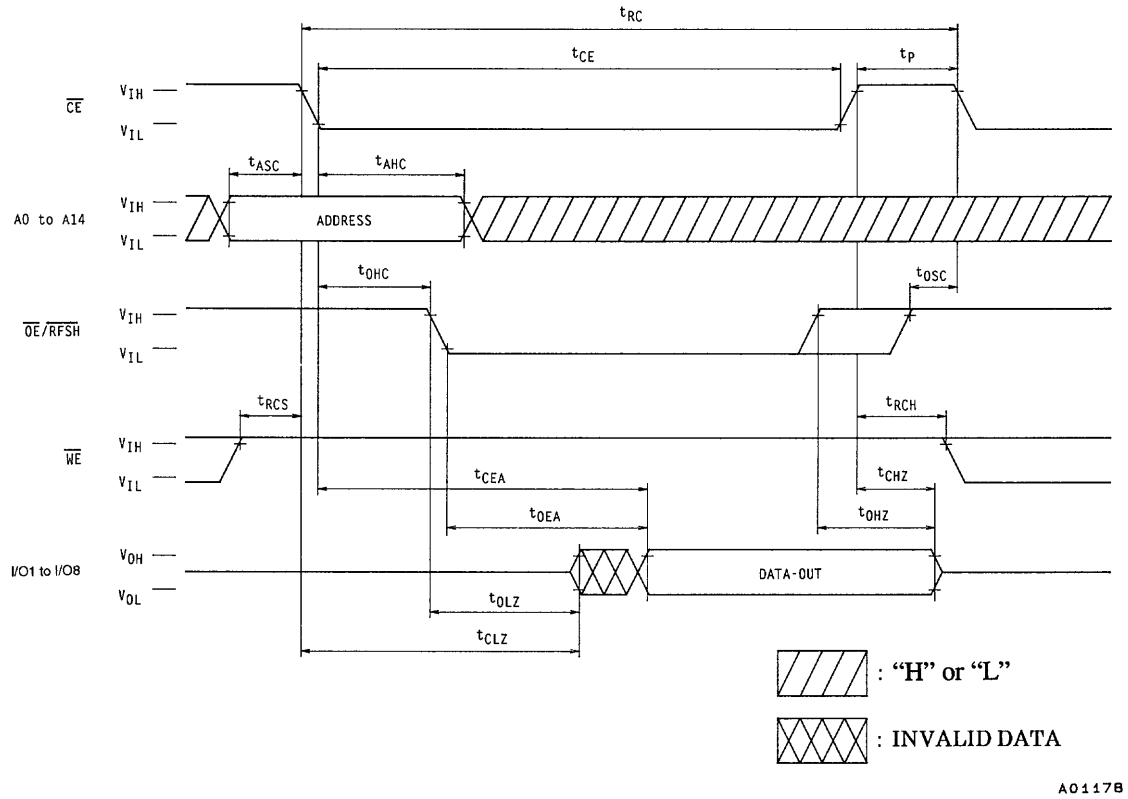
11) As with ordinary static RAM, write data is incorporated at the rise of $\overline{WE}$ input or $\overline{CE}$ input, whichever is earlier, and write data is therefore held during t_{DSW}, t_{DSC}, t_{DHW}, or t_{DHC}.

12) Because address input is incorporated at the fall of $\overline{CE}$, the address is maintained during t_{ASC} or t_{AHC}.

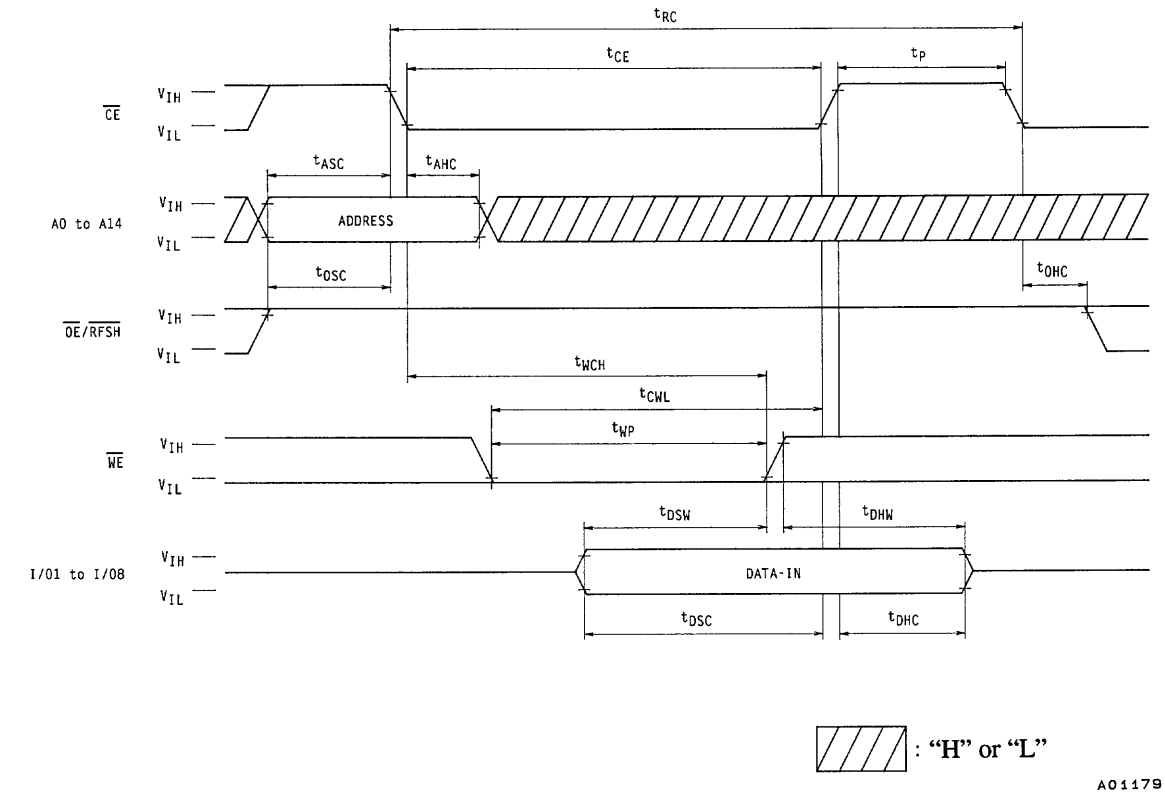
13) Auto-refresh and self-refresh are determined by $\overline{OE}/\overline{RFSH}$ pulse width when $\overline{CE}$ = V_{IH}, and are defined as auto-refresh when below t_{FAP} (max), or as self-refresh when above t_{FAS} (min). In order to activate $\overline{CE}$ after the completion of each refresh, t_{FCE} must be assured for auto-refresh, or t_{FRS} must be assured for self-refresh.

Timing Chart

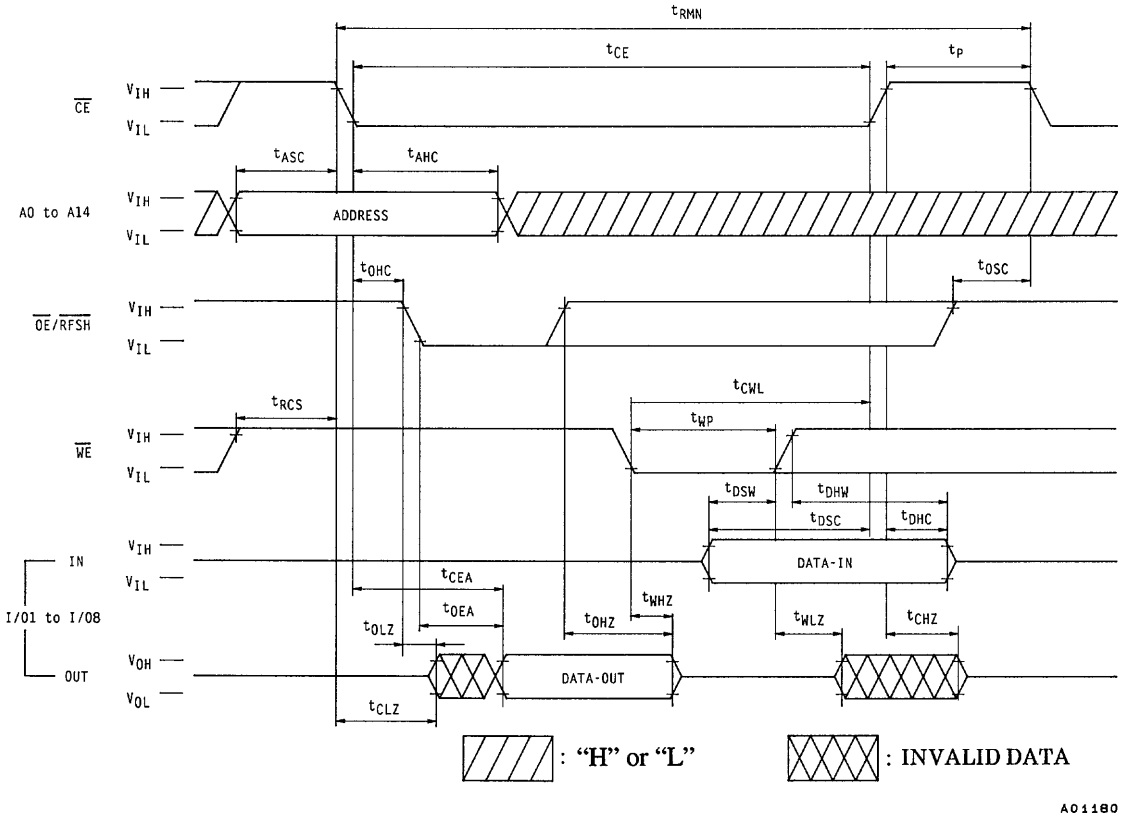
Read Cycle



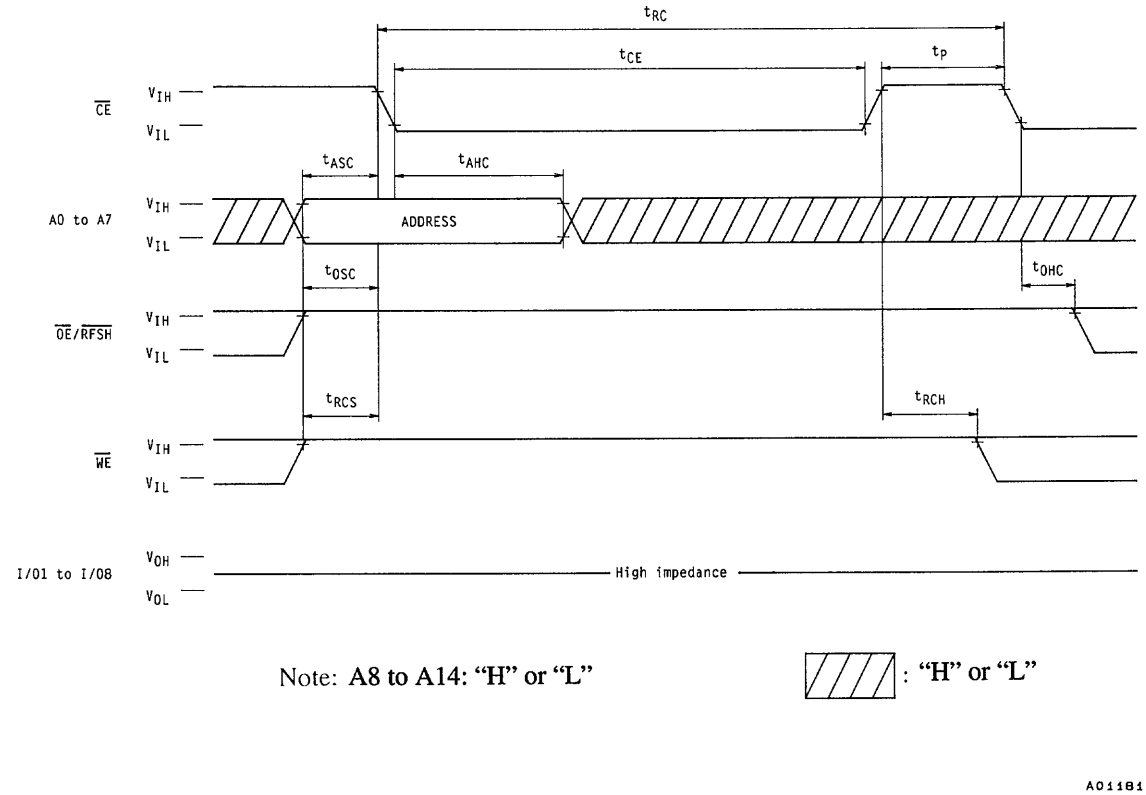
Write Cycle



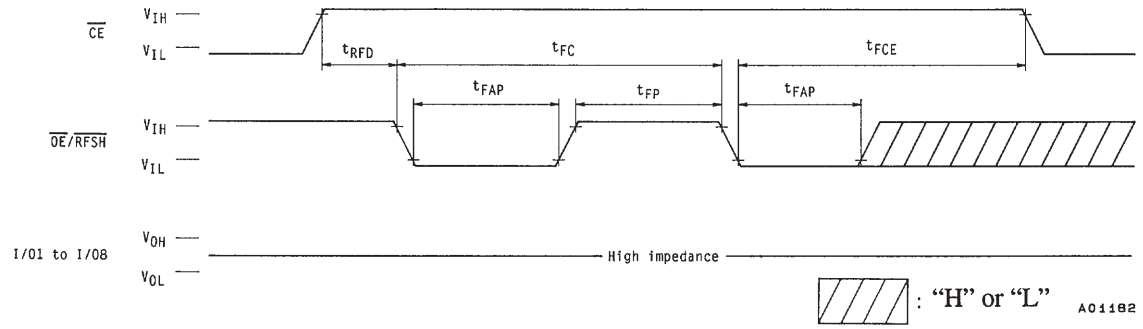
Read-Write Cycle



CE-Only Refresh Cycle

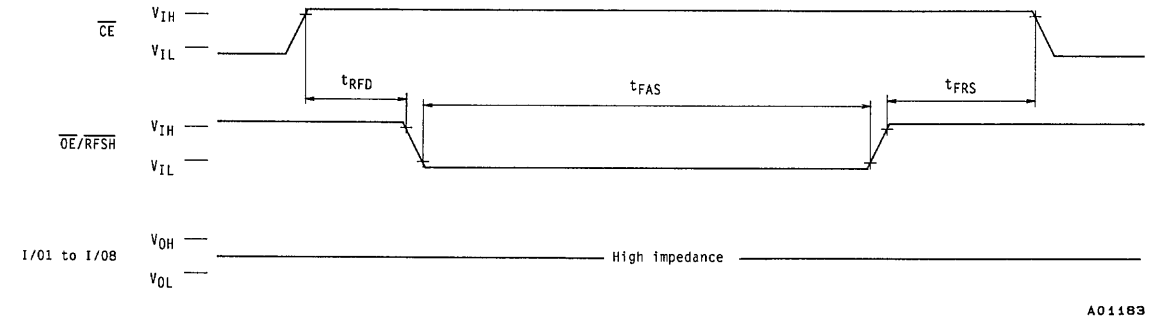


Auto-Refresh Cycle



Note: A0 to A14, $\overline{WE}$: "H" or "L"

Self-Refresh Cycle



Note: A0 to A14, $\overline{WE}$: "H" or "L"