TEMIC
Semiconductors

10MRAD(Si)

DMILL

Mixed Analog/Digital Radiation Hard BiCMOS

MPW

An emerging need in HEP

The decision to develop new equipment for High Energy Physics (HEP) research has led the need for ultra rad hard technology. The radiation tolerance for detector electronics adjacent to proton collision areas can be above 10 Mrad. Furthermore, the low level of the detector signals imposes very high signal to noise ratios. To meet these new requirements, the French Commissariat à l'Energie Atomique (CEA), an organization highly involved in almost all advanced nuclear physics research, has, by taking advantage of its extensive experience in silicon on insulator (SOI) hardened techniques, developed the DMILL technology (Durci Mixte Isolant Logico Linéaire), a mixed analog/digital technology hardened to tolerate more than 10Mrad and 10^{14} neutrons/cm². TEMIC started the industrial transfer of DMILL into its Nantes (France) factory in 1995. Testing of prototyping based on this technology and the subsequent large scale production are planned for early 1997 .

1E14 n/cm^2

Civilian nuclear field

High radiation hardness levels are also of interest for engineers designing civilian nuclear equipment. Up to now they have not been suitable electronics for operating under very high radiation levels in hot areas in nuclear power plants and nuclear waste processing facilities. The rule has been to use discrete or passive equipment. As it is hardened against both photons and neutrons, DMILL technology provides a very efficient solution for these environments.

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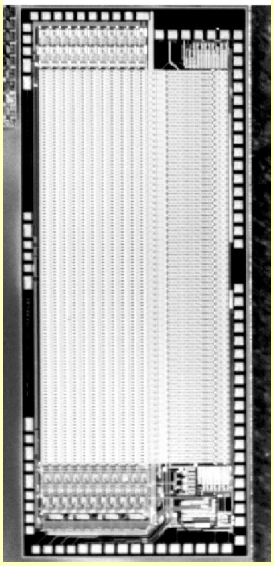


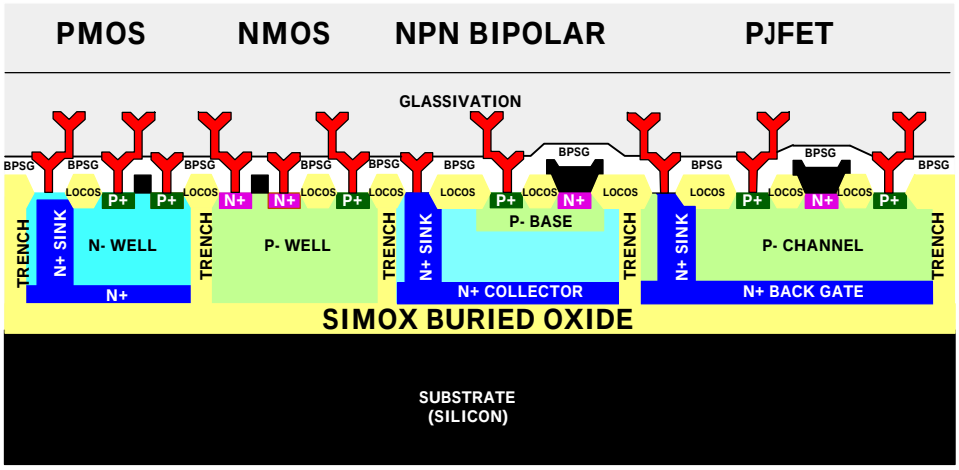
Photo CEA

Performance Demonstration

This technology, which has been selected by numerous groups for the prototype electronics of the two major LHC (Large Hadron Collider) experiments (ATLAS & CMS) has demonstrated high integration levels (1 Million transistors per cm²) for mixed analog/digital circuits, very low noise features and high radiation hardness. For example, the data for a CEA sliced 16-bit microprocessor designed for civilian nuclear applications show an extremely low sensitivity to radiation. application.

DMILL Cross Section

On one single chip, DMILL provides access to 4 different active devices. Two low-noise N and P MOS transistors with 0.8µm minimum gate length are available. For fast-low noise analog applications, there is a NPN bipolar transistor with a typical gain of 150. A-P type JFET is also proposed as well as resistors and capacitors. All these components are hardened to tolerate a combination of 10Mrad and 1E14n/cm² fluence.



DMILL Basic Electrical parameters

Access to DESIGN KIT requires signing a Non Disclosure Agreement. This kit includes electrical and topological data files (for Spice, ELDO environments). Cadence DRC and LVS tools are also available as well as some Input/ Output cells.

Parameter	Typical Value	Unit	Comments
MOS TRANSISTOR			
Leff N	0.62	µm	Electrical length of a 0.8µm N-channel device
Leff P	0.78	µm	Electrical length of a 0.8µm P-channel device
VTN	0.80	V	Threshold voltage for 25/0.8 N transistor
VTP	-0.80	V	Threshold voltage for 25/0.8 P transistor
IDSN (0.8)	7.5	mA	Drain current of a 25/0.8 N Transistor with VGS=VDS=5.0V
IDSP (0.8)	4.25	mA	Drain current of a 25/0.8 P Transistor with VGS=VDS=5.0V
NPN-BIPOLAR			
Beta (1.2*1.2)	175	NU	NPN 1.2*1.2 ideal forward beta
BVCEO	15.0	V	Breakdown of collector/emitter junction with base open
BVCBO	17.0	V	Breakdown of collector/base junction with emitter open
P-JFET			
VPPJ1.2	1.2	V	Pinch-off voltage of a 100/1.2 P-JFET
GDPJ1.2	1.135	µS/µm	Drain Transconductance of a 100/1.2 P-JFET (VGS=0V, VDS=-3V)

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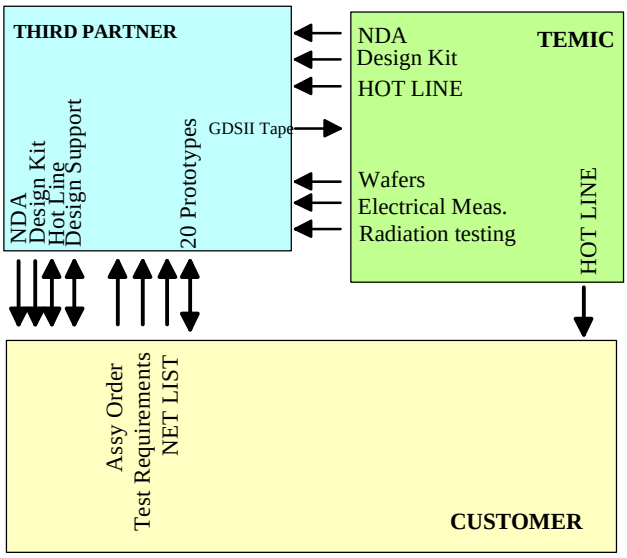
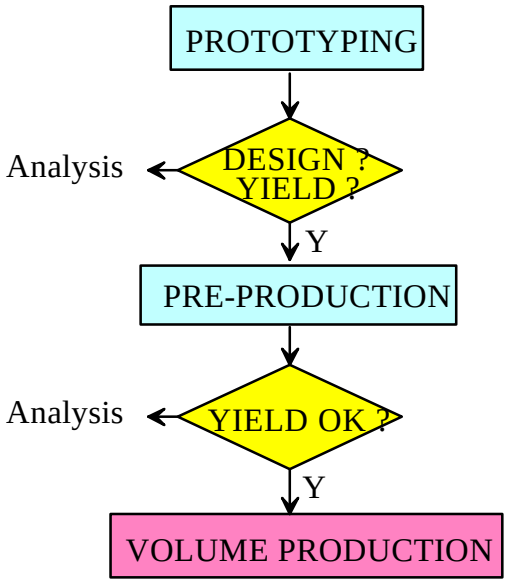
MPW Prototyping

Prototyping is required for validating new functions or architectures. It also allows assessing yield values before large scale production. Cost reduction is achieved by sharing the non-recurring expenses of mask and wafer manufacturing between several users. Multi Project Wafers (MPW) activity is available through a third partner, who also offers front-end and back-end services. The standard offer is the delivery of 10 to 20 untested prototypes with the wafer batch electrical measurements values. Production of MPWs will begin early in 1997.



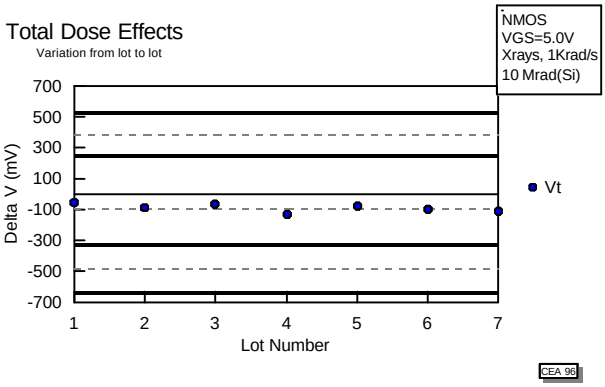


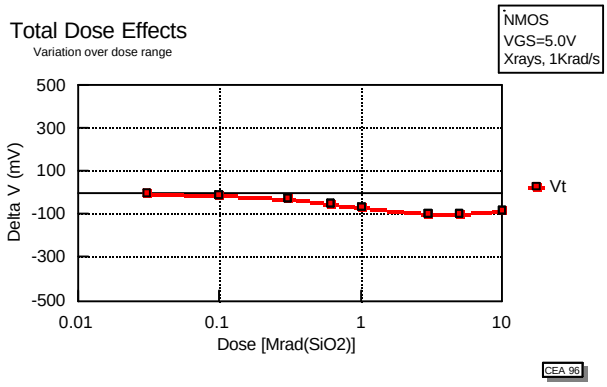
Manufacture

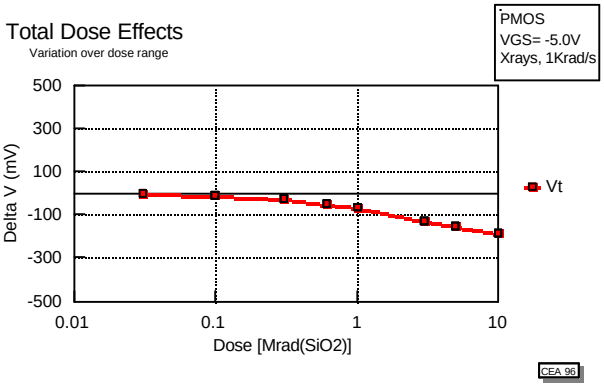
Designer has access to electrical parameters and Topological rules. He provides TEMIC with a GDSII tape including all information required for circuit manufacture. After level checks (minimum size and pitch), reticules are fabricated and production starts at MHS. The wafers are inspected before delivery to ensure they meet electrical specifications. Unless it is not required, radiation hardness is checked up to 10Mrad or more by exposure of the components to Xrays. Eelectrical and dimensional measurement are provided with the wafers .

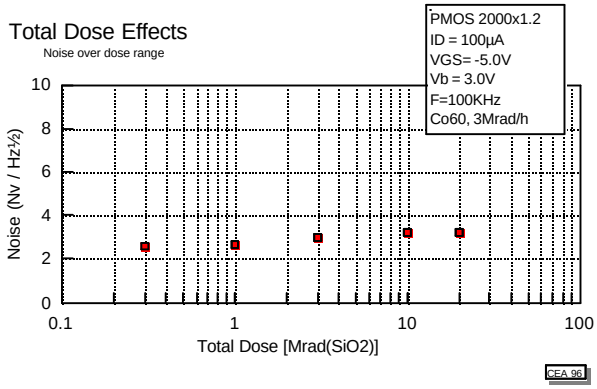
Radiation assurance

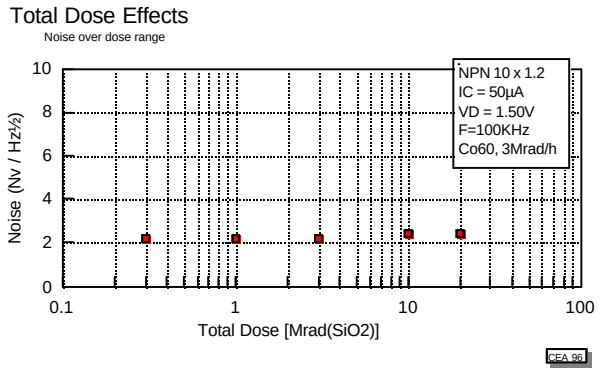
To provide radiation assurance, the variation of each radiation-sensitive parameter with dose is monitored by the irradiation of test structures up to 10Mrad on a Statistical Process Control basis. In addition, regular extended irradiation tests, including neutron and post-irradiation effects, are made to verify functionality and noise performances on specific mixed analog/digital test structures.

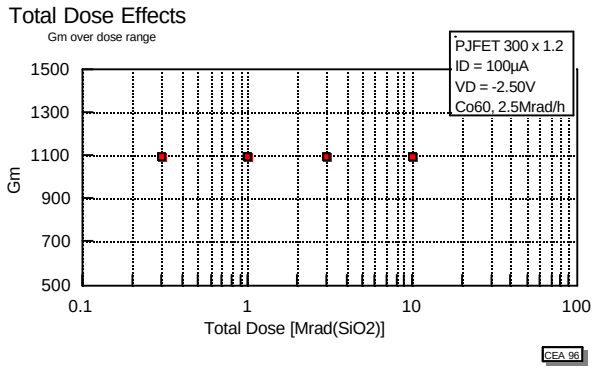












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