Dot matrix LCD controller/driver
BU97711

The BU97711 is a character display LCD controller/driver that has a key scan function and an LED display. The IC can display 10 characters in one or two lines. With a serial interface control circuit and an LCD drive power supply circuit, the IC allows configuration of a compact application.

●Applications

Cellular phones, fax machines, printers, and audio systems

●Features

1) 4-line serial interface control.
2) 6 × 6 key matrix interface.
3) 3 bit LED driver.
4) Data of 240 characters installed.
5) 8 characters can be defined by the user.
6) Up to 50 segments can be displayed.
7) LCD drive power supply circuit.
8) Operation with low voltage and low power dissipation is possible.

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit
Power supply voltage 1	V_{DD}	−0.3～+7.0	V
Power supply voltage 2	V_{LCD}	−0.3～+7.0	V
Power dissipation	Pd	1000*1	mW
		1500*2	
Operating temperature	Topr	−20～+75	℃
Storage temperature	Tstg	−55～+125	℃

*1 Data refers to Independent IC; power dissipation drops by 10mW for every 1℃ above 25℃.
*2 When a 70mm x 70mm x 1.6mm board is mounted; power dissipation drops by 15mW for every 1℃ above 25℃.

●Recommended operating conditions (Ta=25℃, V_{SS}=0V)

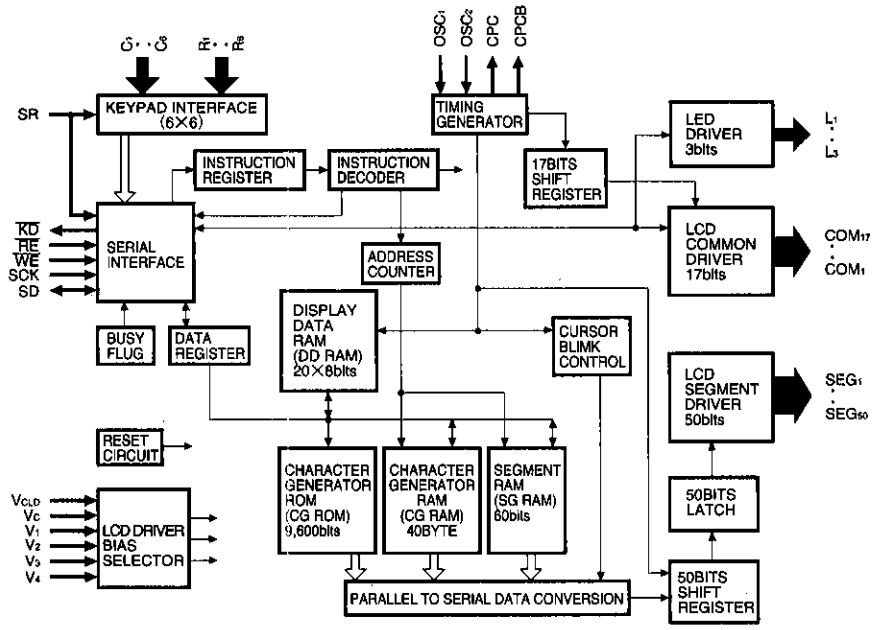
Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage 1	V_{DD}	2.7	−	5.5	V
Supply voltage 2 *3	V_{LCD}	2.7	−	6.0	V
Oscillation frequency *4	fosc	40	70	100	kHz
Key contact resistance	R_{KC}	0	−	5	kΩ

*3 Should satisfy $V_{LCD} \geqq V_C \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{SS}$
*4 Rf=2.2MΩ

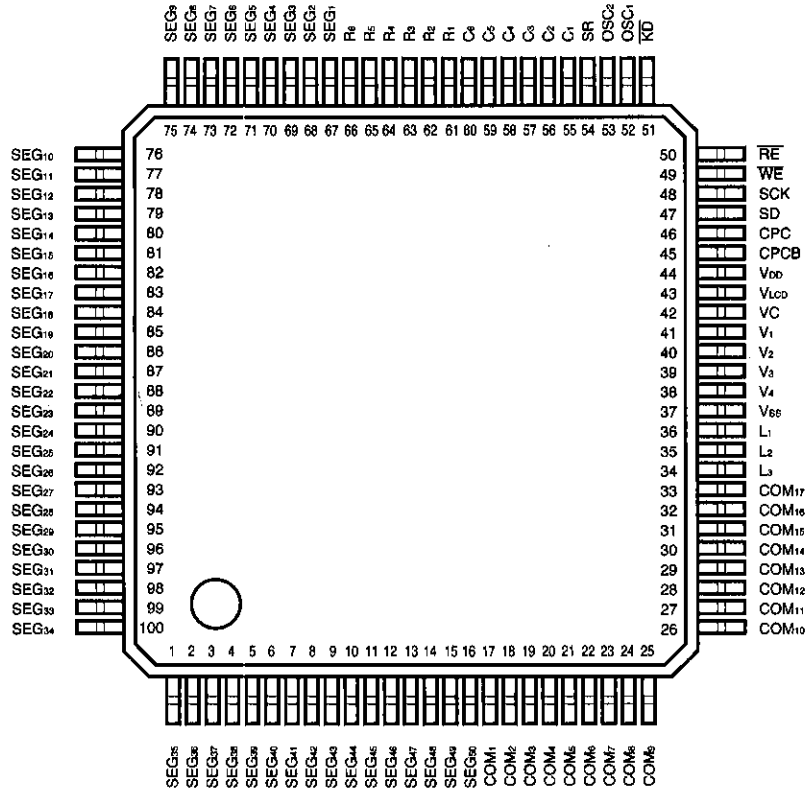
●Model name list

Model Number	Built-in font
BU97711−00	ROM Ver.00

●Block diagram



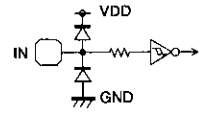
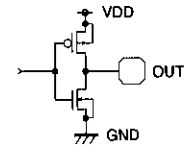
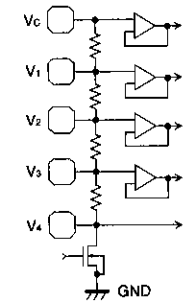
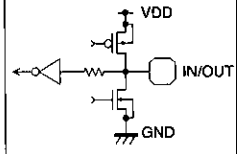
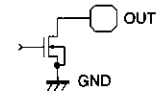
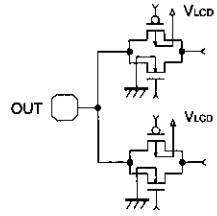
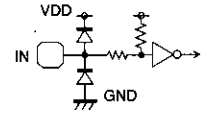
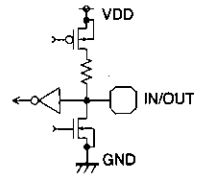
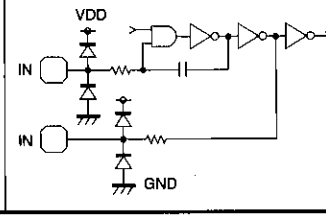
●Pin layout



●Pin descriptions

Pin NO.	Pin name	Type	Function
L_1~L_3	36~34	O	Output pins for the LED drive; output FET is turned ON when "1" is written to the LED register, and the output FET and the LED are turned OFF when "0" is written to the LED register
COM_{17}~COM_1	33~17	O	Output pins for the LCD drive; connected to the common terminal of the LCD panel; all the pins output at the V_{LCD} level when the display is OFF
SEG_{50}~SEG_1	16~1 100~67	O	Segment output pins for the LCD drive; connected to the segment terminal of the LCD panel; all the pins output at the V_{LCD} level when the display is OFF
R_1~R_6 C_1~C_6	61~66 55~60	I/O	Keypad output pins; a keypad (up to 6 X 6) can be configured with single contact key switches
OSC_1 OSC_2	52 53	I O	Internal oscillator I/O pins; connect a resistor between the pins when the internal clock is operating; input from OSC_1 and leave OSC_2 open when the external clock is operating
$\overline{KD}$	51	O	Key press-down output pin; after a key is pressed down, the output is LOW level with the ON debounce effective; after a key is released, the output is ZERO (high impedance) with the OFF debounce effective
$\overline{RE}$	50	I	Read enable input pin; read mode at LOW level; data is read to the output serial register at the signal falling edge
$\overline{WE}$	49	I	Light enable input pin; light mode at LOW level; data is read to the register at the signal rising edge when writing data to the LED port
SCK	47	I	Shift clock input pin for serial data; data is read bit-by-bit from the SD pin at the signal rising edge when $\overline{RE}$ is LOW level; data is written bit-by-bit from the SD pin at the signal falling edge when $\overline{WE}$ is LOW level
SD	48	I/O	Serial data I/O pin; data format-related data is input and output; $\overline{RE}$ is LOW level and $\overline{WE}$ is HIGH level in the data output mode; "Z" (high impedance) if not in the output mode
SR	54	I	Input pin for clearing the standby mode; input is possible even when $\overline{RE}$ and $\overline{WE}$ are both LOW level; the standby mode is released at LOW level; because the resistance is pulled up, the standby release key is configured by connecting a single contact key switch to V_{SS}
CPC CPCB	46 45	O	Output pin for booster circuit drive; booster power supply for V_{LCD} an be configured with external diodes and capacitors
V_{LCD} V_1~V_4	43 41~38		LCD power supply pin; should satisfy (High) $V_{LCD} \geqq V_C \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{SS}$ (Low)
V_C	42		Contrast adjustment pin
V_{DD}	44		V_{DD} pin
V_{SS}	37		V_{SS} pin

●Input/output circuit

Pin name	I/O	Equivalent circuit	Pin name	I/O	Equivalent circuit	Pin name	I/O	Equivalent circuit
SCK, WE, RE	IN		CPC, CPCB	OUT		V_C V_1 V_2 V_3 V_4		
SD	IN/ OUT		$\overline{KD}$ L_1 L_2 L_3	IN				
SEGn COMn	OUT		SR	IN				
Rn Cn	IN/ OUT		OSC_1 OSC_2					

●Electrical characteristics

DC characteristics (unless otherwise noted, V_{DD}=2.7~5.5V, V_{SS}=0V, and Ta=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Pin.
HIGH level input voltage	V_{IH1}	0.8×V_{DD}	—	V_{DD}	V		OSC_1,$\overline{RE}$,$\overline{WE}$, SCK,SD,SR, R_1~R_8 C_1~C_8
LOW level input voltage	V_{IL1}	0	—	0.2×V_{DD}	V		
COM driver ON resistance	R_{COM}	—	—	20	kΩ	Id=±50μA	$COM_{1\sim17}$
SEG driver ON resistance	R_{SEG}	—	—	30	kΩ	Id=±50μA	$SEG_{1\sim50}$
Input current	I_{IN1}	−1	—	1	μA	V_{IN}=0~V_{DD}	$\overline{RE}$,$\overline{WE}$,SCK,SD
HIGH level output voltage 1	V_{OH1}	0.8×V_{DD}	—	—	V	I_{OH}=−100μA	SD
LOW level output voltage 1	V_{OL1}	—	—	0.2×V_{DD}	V	I_{OL}=100μA	SD,$\overline{KD}$
LOW level output voltage 2	V_{OL2}	—	—	0.7	V	V_{DD}=5V, I_{OL}=60mA	L_1,L_2
		—	—	0.9	V	V_{DD}=3V, I_{OL}=60mA	
LOW level output voltage 3	V_{OL3}	—	—	0.5	V	V_{DD}=5V, I_{OL}=10mA	L_3
		—	—	0.7	V	V_{DD}=3V, I_{OL}=10mA	
Current consumption	I_{DD}	—	35	60	μA	f_{OSC}=70kHz, without load	V_{DD}
		—	—	2	μA	Standby mode	

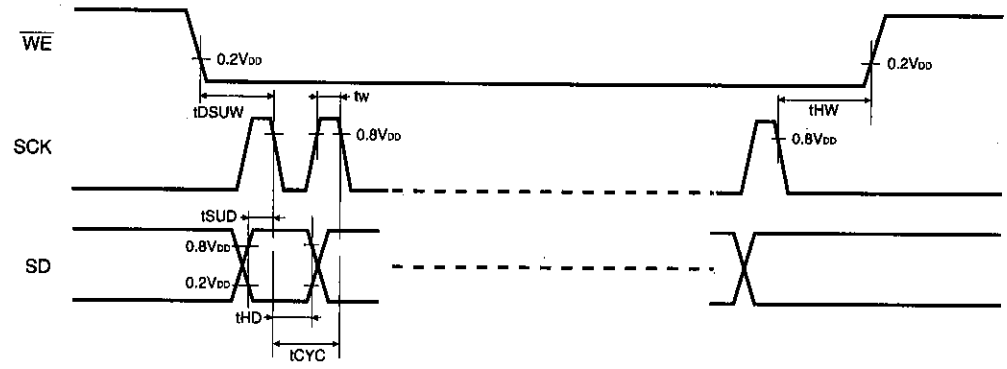
AC characteristics (unless otherwise noted, V_{DD}=2.7~5.5V, V_{SS}=0V, and Ta=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Clock (fosc) characteristics						
Operating frequency	f_{IN}	—	—	200	kHz	External clock operating
Clock duty ratio	f_{Duty}	45	50	55	%	
Clock rise time	t_r	—	—	100	ns	
Clock fall time	t_f	—	—	100	ns	
Serial interface timing characteristics						
SCK cycle time	f_{CYC}	400	—	—	ns	
SCK pulse width	fw	100	—	—	ns	

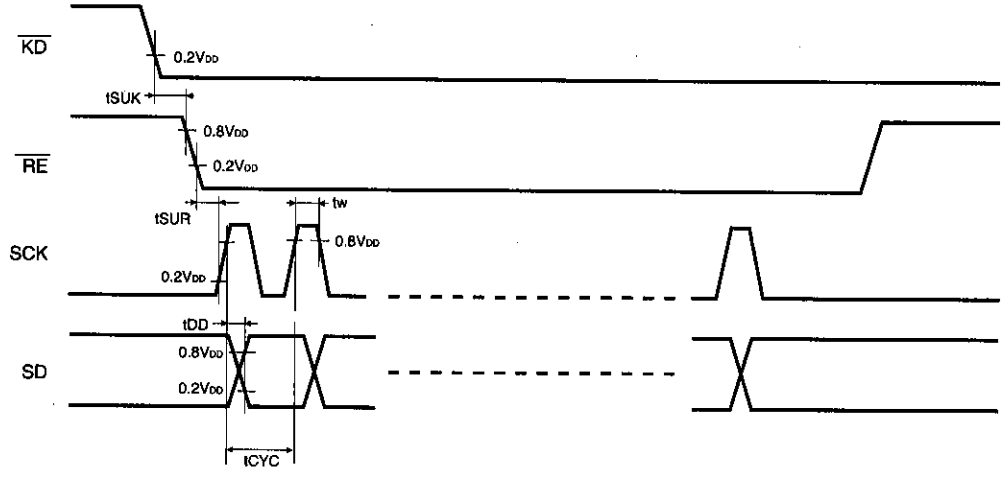
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Setup time 1	t_{SUW}	100	—	—	ns	$\overline{WE}$→SCK
Setup time 2	t_{SUD}	100	—	—	ns	SD→SCK
Setup time 3	t_{SUR}	100	—	—	ns	$\overline{RE}$→SCK
Setup time 4	t_{SUK}	100	—	—	ns	$\overline{KD}$→$\overline{RE}$
Hold time 1	t_{HW}	100	—	—	ns	SCK→$\overline{WE}$
Hold time 2	t_{HD}	100	—	—	ns	SCK→SD
SD output delay time	t_{DO}	--	—	150	ns	SCK→SD,CL=30pF
Key interface characteristics						
Key ON debounce time	t_{DBN}	--	1500/fosc	—	s	B1=1,B2=0,B3=0
		--	800/fosc	—	s	B1=0,B2=1,B3=0
		—	400/fosc	—	s	B1=0,B2=0,B3=1
Key OFF debounce time	t_{DBF}	--	2400/fosc	—	s	B1=1,B2=0,B3=0
		--	1400/fosc	—	s	B1=0,B2=1,B3=0
		--	650/fosc	—	s	B1=0,B2=0,B3=1
Power supply characteristics when reset						
Power supply rise time	trcc	0.05	—	10	ms	
Power supply fall time	toff	1	—	—	ms	

●Interface timing

○Serial data input timing

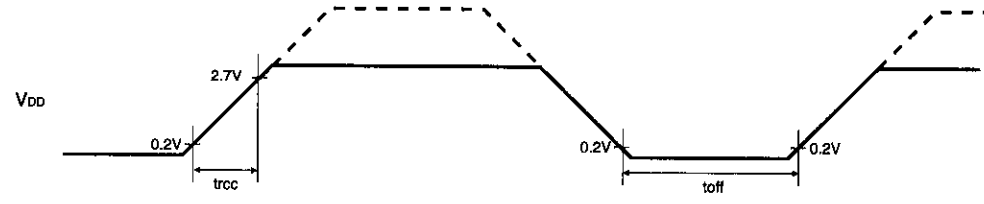


○Serial data output timing



Power supply characteristics

When initialization is carried out in the internal reset circuit at start-up, the power supply characteristics described below should be satisfied.



●Data format

Serial data is transferred by a 4-line clock synchronous communication system. The I/O of serial data is synchronized with SCK. The following modes are selected according to the status of $\overline{RE}$ and $\overline{WE}$. Either data input or output is carried out sequentially from MSB.

$\overline{RE}$	$\overline{WE}$	Operating mode
H	H	Normal (waiting for instruction) Stop when SCK is LOW
H	L	Write mode
L	H	Read mode
L	L	Standby mode

Serial data is input and output as 16-bit data. Execution of each instruction starts after the transfer of the final bit is confirmed. While an instruction is executed, no command can be executed except "SR / BF / key data read," "SR/BF/LED register read," and "LED register write." The busy flag is "1" (busy state) until the end of an instruction. Therefore, the MPU has to confirm that the busy flag is "0" (not busy) before sending an instruction to BU97711.
If a next instruction is successively transferred without checking the busy flag, a transfer wait time longer than the instruction execution time is needed. A next instruction is ignored if the last bit of the instruction is received while a previous instruction is being executed.

Note: The $\overline{RE}$ and $\overline{WE}$ pins must be in the normal sate ($\overline{RE}$=$\overline{WE}$="H") and the SCK pin must be LOW before executing an instruction.

●List of instructions

Instruction	Code																Function	Execution time (fosc=70kHz)
	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1		
Standby mode clear	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Clears the standby mode; oscillation starts and all instructions become executable	0S
KEY SCAN timing set	0	0	0	0	0	0	0	0	0	0	0	0	1	B3	B2	B1	Sets ON and OFF debounce times when a key is pressed down	143us
Display clear	0	0	0	0	0	0	0	0	0	0	1	L	SG	*	*	*	LCD is cleared and the DDRAM address 0 is set to the address counter	286us
Return home	0	0	0	0	0	0	0	0	0	1	*	*	*	*	*	*	DDRAM address 0 is set to the address counter, display shift is cleared,and DDRAM contents are unchanged	286us
Entry mode set	0	0	0	0	0	0	0	0	1	I/D	S	*	*	*	*	*	Sets the cursor direction and the display shift; carries out the operation designated during RAM data writing	143us
Display ON/OFF	0	0	0	0	0	0	0	1	D	C	B	R	*	*	*	*	Sets LCD ON/OFF, cursor ON/OFF, and blink/inversion of the cursor position character	143us
Cursor/display shift	0	0	0	0	0	0	1	S/C	R/L	*	*	*	*	*	*	*	Shifts the cursor movement and the display without changing the DDRAM contents	143us
Display mode set	0	0	0	0	0	1	N	*	*	*	*	*	*	*	*	*	Sets one- or two-line display mode	143us
SGRAM address set	0	0	0	0	1	ADDRESS				*	*	*	*	*	*	*	Sets the SGRAM address; the data to be followed is SGRAM data	143us
DDRAM address set	0	0	0	1	ADDRESS					*	*	*	*	*	*	*	Sets the DDRAM address; the data to be followed is DDRAM data	143us
CGRAM address set	0	0	1	ADDRESS						*	*	*	*	*	*	*	Sets the CGRAM address; the data to be followed is CGRAM data	143us
SR/BF/ key data read	SR	BF	R6	R5	R4	R3	R2	R1	C6	C5	C4	C3	C2	C1	0	0	Reads SR pin status, BF status that indicates internal operation, and key data	0S
LED register write	1	0	*	*	*	*	*	*	*	*	*	*	*	L3	L2	L1	Controls LED port ON/OFF; ON when "1"	0S
CG/DD/SGRAM data write	1	1	*	*	*	*	*	*	RAM WRITE DATA								Writes data to the CGRAM, DDRAM, or SGRAM	143us

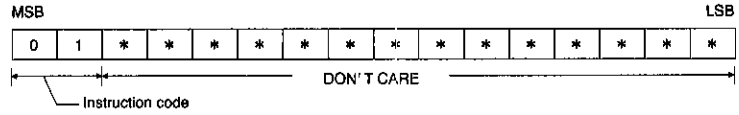
Key interface timing is set by B1, B2, and B3

B1	B2	B3	ON debounce time	OFF debounce time
1	0	0	1500/fosc	2400/fosc
0	1	0	800/fosc	1400/fosc
0	0	1	400/fosc	650/fosc

LED register is cleared when L = 1 / LED register is not cleared when L = 0
SGRAM is cleared when SG = 1 / SGRAM is not cleared when SG = 0
Increment when I/D = 1 / Decrement when I/D = 0
Display shifted when S = 1 / Display not shifted when S = 0
Display ON when D = 1
Cursor ON when C = 1
When B = 1, blink ON if R = 0 and inversion ON if R = 1
When B = 0, blink and inversion are both OFF regardless of R
Display shifted when S/C = 1 / Cursor moved when S/C = 0
Shift right when R/L = 1 / Shift left when R/L = 0
When N = 1, display is 2 lines / One-line display when N = 0
Internally operating when BF = 1 / Instruction acceptable when BF = 0

●Circuit operation

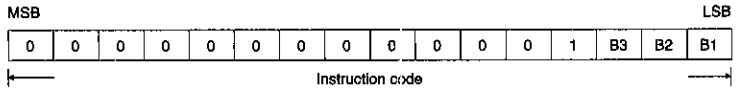
○ Standby mode clear ($\overline{RE}$ = HIGH, $\overline{WE}$ = LOW) Execution time : 0s



The instruction clears the standby mode. Oscillation starts and all instructions become executable. Display is turned OFF, and the bias current path is shut down.
Execute this instruction prior to any other instructions because the BU97711 is in the standby mode at start-up.

Note: This instruction is acceptable only during the standby mode. The instruction will be ignored if the mode is not standby.

○ Key scan timing set ($\overline{RE}$ = HIGH, $\overline{WE}$ = LOW) Execution time : 10/fosc (286 μs when fosc = 70kHz)

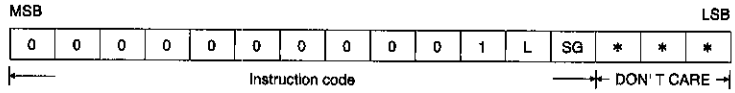


Sets ON and OFF debounce times when a key is pressed down.

B1	B2	B3	ON debounce time	OFF debounce time
1	0	0	1500 / fosc	2400 / fosc
0	1	0	800 / fosc	1400 / fosc
0	0	1	400 / fosc	650 / fosc

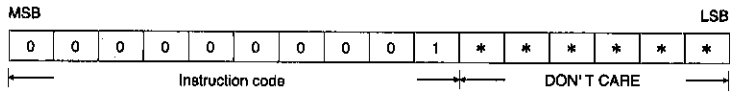
At start-up, the ON debounce time is set to 1500/fosc, and the OFF debounce time is set to 2400/fosc.

○ Display clear ($\overline{RE}$ = HIGH, $\overline{WE}$ = LOW) Execution time : 20/fosc (286 μs when fosc = 70kHz)



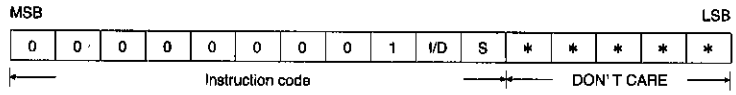
The space code (20H) is written to all the DDRAM addresses (when rewriting the ROM, "20H" must be allocated to the space code).
The DDRAM address 0 is set to the address counter. The display is cleared, and the cursor/blink moves to the first position (first position of the first line in the case of two-line display mode)
When L = 1, "0" is written to the LED register and the LED is turned off.
When L = 0, the states of the LED register and the LED port do not change.
When SG = 1, "00H" is written to all the SGRAM addresses.
When SG = 0, the SGRAM contents do not change.

○ Return home ($\overline{RE}$ = HIGH, $\overline{WE}$ = LOW) Execution time : 20/fosc (286 μs when fosc = 70kHz)



The DDRAM address 0 is set to the address counter. If shifted, the display reverts to the home position. The DDRAM contents are not changed.
The cursor/blink moves to the first position (first position of the first line in the case of two-line display mode)

○ Entry mode set ($\overline{RE}$ = HIGH, $\overline{WE}$ = LOW) Execution time : 10/fosc (143 μs when fosc = 70kHz)



I/D : When writing character codes to the DDRAM, each DDRAM address is set to either +1 (I/D = 1) or -1 (I/D = 0).
When I/D = 1, the cursor/blink moves to the right.
When I/D = 0, the cursor/blink moves to the left.
The same rule applies when writing data to the CGRAM or SGRAM.

S : When S = 1 and I/D = 1, all the displayed data is shifted to the left while data is written to the DDRAM.
When S = 1 and I/D = 0, all the displayed data is shifted to the right. This means the cursor appears stable while characters are shifted.
When S = 0, the display does not shift.

○ Display ON/OFF ($\overline{RE}$ = HIGH, $\overline{WE}$ = LOW) Execution time : 10/fosc (143 μs when fosc = 70kHz)

MSB															LSB
0	0	0	0	0	0	0	1	D	C	B	R	*	*	*	*
← Instruction code												→ DON'T CARE →			

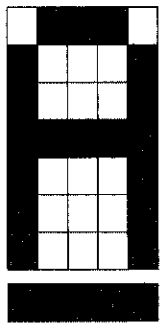
D : The display is turned ON when D = 1. The display is turned OFF and the bias current path of the LCD power supply is shut down when D = 0. Because the DDRAM contents are not changed when the D is reset, the display reverts to the original state when D is set.

C : The cursor is shown when C = 1 and not shown when C = 0. The cursor is presented as five consecutive dots of the eighth line.

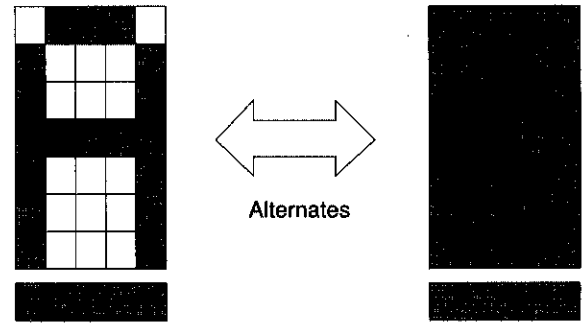
B, R : When R = 0 and B = 1, the character of the cursor position blinks.
When R = 1 and B = 1, the character of the cursor position is inverted periodically. In this case, the cursor and blink are not displayed.
When R = 1 and B = 0, the display complies with the states of D and C.

The blink and inversion displays have a period of 411ms when fosc = 70kHz. They can be set simultaneously.

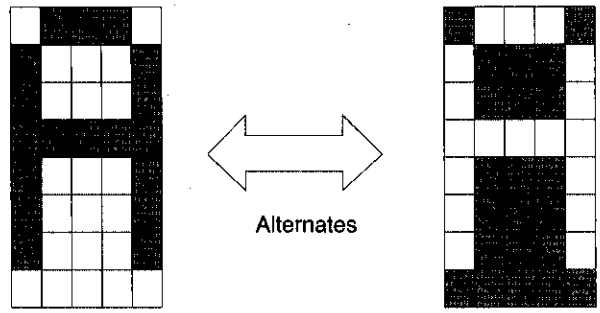
• Examples of cursor, blink, and inversion displays



(a) Cursor

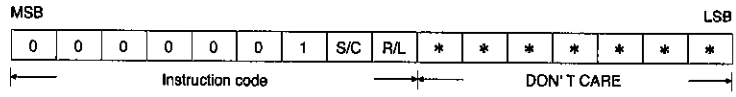


(b) Blink



(c) Inversion

○ Cursor shift ($\overline{RE}$ = HIGH, $\overline{WE}$ = LOW) Execution time : 10/fosc (143 μs when fosc = 70kHz)

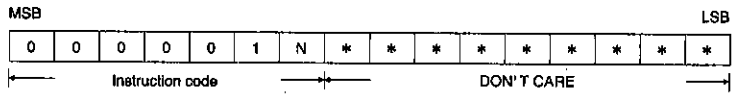


The cursor or the displayed data is moved to the right or left without writing data. In the case of two-line display mode, the cursor moves from the tenth character of the first line to the first character of the second line, and the displayed data is shifted only in the horizontal direction (first and second lines are not exchanged).

S/C : When S/C = 0, only the cursor is shifted.
When S/C = 1, only the displayed data is shifted and the cursor moves together with the characters. The address counter contents are not changed.

R/L : When R/L = 0, the cursor or the displayed data is shifted to the left.
When R/L = 1, the cursor or the displayed data is shifted to the right.

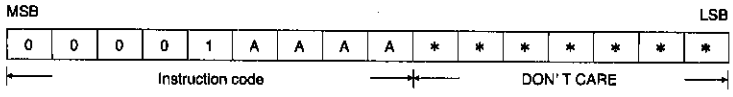
○ Display set mode ($\overline{RE}$ = HIGH, $\overline{WE}$ = LOW) Execution time : 10/fosc (143 μs when fosc = 70kHz)



N : One-line mode when N = 0 (duty ratio is 1/9)
Two-line mode when N = 1 (duty ratio is 1/17)

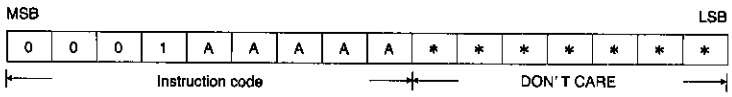
Note: Execute this instruction at the beginning of a program before executing any other instructions.
This instruction cannot be executed after "standby mode clear," "SR/BF/key data read," or "LED register write" (except commands).

○ SGRAM address set ($\overline{RE}$ = HIGH, $\overline{WE}$ = LOW) Execution time : 10/fosc (143 μs when fosc = 70kHz)



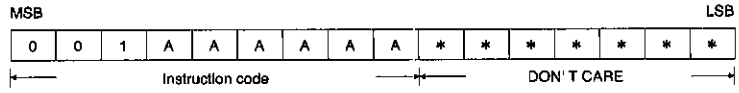
The binary data "AAAA" is set to the SGRAM address counter. After this instruction, RAM data from the MPU is written to the SGRAM.

○ DDRAM address set ($\overline{RE}$ = HIGH, $\overline{WE}$ = LOW) Execution time : 10/fosc (143 μs when fosc = 70kHz)



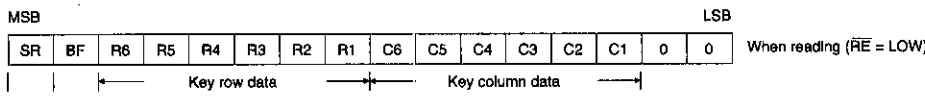
The binary data "AAAAA" is set to the DDRAM address counter. After this instruction, RAM data from the MPU is written to the DDRAM.

○ CGRAM address set ($\overline{RE}$ = HIGH, $\overline{WE}$ = LOW) Execution time : 10/fosc (143 μs when fosc = 70kHz)



The binary data "AAAAAA" is set to the CGRAM address counter. After this instruction, RAM data from the MPU is written to the CGRAM.

○ SR/BF/key data read ($\overline{RE}$ = HIGH to LOW, $\overline{WE}$ = LOW) Execution time : 0s



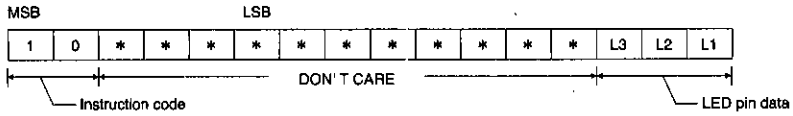
SR : The state of the SR pin is output : SR = 1 when a key is pressed down (LOW level), and SR = 0 when a key is released (HIGH level).

BF : The busy flag is output. The internal operation mode is indicated when BF = 1. Adjust the transfer rate so that the last bit of a next instruction will be received after BF is changed to "0."

R1~R6, C1~C6 : Key data outputs. "1" is output if a key is pressed down, and "0" is output if a key is pressed down (LOW level). The last 2 bits are read as "0."

Note: This instruction is executable even when the internal operation is busy.
The same readout sequence applies when data is successively read with RE = LOW. Data is renewed after each 16-bit batch is transferred.

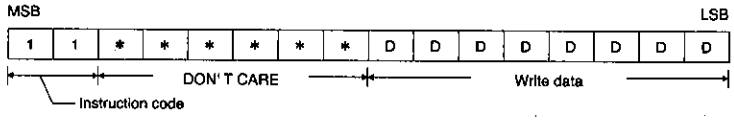
○ LED register write ($\overline{RE}$ = HIGH, $\overline{WE}$ = LOW to HIGH) Execution time : 0s



L1~L3 : LED control data inputs. Light is on when "1", and off when "0." Data is input with $\overline{WE}$ = LOW, and written to the LED register at the $\overline{WE}$ rising edge.

Note: When rewriting LED data, not only the relevant bit but all bits should be renewed.
This instruction is executable even during the standby mode or the internal operation busy mode.

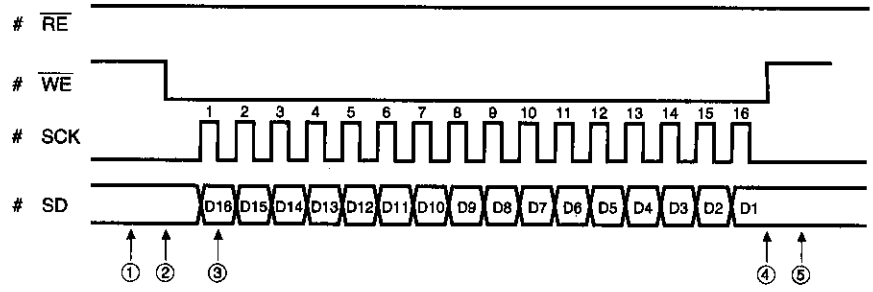
○ CG/DD/SGRAM data write ($\overline{RE}$ = HIGH, $\overline{WE}$ = LOW)
Execution time : 10/fosc (143 μs when fosc = 70kHz)



The binary 8-bit data "DDDDDDDD" is written to the CGRAM, DDRAM or SGRAM. The last 3 bits are ignored when writing data to the CGRAM.
The selection of the CGRAM, DDRAM, or SGRAM is determined by the CG/DD/SGRAM address set command that has been executed before this instruction.
The execution of the address set command does not have to be right before the write command.
Each address is automatically set to +1 or -1 according to the entry mode. The display shift complies with the entry mode.
When writing data successively with RE and WE being fixed, only 8-bit RAM data is input after the first input.

Note: When rewriting RAM data, not only the relevant bit but all bits should be renewed.
When writing data successively, a transfer wait time longer than the instruction execution time is required after each 8-bit batch is input.

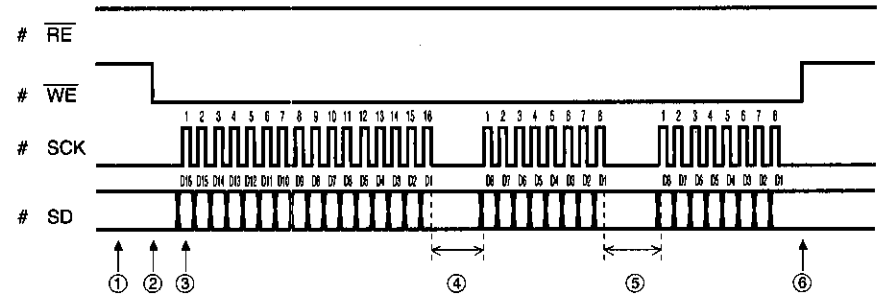
●Recommended procedures of data I/O
○Serial input of control and write commands



State	CPU operation (#)
①	$\overline{RE}$ = HIGH, $\overline{WE}$ = HIGH, and SCK = LOW during the standby mode
②	Set $\overline{WE}$ to LOW (write mode)
③	Serial data is input to SD in synchronization with the SCK falling
④	After write data is transferred (16-bit data, or 8-bit data after the first input in successive writing), the write mode is ended by setting $\overline{WE}$ to HIGH level LED data is latched if the LED write command is executed
⑤	The wait time should be longer than the instruction execution time

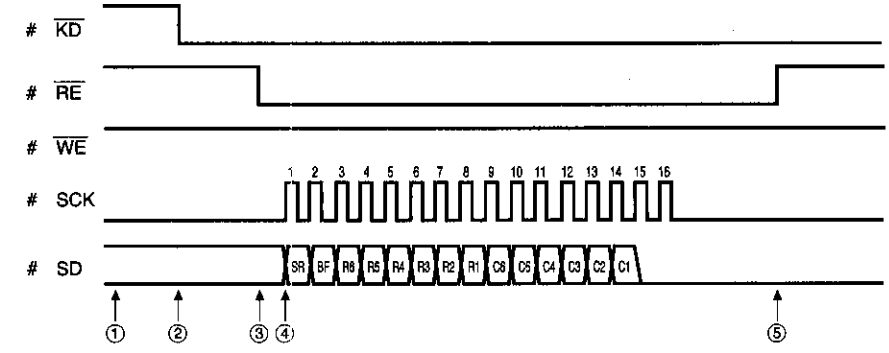
* The order of ④ and ⑤ can be exchanged.

○Serial input for the successive write command (RAM writing)



State	CPU operation (#)
①	$\overline{RE}$ = HIGH, $\overline{WE}$ = HIGH, and SCK = LOW during the standby mode
②	Set $\overline{WE}$ to LOW (write mode)
③	Serial data is input to SD in synchronization with the SCK falling
④⑤	After write data is transferred to the allocated addresses, wait for a period longer than the instruction execution time.
⑥	After the transfer of data, set $\overline{WE}$ to HIGH to end the write mode, and wait for a period longer than the instruction execution time.

○Serial I/O for the read command



State	CPU operation (#)	BU97711 operation
①	$\overline{RE}$ = HIGH, $\overline{WE}$ = HIGH, and SCK = LOW during the standby mode	
②		$\overline{KD}$ is set to LOW by pressing down a key
③	Set $\overline{RE}$ to LOW (read mode)	Readout data is set
④	SCK rising edges are provided sequentially	Serial data is output sequentially from SD
⑤	End the read mode by setting $\overline{RE}$ to HIGH	

●Standby mode

○ Standby mode setting

The standby mode is set with $\overline{RE}$ = LOW and $\overline{WE}$ = LOW. The standby mode has the following characteristics :

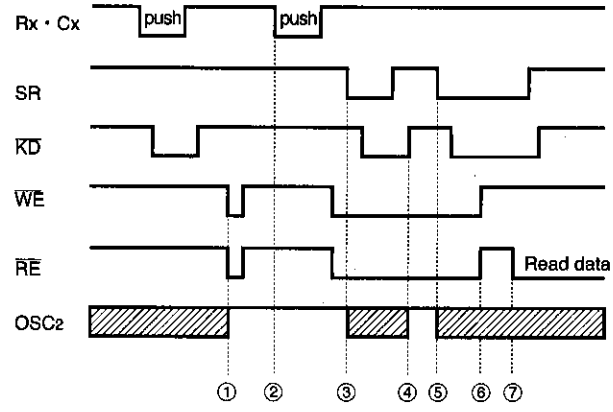
- Oscillation stops and the circuit current is reduced to a very low level.
- The display data goes out together with the blink/inversion display.
- The space code "20H" is written to all DDRAM addresses.
- The DDRAM address 0 is set to the address counter.
- LCD output is set to the V_{LCD} level, and the bias current path is shut down.
- Only the SR key is available for key input. No input from the keypad is accepted.
- Whether the SGRAM contents are cleared depends on the D4 value of the instruction code in the command right before RE and WE are set to LOW. The contents are cleared and not cleared when D4 is "1" and "0", respectively.
- The LED port state is unchanged.

○ Standby mode clearing

- The standby mode is cleared by the standby mode clear command.
- The standby mode is cleared immediately by setting SR to LOW unless $\overline{RE}$ and $\overline{WE}$ are both LOW.
- If SR is set to LOW with $\overline{RE}$ and $\overline{WE}$ both LOW, oscillation starts without clearing the standby mode. Oscillation stops if SR is reverted to HIGH (if the SR key is ON debounce effective and the KD output is LOW level, oscillation continues until the OFF debounce is effective).

Note: If the SGRAM has not been cleared in the standby mode, set the SGRAM before clearing the standby mode and turning on the display.

○ Example of standby mode setting



①The standby mode is set and oscillation stops when $\overline{RE}$ and $\overline{WE}$ are both set to LOW.

②No input from the keypad is accepted in the standby mode.

③Oscillation starts even in the standby mode when the SR pin is set to LOW level (SR = LOW takes precedence over $\overline{RE}$ = LOW and $\overline{WE}$ = LOW).

④When the SR pin is set to HIGH level, oscillation stops and the standby mode continues as long as $\overline{RE}$ = LOW and $\overline{WE}$ = LOW.

⑤Oscillation starts even in the standby mode by setting the SR pin to LOW level.

⑥Because $\overline{RE}$ and $\overline{WE}$ are not both LOW anymore, the standby mode is cleared, and oscillation continues even when the SR pin is set to HIGH.

⑦The state of SR = LOW is set to the serial register at the $\overline{RE}$ falling edge, so that the data becomes readable.

●Functions

○ Register

The BU97711 has two 8-bit registers : one is an instruction register (IR) and the other is a data resistor (DR).
The IR stores instruction codes and address data of the data display RAM (DDRAM), the character generator RAM (CGRAM), and the segment RAM (SGRAM). The MPU can write data to the IR but cannot read data from the IR.
The DR temporarily stores read/write data of the DDRAM, CGRAM, and SGRAM. In the write mode, the data in the DR is automatically written to the DDRAM, CGRAM, and SGRAM. In the read mode, the address data written by the IR is automatically read from the DDRAM, CGRAM, and SGRAM by the DR, so that the MPU can read data from the DR.
After the MPU has read data from the DR, each address is set to either +1 or -1 for the next readout.

○ Busy flag (BF)

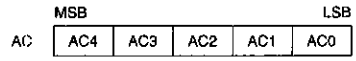
The busy flag is set during the execution of an instruction. The BU97711 does not accept any instruction during the busy state (exemptions are the busy flag read command and the LED write command). The busy flag has to be cleared before sending an instruction.

○ Address counter (AC)

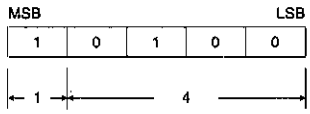
The address counter (AC) shows the addresses of the DDRAM, CGRAM, and SGRAM. When a RAM address setting instruction is written to the IR, the address data is automatically transferred from the IR to the AC. Simultaneously, selection of DDRAM, CGRAM, and SGRAM is made according to the instructions. The AC is set to +1 or -1 after the data is read from or written to the DDRAM, CGRAM, and SGRAM.

○ Display data RAM (DDRAM)

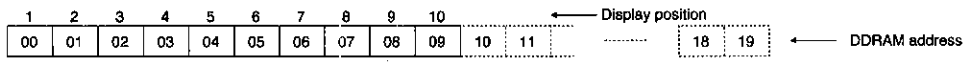
The display data RAM (DDRAM) stores 8-bit character codes. The storage capacity is 20 8-bit characters. The relationship between the DDRAM address and the display position is described in the following.
A DDRAM address is set to the address counter as a hexadecimal number.



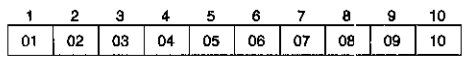
Example : when the DDRAM address is "14"



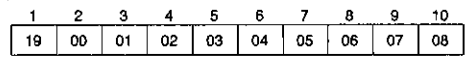
(1) Relationship between the DDRAM address and the display position in the one-line display mode (N = 0)



The eleventh character of the DDRAM address is "10."
When the display data is shifted, the display position is related to the DDRAM address as follows.



Display left shift



Display right shift

(2) Relationship between the DDRAM address and the display position in the two-line display mode (N = 1)

	1	2	3	4	5	6	7	8	9	10	
	← Display position										
1-line display	00	01	02	03	04	05	06	07	08	09	← DDRAM address
2-line display	10	11	12	13	14	15	16	17	18	19	

When the display data is shifted, the display position is related to the DDRAM address as follows.

1	2	3	4	5	6	7	8	9	10
01	02	03	04	05	06	07	08	09	00
11	12	13	14	15	16	17	18	19	10

Display left shift

1	2	3	4	5	6	7	8	9	10
09	00	01	02	03	04	05	06	07	08
19	10	11	12	13	14	15	16	17	18

Display right shift

○ Character generator ROM (CGROM)

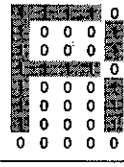
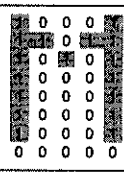
The character generator ROM (CGROM) generates character patterns (5 × 8 dots × 240 characters) from 8-bit character codes. The character codes and the character patterns are shown in Table 4 (List of character codes and character patterns, ROM Ver. 00).

The user can change the ROM contents and define new character patterns.

○ Character generator RAM (CGRAM)

The character generator RAM (CGRAM) is used for displaying user-defined character patterns (5 × 8 dots × 8 characters).

The character code, the CGRAM address, and the character pattern are related to each other as follows.

Character code (DDRAM Data)		CGRAM address		Character pattern (CGRAM Data)	
7 6 5 4 3 2 1 0		5 4 3	2 1 0	4 3 2 1 0	
0 0 0 0 * 0 0 0		0 0 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1		Character pattern
			0 0 0 0 0 1		
			1 1 0 1 1 1		
0 0 0 0 * 1 1 1		1 1 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1		* Invalid

Note 1. The character code bits 0-2 correspond to the CGRAM address bits 3-5.

2. The CGRAM address bits 0-2 indicate the line number of a character pattern. The eighth line is given as either the cursor or the display data. Because the eighth line data overlaps with the cursor, the data has to be "0" in order to distinguish the cursor. The cursor cannot be distinguished if the eighth line data is "1."
3. The CGRAM character code is selected when the character code bits 4-7 are all "0." The character code bit 3 is invalid. The character codes 00H and 08H have the same character pattern.
4. "1" and "0" correspond to data ON and OFF, respectively.

○ Character codes and character patterns (ROM Ver. 00)

Upper 4 bit / Lower 4 bit	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
XXXX0000	CGRAM (1)															
XXXX0001	(2)															
XXXX0010	(3)															
XXXX0011	(4)															
XXXX0100	(5)															
XXXX0101	(6)															
XXXX0110	(7)															
XXXX0111	(8)															
XXXX1000	(1)															
XXXX1001	(2)															
XXXX1010	(3)															
XXXX1011	(4)															
XXXX1100	(5)															
XXXX1101	(6)															
XXXX1110	(7)															
XXXX1111	(8)															

Note: The CGRAM data allocated to addressees "00" through "08" is the same as the CGRAM data allocated to "00" through "0F".

○ Segment RAM (SGRAM)

The segment RAM (SGRAM) allows the user to display or not display icons and marks through user's programs. Data is read from the SGRAM and segments are displayed by selecting COM_9 in the one-line display mode, and selecting COM_{17} in the two-line display mode. The SGRAM bits that correspond with the display segments are set directly. The display is not shifted and does not depend on the DDRAM and CGRAM set values.

The SGRAM contains 8-bit data. The last 6-bit data controls ON/OFF of each segment and the blink of the 5-bit segments in each address. The first 2 bits are invalid.

Relationship between the SGRAM addresses and display patterns

SGRAM ADDRESS				SEGRAM DATA							
A_3	A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	*	*	B	S_5	S_4	S_3	S_2	S_1
0	0	0	1	*	*	B	S_{10}	S_9	S_8	S_7	S_6
0	0	1	0	*	*	B	S_{15}	S_{14}	S_{13}	S_{12}	S_{11}
0	0	1	1	*	*	B	S_{20}	S_{19}	S_{18}	S_{17}	S_{16}
0	1	0	0	*	*	B	S_{25}	S_{24}	S_{23}	S_{22}	S_{21}
0	1	0	1	*	*	B	S_{30}	S_{29}	S_{28}	S_{27}	S_{26}
0	1	1	0	*	*	B	S_{35}	S_{34}	S_{33}	S_{32}	S_{31}
0	1	1	1	*	*	B	S_{40}	S_{39}	S_{38}	S_{37}	S_{36}
1	0	0	0	*	*	B	S_{45}	S_{44}	S_{43}	S_{42}	S_{41}
1	0	0	1	*	*	B	S_{50}	S_{49}	S_{48}	S_{47}	S_{46}

*: Invalid

Notes:

1.) The data set in SGRAM is output in 1-line display mode when COM_9 is selected and in 2-line display mode when COM_{17} is selected.

2.) S_1 throuth S_{50} correspond to segment output driver pin numbers SEG_1 throuhgh SEG_{50}.

3.) B is segment blink control data, expressed using 8-bit data. When it is "1", the segment display where "1" is written, from among the segment data within that SGRAM address, is printed; "0" turns OFF blink.

○ Timing generation circuit

The timing generation circuit generates timing signals to operate internal circuits such as the DDRAM, CGROM, CGRAM, and SGRAM.

MPU operations do not affect LCD display operations. No adverse effect (such as flickering at positions other than the data input position) occurs when writing data to the DDRAM from the MPU.

○ LCD drive circuit

The LCD drive circuit consists of 17 common drivers and 50 segment drivers.

When the display line mode is selected by a command, effective common drivers output driving waveforms, and the other drivers output nonselective waveforms.

○ Cursor/blink/inversion control circuit

This circuit controls the cursor/blink/inversion display. The position of cursor/blink/inversion corresponds to the DDRAM data address set in the address counter.

The cursor position is given as follows when the address counter is "08H."

N=0 (1-line display)

1	2	3	4	5	6	7	8	9	10	← Display position
00	01	02	03	04	05	06	07	08	09	← DDRAM address

Cursor position

N=1 (2-line display)

1	2	3	4	5	6	7	8	9	10	← Display position
00	01	02	03	04	05	06	07	08	09	← DDRAM address
10	11	12	13	14	15	16	17	18	19	← DDRAM address

Cursor position

Note: The cursor/blink/inversion display is given likewise when the CGRAM or SGRAM address is in the address counter. In this case, the cursor/blink/inversion display is irrelevant to the DDRAM data address.

○ LED control

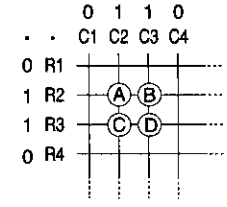
The BU97711 has an NMOS open drain output for 3-bit register control. LED ON/OFF can be controlled by the MPU through the serial interface.

Because 2 bits out of the 3 bits can be allocated for a large current drive, the output is suited for driving equipment backlights.

○ Keypad matrix interface

A 6 × 6 keypad can be configured with single contact key switches. Key data can be directly read from the MPU through the serial interface.

The serial outputs of key data when multiple keys are pressed down at the same time are shown in the figure at right. Pressing Ⓐ and Ⓓ simultaneously results in the same key data as pressing Ⓑ and Ⓒ simultaneously.



○ Reset circuit for start-up

The BU97711 is automatically initialized at start-up by the internal reset circuit, and then set to the standby mode. To operate the BU97711 after turning the power on, the standby mode has to be cleared first (the only executable commands in the standby mode are the standby mode clear command and the LED control command).

The initial state corresponds to the state attained after executing the following instructions :

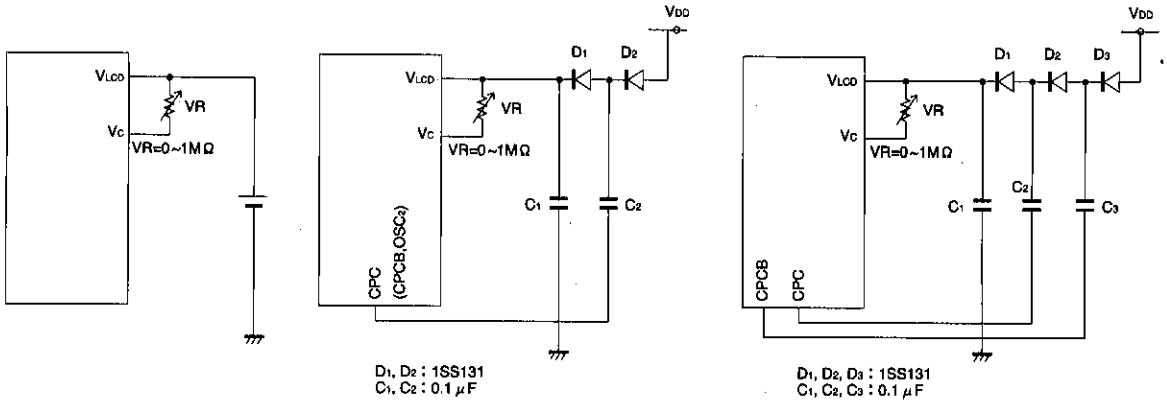
- Display clear : R = 1 (LED is OFF)
- Display mode set : N = 1 (two-line display mode)
- Entry mode set : I/D = 1 (increment mode), S = 0 (shift if OFF)
- Display ON/OFF : D = 0 (display is OFF), C = 0 (cursor is OFF), B = 0 (blink/inversion is OFF)
- Key scan timing set : B1 = 1, B2 = 0, B3 = 0 (ON debounce time is 1500/fosc, OFF debounce time is 2400/fosc)

Note: The reset circuit may not work properly depending on the power supply. If the reset circuit does not work, carry out the initialization by using Instructions.

○ LCD drive power supply

The V_{LCD} voltage is supplied within the range between V_{SS} and 6.0V, regardless of the supply voltage. A contrast adjustment resistor is connected between V_{LCD} and V_C. The power is supplied with a bias of 1/4 by using the internal bleeder resistors between V_C, V_1, V_2, V_3, and V_4.

The BU97711 is receiving output for the booster circuit drive, which can be used to obtain from V_{DD} the V_{LCD} voltage for the LCD drive.



a) V_{LCD}: External supply

D_1, D_2 : 1SS131
C_1, C_2 : 0.1 μF

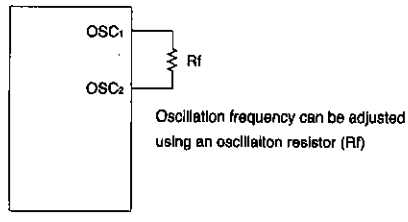
b) V_{LCD}: Using 2x boosted power supply

D_1, D_2, D_3 : 1SS131
C_1, C_2, C_3 : 0.1 μF

c) V_{LCD}: Using 3x boosted power supply

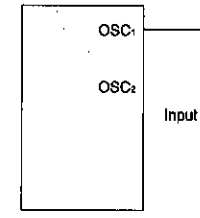
○ Oscillation circuit

The oscillation circuit can be configured with a single external resistor.



Oscillation frequency can be adjusted using an oscillaiton resistor (Rf)

a) Internal oscillation circuit



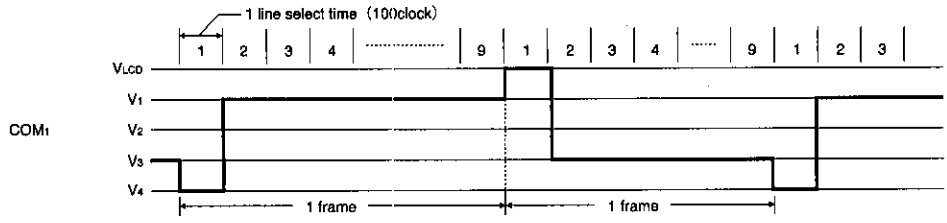
Input from OSC_1 and leave OCS_2 open.

b) Clock external supply

●Relationship between oscillation frequency and frame frequency

All the LCD frame frequencies in the examples below assume an oscillation clock frequency of 80kHz (12.5 μs/CLK).

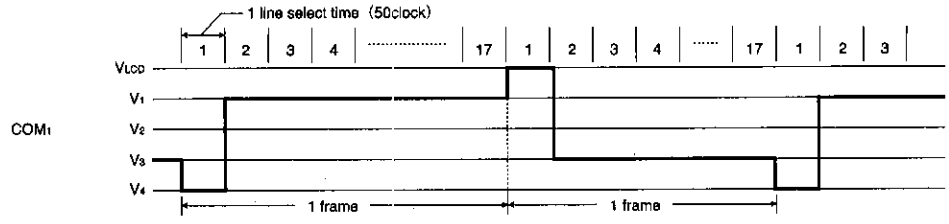
a) 1/9 Duty



1 frame=12.5 (μs) ×100×9=11250 (μs) =11.25 (ms)

$$\text{Frame frequency}=\frac{1}{11.25\ (\text{ms})}=88.89\ (\text{Hz})$$

b) 1/17 Duty

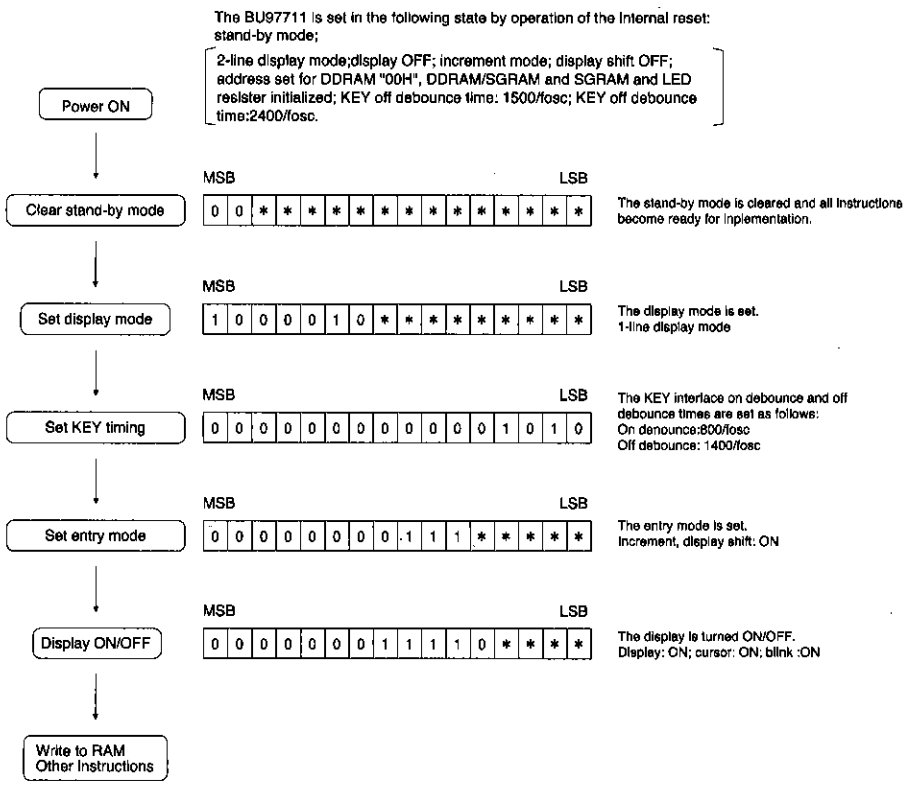


1 frame=12.5 (μs) ×50×17=10625 (μs) =10.625 (ms)

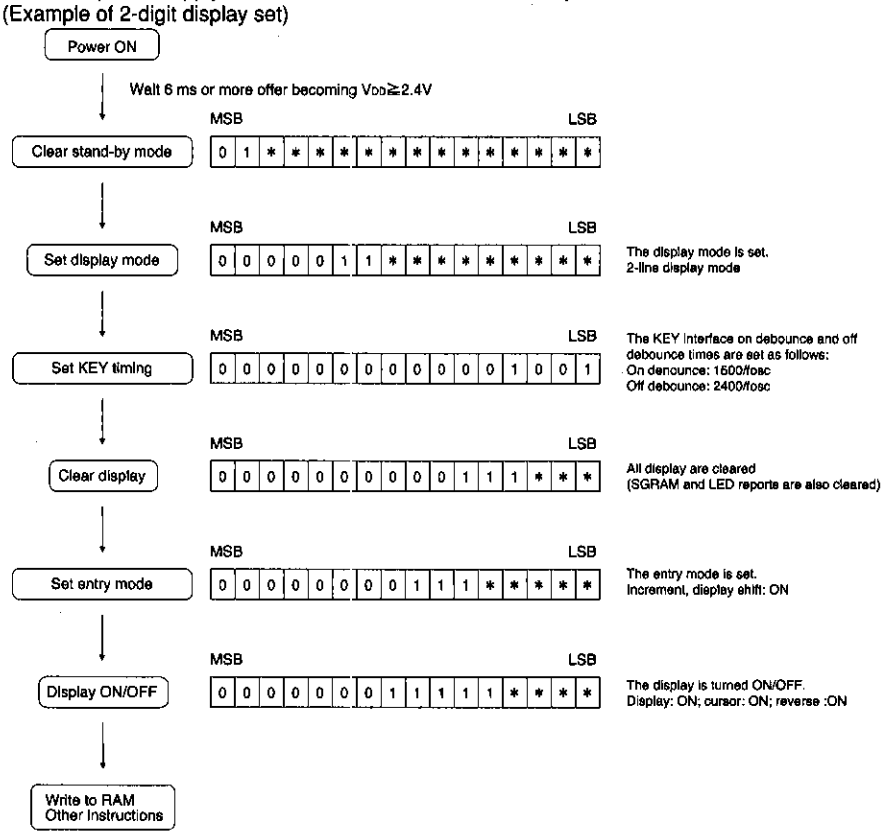
$$\text{Frame frequency}=\frac{1}{10.625\ (\text{ms})}=94.1\ (\text{Hz})$$

●Examples of instruction setting

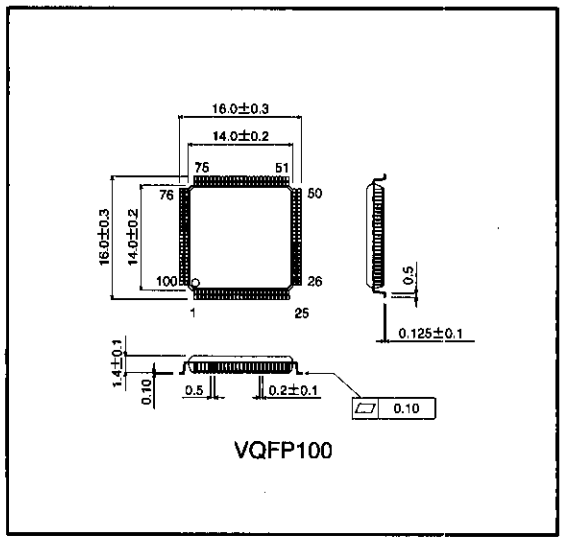
a) When the power supply characteristics of the internal reset are satisfied.



b) When the power supply characteristics of the internal reset operation are not satisfied
(Example of 2-digit display set)



●External dimensions (Units: mm)



VQFP100

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