

# Gray scale processor (64 tones)

## BU2135K

The BU2135K is an LSI designed for use in image scanners and facsimile machines, with a function which takes analog image signals output from an image sensor in an image processing device and converts them to binary format.

This product is equipped with an internal 8-bit A/D converter, image sensor control circuit, and CPU interface, and can be configured easily for data reading. It is compatible with the BU2134AK, making it easy to configure up 64-tone settings.

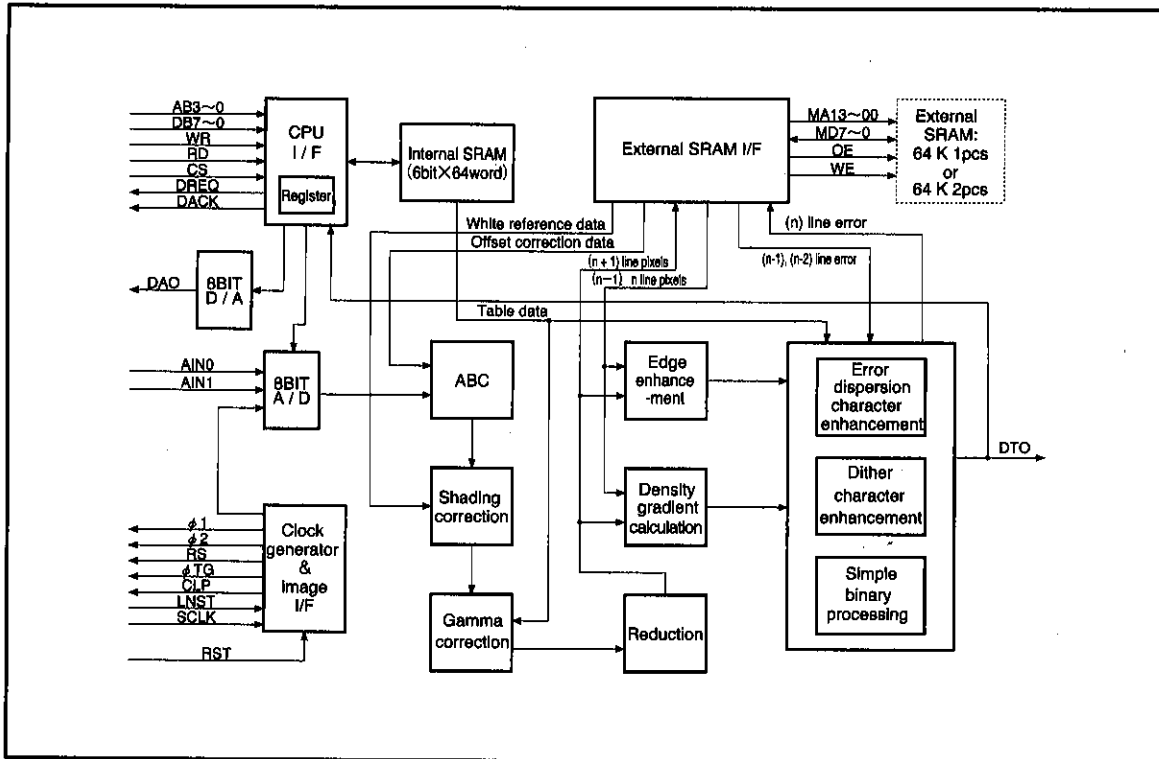
● Applications

Facsimile machines, word processors, and other similar devices

● Features

- 1) Internal 8-bit A/D converter. (internal data width after shading : 6 bits)
- 2) Internal 8-bit D/A converter.
- 3) Isolated point rejection. (when using simple binary processing)
- 4) Applied binary processing.
- 5) Data can be read following shading correction. All other functions of the BU2134AK are included in the BU2135K.

● Block diagram



● Absolute maximum ratings (Unless otherwise noted,  $T_a=25^\circ\text{C}$ ,  $V_{DD}=5\text{V}$ )

Parameter	Symbol	Limits	Unit
Power supply voltage	$V_{DD}$	$-0.3\sim 7.0$	V
Input voltage	$V_{IN}$	$-0.3\sim V_{DD}+0.3$	V
Analog power supply voltage	$AV_{DD}$	$-0.3\sim V_{DD}+0.3$	V
Analog input voltage	$AV_{IN}$	$-0.3\sim AV_{DD}+0.3$	V
Operating temperature	$T_{opr}$	$0\sim 70$	$^\circ\text{C}$
Storage temperature	$T_{stg}$	$-55\sim 150$	$^\circ\text{C}$
Input current	$I_{IN}$	$\pm 20$	mA
Output current	$I_o$	$\pm 20$	mA
Power dissipation	$P_d$	800*	mW

\* Reduced by 8.0mW for each increase in  $T_a$  of  $1^\circ\text{C}$  over  $25^\circ\text{C}$ .

● Recommended operating conditions (Unless otherwise noted,  $T_a=25^\circ\text{C}$ ,  $V_{DD}=5\text{V}$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	$V_{DD}$	4.75	5	5.25	V
Input voltage	$V_{IN}$	0	—	$V_{DD}$	V
Analog power supply voltage	$AV_{DD}$	0	—	$V_{DD}$	V
Analog ground voltage	$A_{GND}$	—	0	—	V
Reference voltage +	$REF+$	3	—	$AV_{DD}$	V
Reference voltage —	$REF-$	0	—	1	V
Analog input voltage	$A_{IN}$	$REF-$	—	$REF+$	V

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## ● Pin descriptions

Parameter	Pin Name	I/O	Function
Video signal output	DTO	Output	Outputs binary video signal as serial data.
Line memory interface	MA13~MA00	Output	Outputs external SRAM address; MA13 is MSB.
	MD7~MD0	Input/Output	Data bus for external SRAM; MD7 is MSB.
	$\overline{OE}$	Output	Output Enable signal for external SRAM (negative logic)
	$\overline{WE}$	Output	Write Enable signal for external SRAM (negative logic)
CPU interface	AB3~AB0	Input	Address input pin; AB4 is MSB.
	DB7~DB0	Input/Output	Data input/output pin; DB7 is MSB.
	$\overline{WR}$	Input	Write input pin for setting internal register (negative logic)
	$\overline{RD}$	Input	Read input pin for reading internal register (negative logic)
	DREQ	Output	Outputs DMA Request signal in parallel mode. Outputs DTO latch clock in serial mode.
	$\overline{DACK}$	Input/Output	Inputs DMA Acknowledge signal in parallel mode (negative logic). Outputs DTO Enable signal in serial mode (negative logic).
	$\overline{CS}$	Input	Chip Select input pin which enables access to internal register (negative logic)
	$\overline{RST}$	Input	System reset input pin (negative logic)
System clock	SCLK	Input	System clock input pin
Line start	LNST	Input	Inputs line start signal
Image sensor interface	$\phi 1$	Output	Output pin 1 for image sensor drive clock
	$\phi 2$	Output	Output pin 2 for image sensor drive clock
	RS	Output	Image sensor reset signal output pin
	$\phi TG$	Output	Image sensor transfer gate pulse output pin
	CLP	Output	Analog ground signal
Analog interface	DAO	Output	Outputs conversion voltage for D/A converter.
	AIN0	Input	Inputs image sensor analog video signals.
	AIN1	Input	Inputs analog signals (such as temperature sensor).
	REF+		Connect this to reference voltage of the A/D converter full-scale point.
	REF-		Connect this to reference voltage of the A/D converter zero point.
Power supply/ground	V <sub>DD</sub>		Connect this to the digital power supply (+5 V) (Pin 3).
	GND		Connect this to the digital ground (Pin 4).
	AV <sub>DD</sub>		Connect this to the analog power supply (Pin 1).
	AGND		Connect this to the analog ground (Pin 1).

● Pin assignments

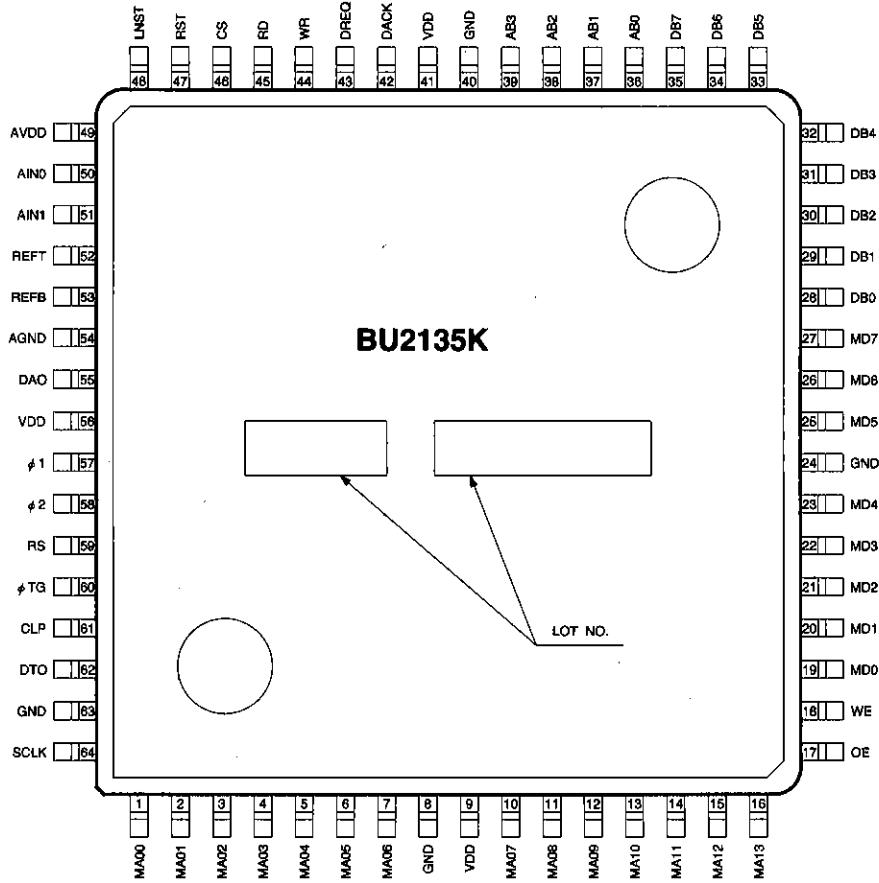


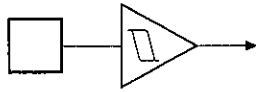
Fig. 1

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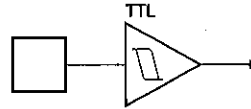
## ● Input/output circuit formats

Pin No.	I/O	Pin Name	I/O Circuit Format	Pin No.	I/O	Pin Name	I/O Circuit Format
1	O	MA00	C	33	I/O	DB5	E
2	O	MA01	C	34	I/O	DB6	E
3	O	MA02	C	35	I/O	DB7	E
4	O	MA03	C	36	I	AB0	B
5	O	MA04	C	37	I	AB1	B
6	O	MA05	C	38	I	AB2	B
7	O	MA06	C	39	I	AB3	B
8	G	GND	—	40	G	GND	—
9	V	V <sub>DD</sub>	—	41	V	V <sub>DD</sub>	—
10	O	MA07	C	42	I/O	DACK	E
11	O	MA08	C	43	O	DREQ	C
12	O	MA09	C	44	I	WR	B
13	O	MA10	C	45	I	RD	B
14	O	MA11	C	46	I	CS	A
15	O	MA12	C	47	I	RST	A
16	O	MA13	C	48	I	LNST	A
17	O	OE	C	49	V	AV <sub>DD</sub>	—
18	O	WE	C	50	I	AIN0	F
19	I/O	MD0	D	51	I	AIN1	F
20	I/O	MD1	D	52	—	REF+	G
21	I/O	MD2	D	53	—	REF-	G
22	I/O	MD3	D	54	G	AGND	—
23	I/O	MD4	D	55	O	DAO	H
24	G	GND	—	56	V	V <sub>DD</sub>	—
25	I/O	MD5	D	57	O	φ1	C
26	I/O	MD6	D	58	O	φ2	C
27	I/O	MD7	D	59	O	RS	C
28	I/O	DB0	E	60	O	φTG	C
29	I/O	DB1	E	61	O	CLP	C
30	I/O	DB2	E	62	O	DTO	C
31	I/O	DB3	E	63	G	GND	—
32	I/O	DB4	E	64	I	SCLK	A

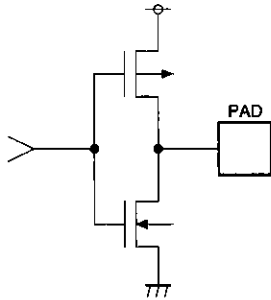
● Input/output circuits



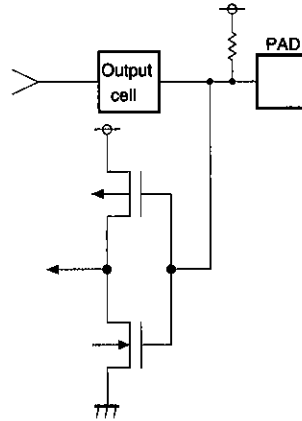
(A) Schmitt input cell



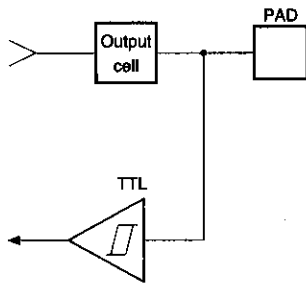
(B) TTL Schmitt input cell



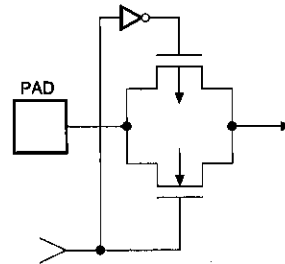
(C) CMOS output cell



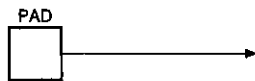
(D) Bi-directional CMOS Input pull-up cell



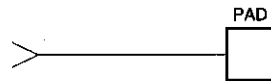
(E) Bi-directional TTL Schmitt input cell



(F) Analog input cell



(G) Reference voltage input cell



(H) Analog output cell

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●DC characteristics (Unless otherwise noted,  $T_a=25^\circ\text{C}$ ,  $V_{DD}=5\text{V}$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input voltage "H"	$V_{IH1}$	3.5	—	$V_{DD}$	V	CMOS level
Input voltage "L"	$V_{IL1}$	0	—	1.5	V	CMOS level
Input voltage "H"	$V_{IH2}$	2.4	—	$V_{DD}$	V	TTL Schmitt
Input voltage "L"	$V_{IL2}$	0	—	0.8	V	TTL Schmitt
Input voltage "H"	$V_{IH3}$	2.7	—	4.0	V	CMOS Schmitt
Input voltage "L"	$V_{IL3}$	1.3	—	2.0	V	CMOS Schmitt
Hysteresis voltage	$V_H$	0.4	—	1.8	V	Schmitt level
Input current "H"	$I_{IH}$	—	—	-10	$\mu\text{A}$	$V_{IH}=V_{DD}$
Input current "L"	$I_{IL}$	—	—	10	$\mu\text{A}$	$V_{IL}=\text{GND}$
Output voltage "H" 1	$V_{OH1}$	4.6	—	—	V	$I_{OH1}=-1.0\text{mA}$
Output voltage "L" 1	$V_{OL1}$	—	—	0.4	V	$I_{OL1}=3.2\text{mA}$
Output voltage "H" 2	$V_{OH2}$	4.6	—	—	V	$I_{OH2}=-2.0\text{mA}$
Output voltage "H" 3	$V_{OH3}$	4.6	—	—	V	$I_{OH3}=-3.5\text{mA}$
Output voltage "L" 3	$V_{OL3}$	—	—	0.4	V	$I_{OL3}=11.2\text{mA}$
Output leakage current	$I_{OZ}$	—	—	$\pm 10$	$\mu\text{A}$	$V_O=V_{DD}$ or GND
Static current consumption	$I_{ST}$	—	—	100	$\mu\text{A}$	$V_i=V_{DD}$ or GND

\* 1  $V_{IH1}$  and  $V_{IL1}$  are applied to Pins MD0 to 7.

\* 2  $V_{IH2}$  and  $V_{IL2}$  are applied to Pins DB0 to 7, AB0 to 3, DACK, WR, and RD.

\* 3  $V_{IH3}$  and  $V_{IL3}$  are applied to Pins CS, RST, LNST, and SCLK.

\* 4  $V_H$  is applied to pins DB0 to 7, AB0 to 3, DACK, WR, RD, CS, RST, LNST, and SCLK.

\* 5  $V_{OH1}$  is applied to the DACK pin.

\* 6  $V_{OL1}$  is applied to Pins MA0 to 13, OE, WE, MD0 to 7, DACK, DREQ,  $\phi 1$ ,  $\phi 2$ , RS,  $\phi$  TG, CLP, and DTO.

\* 7  $V_{OH2}$  is applied to Pins MA0 to 13, OE, WE, MD0 to 7, DREQ,  $\phi 1$ ,  $\phi 2$ , RS,  $\phi$  TG, CLP, and DTO.

\* 8  $V_{OH3}$  and  $V_{OL3}$  are applied to Pins DB0 to 7.

● Switching characteristics (Unless otherwise noted, Ta=25°C, VDD=5V)

	Parameter	Symbol	Min.	Typ.	Max.	Unit
System clock	System clock cycle tcyc	1	60	—	—	ns
	System clock pulse width "H" twh	2	30	—	—	ns
	System clock pulse width "L" twl	3	30	—	—	ns
CPU interface	CS ~ WR, RD setup time	4	0	—	—	ns
	AAB ~ WR, RD setup time	5	20	—	—	ns
	DB ~ WR setup time	6	50	—	—	ns
	WR, RD pulse width	7	100	—	—	ns
	WR, RD ~ CS hold time	8	0	—	—	ns
	WR, RD ~ AB hold time	9	20	—	—	ns
	WR ~ DB hold time	10	20	—	110	ns
	RD ~ DB hold time	10	0	—	—	ns
SRAM interface	Read cycle time	11	—	tcyc	—	ns
	MA, MCS ~ OE setup time	12	—	twh	—	ns
	OE pulse width	13	—	twl	—	ns
	OE ~ MA, MCS hold time	14	0	—	—	ns
	Write cycle time	15	—	tcyc	—	ns
	MA, MCS ~ WE setup time	16	—	twh	—	ns
	MA, MCS ~ WE setup time	17	—	twl	—	ns
	WE pulse width	18	—	twl	—	ns
	WE ~ MA, MCS hold time	19	0	—	—	ns
WE ~ MD hold time	20	0	—	—	ns	

SYSTEM CLOCK

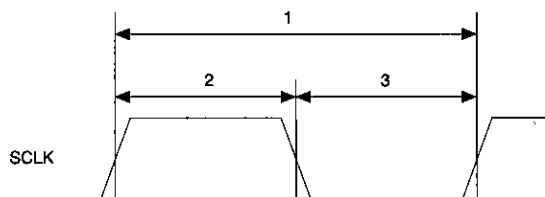


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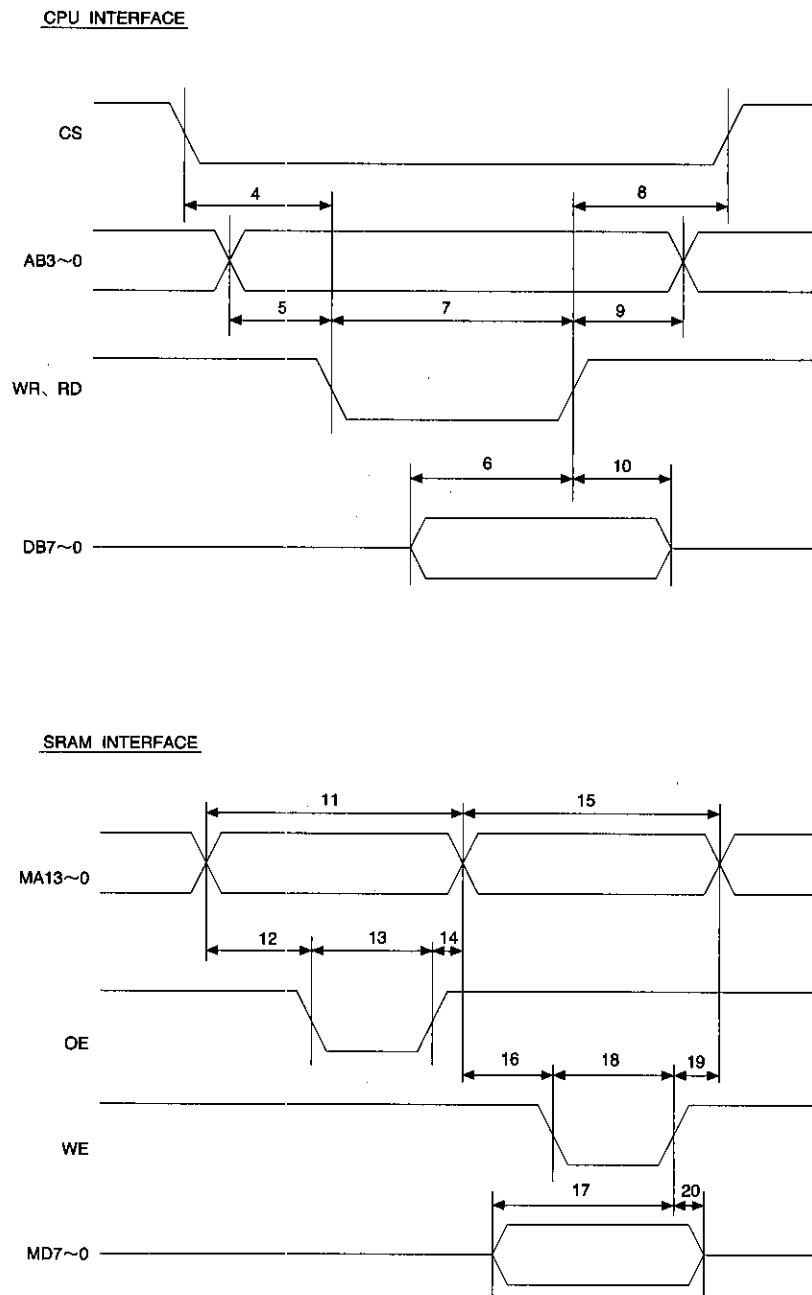


Fig. 2 Data input/output timing

●Description of register functions

Address	DB7	DB6	DB5	D4	DB3	DB2	DB1	DB0	R	W	
0	*8	*7	*6	*5	*4	*3	*2	*1	○	○	
1	*14	*13			*12	*11	*10	*9	×	○	
2	*21	*20	*19		*18	*17	*16	*15	×	○	
3	Line clamp/start position MSB is #				*22				×	○	
4	#	Line clamp/end position							×	○	
5	Distortion correction start position									×	○
6	\$	ABC start position							×	○	
7	ABC end position; MSB is \$									×	○
8	*23									○	○
9	*24									×	○
A	*26				*25				×	○	
B	*28			*27				×	○		
C	*30				*29				×	○	
D	*32			*31				×	○		
E	*35	*34			*33				×	○	
F	D/A converter digital data									×	○
FU	*38	*37	*36	0	0	0	0	0	×	○	

- \*1 White reference screen scan (read enabled)  
 When 0 : Stop  
 When 1 : Start
- \*2 Offset scan (read enabled)  
 When 0 : Stop  
 When 1 : Start
- \*3 Binary processing (read enabled)  
 When 0 : Stop  
 When 1 : Start
- \*4 ABC Enable (read enabled)  
 When 0 : Off  
 When 1 : On
- \*5 ABC initialization  
 When 0 : Off  
 When 1 : On
- \*6 SRAM access select  
 When 0 : Access to external SRAM  
 1) When \*35 is 0 and \*38 is 0 : Read/write white reference data  
 2) When \*35 is 0 and \*38 is 1 : Read/write all addresses  
 3) When \*35 is 1 and \*38 is 0 : Read/write thresholds of applied binary data  
 4) When \*35 is 1 and \*38 is 1 : Use inhibited  
 When 1 : Access to internal SRAM  
 1) When using simple binary processing : 6 bits X 64 words (gamma correction data)  
 2) For dither method : 6 bits X 64 words (slice data)  
 3) For error dispersion method : 6 bits X 64 words (white level)
- \*7 SRAM data/Write Enable  
 When 0 : Writing to SRAM from Address 8 is off  
 When 1 : Writing to SRAM from Address 8 is on
- \*8 SRAM data/Read Enable  
 When 0 : Reading to SRAM from Address 8 is off  
 When 1 : Reading to SRAM from Address 8 is on

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*9 Binary video signal output mode	
When 0 :	Binary video signals are output as serial data.
When 1 :	Binary video signals are output as parallel data.
*10 Parallel mode specification	
When 0 :	First bit of binary video signal is taken as LSB.
When 1 :	First bit of binary video signal is taken as MSB.
*11 Binary video signal selection	
When 0 :	Black = 0, White = 1
When 1 :	Black = 1, White = 0
*12 Offset correction	
When 0 :	Off
When 1 :	On
*13 Internal sample/hold timing	
When 000 :	Sampled at S1 cycle
When 001 :	Sampled at S2 cycle
When 010 :	Sampled at S3 cycle
When 011 :	Sampled at S4 cycle
When 100 :	Sampled at S5 cycle
When 101 :	Sampled at S6 cycle
When 110 :	Sampled at S7 cycle
When 111 :	Sampled at S0 cycle
*14 A/D converter channel switching	
When 0 :	Connected to AIN0
When 1 :	Connected to AIN1
*15 Image sensor	
When 0 :	CCD
When 1 :	CIS
*16 $\phi$ TG output logic	
When 0 :	Positive logic
When 1 :	Negative logic
*17 RS and CLP output logic	
When 0 :	Positive logic
When 1 :	Negative logic
*18 Clamping method	
When 0 :	Bit clamping
When 1 :	Line clamping
*19 $\phi$ 1 clock and RS output specification	
1) $\phi$ 1 clock duty (when using CIS)	
When 00 :	HIGH for S0 to S3 cycles, LOW for S4 to S7 cycles
When 01 :	HIGH for S0 to S3 cycles, LOW for S4 to S7 cycles
When 10 :	HIGH for S0 to S1 cycles, LOW for S2 to S7 cycles
When 11 :	HIGH for S0 to S5 cycles, LOW for S6 to S7 cycles
2) RS output position (when using CCD)	
When 00 :	Output at S5 cycle
When 01 :	Output at S6 cycle
*20 $\phi$ TG pulse width	
1) When using CCD	
When 0 :	Output at S1 to S6 cycles
When 1 :	Output at S0 to S7 cycles
2) When using CIS	
When 0 :	Output at S1 to S0 cycles
When 1 :	Output at S0 to S7 cycles

\*21 Back register enable

When 0 :

Register of Address F is valid.

When 1 :

Register of Address FU is valid.

\*22 Manuscript width specification

DB3	DB2	DB1	DB0	Distortion correction width	Reading width	Reading position
0	0	0	0	1728	1728 (A4, 8 dots/mm or equivalent)	
0	0	0	1	2048	1728 (A4, 8 dots/mm or equivalent)	Center
0	0	1	0	2048	2048 (B4, 8 dots/mm or equivalent)	
0	0	1	1	2432	1728 (A4, 8 dots/mm or equivalent)	Center
0	1	0	0	2432	2048 (B4, 8 dots/mm or equivalent)	Center
0	1	0	1	2432	2432 (A3, 8 dots/mm or equivalent)	
0	1	1	0	2592	2592 (A4, 12 dots/mm or equivalent)	
0	1	1	1	3072	2592 (A4, 12 dots/mm or equivalent)	Center
1	0	0	0	3072	3072 (B4, 12 dots/mm or equivalent)	
1	0	0	1	3648	2592 (A4, 12 dots/mm or equivalent)	Center
1	0	1	0	3648	3072 (B4, 12 dots/mm or equivalent)	Center
1	0	1	1	3648	3648 (A3, 12 dots/mm or equivalent)	
1	1	0	0	3456	3456 (A4, 16 dots/mm or equivalent)	
1	1	0	1	4096	3456 (A4, 16 dots/mm or equivalent)	Center
1	1	1	0	4096	4096 (A4, 16 dots/mm or equivalent)	

\*23 Numerator of reduction ratio in horizontal direction

\*24 Denominator of reduction ratio in horizontal direction

The reduction ratio is set as shown below, using Address 8 (numerator) and Address 9 (denominator).

$$\text{Reduction ratio} = \frac{(\text{value set for reduction ratio numerator}) + 1}{(\text{value set for reduction ratio denominator}) + 1}$$

\*25 Black follow-up speed

When 0 :

ABC circuit not followed on dark background

When 1 to 15 :

The larger the set value, the faster the ABC is followed on a dark background.

\*26 White follow-up speed

When 0 :

ABC circuit not followed on light background

When 1 to 15 :

The larger the set value, the faster the ABC is followed on a light background.

\*27 Binary parameter

1) For simple binary processing :

Set the slice level.

2) For organizational dither processing :

This parameter is invalid.

3) For error dispersion processing :

Set the black level.

\*28 Binary mode

When 00 :

Simple binary processing

When 01 :

Simple binary processing

When 10 :

Pseudo intermediate processing using organizational dither method

When 11 :

Pseudo intermediate processing using error dispersion method

\*29 Degree of edge enhancement in horizontal direction

When 0 :

Edge enhancement off

When 1 to 15 :

The larger the set value, the stronger the enhancement will be.

\*30 Degree of edge enhancement in vertical direction

When 0 :

Edge enhancement off

When 1 to 15 :

The larger the set value, the stronger the enhancement will be.

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- \*31 Edge enhancement correction parameter  
This parameter is used as a threshold to judge whether edge enhancement or smoothing is to be carried out when the amount of density of the pixel edge in question changes.
- \*32 Degree of smoothing  
When 0 : Smoothing function off  
When 1 to 6 : The larger the set value, the greater the degree of smoothing that is carried out.  
When 7 : Use inhibited
- \*33 Character enhancement parameter B  
When pseudo intermediate processing is used, this parameter is used as a threshold to determine whether or not edge enhancement is to be carried out when the amount of density in both the horizontal and vertical directions is changed.
- \*34 Character enhancement parameter A  
1) This parameter defines character enhancement when pseudo intermediate processing is used.  
2) When using the dither method  
When 000 : Character enhancement off  
When 001 to 111 : The larger the set value, the stronger the enhancement will be.  
3) When using the error dispersion method  
When 000 : Character enhancement off  
When 001 to 111 : The larger the set value, the stronger the enhancement will be.
- \*35 Applied binary enable  
When 0 : When using simple binary processing, the slice level is determined by the binary parameter.  
When 1 : When using simple binary processing, the slice level is determined by the average density.
- \*36 Expansion port enable  
When 0 : No expansion ports are used.  
When 1 : Pin 16 (MA13) is used as the expansion port.
- \*37 Expansion port data  
When 0 : The expansion port data is 0.  
When 1 : The expansion port data is 1.
- \*39 Resetting the internal registers of Addresses 0 to 2 and Address FU clears the values to 0.  
The set values for other internal registers do not change when a reset is initiated.
- \*40 Register setting unit  
1) The line clamping start and end positions can be specified in units of 1 pixel.  
2) The distortion correction start position can be specified in units of 1 pixel.  
3) The ABC start and end positions can be specified in units of 16 pixels.
- \*41 In the following cases, Address 8 should be used for reading and writing of data.  
1) Reading digital data after A/D conversion  
2) Reading and writing internal SRAM data  
3) Reading and writing external SRAM data

● Operation timing charts

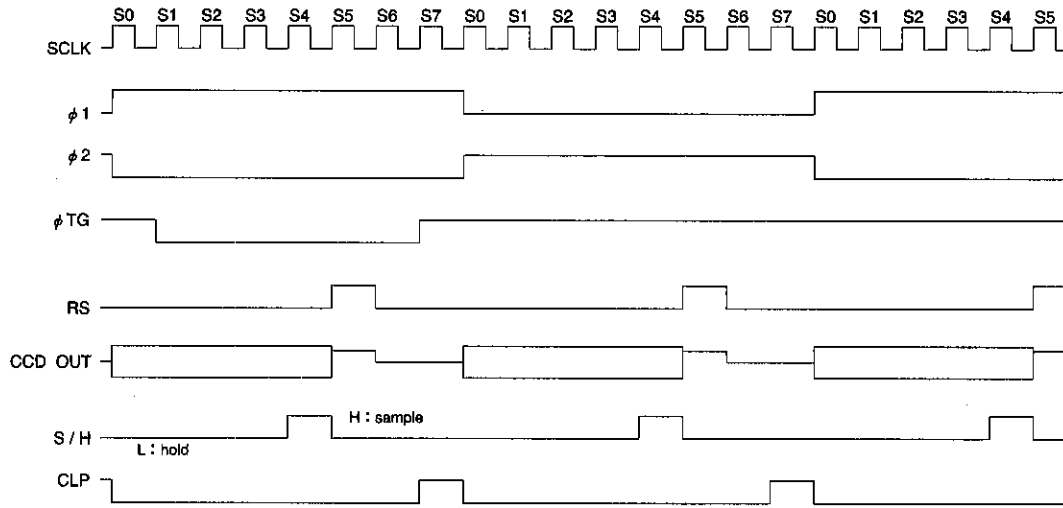


Fig. 3 CCD drive timing diagram -1

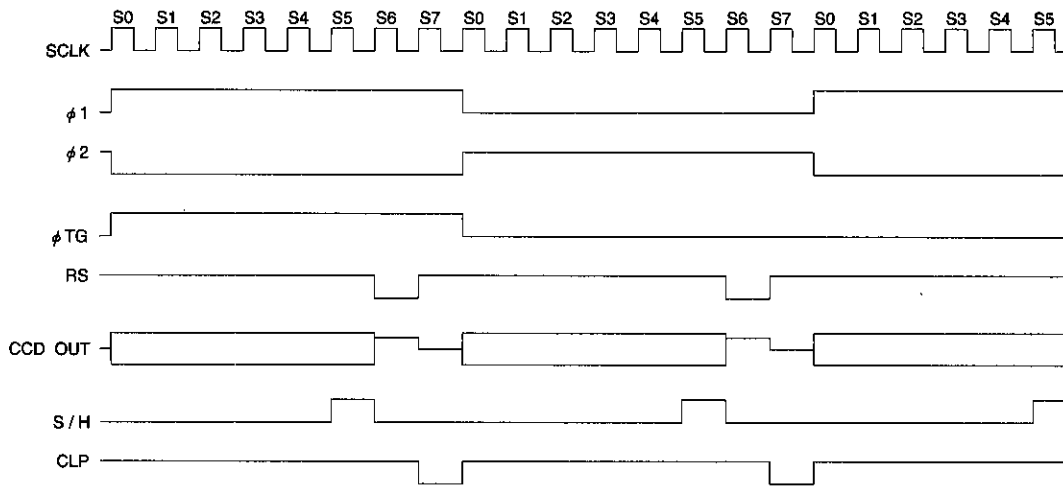


Fig. 4 CCD drive timing diagram -2

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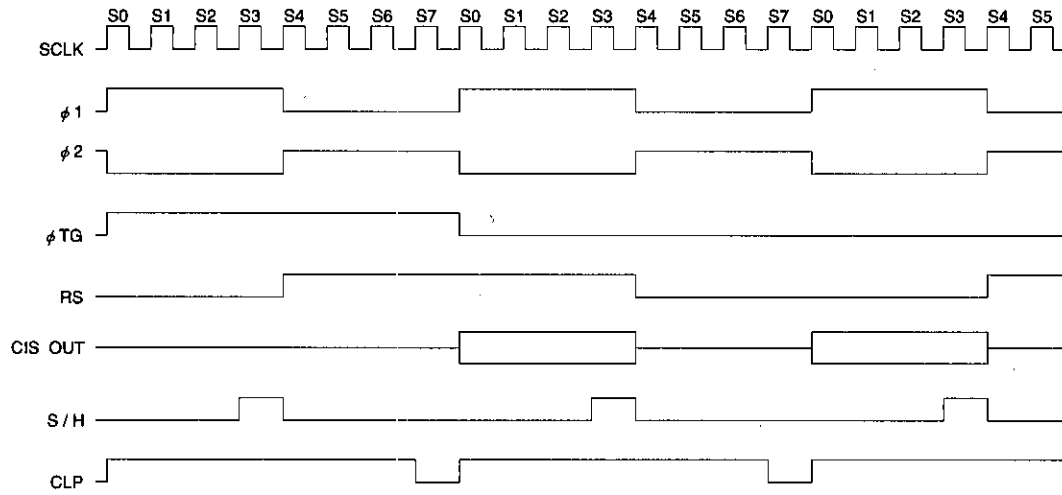


Fig. 5 CIS drive timing diagram -1

● Operation timing charts

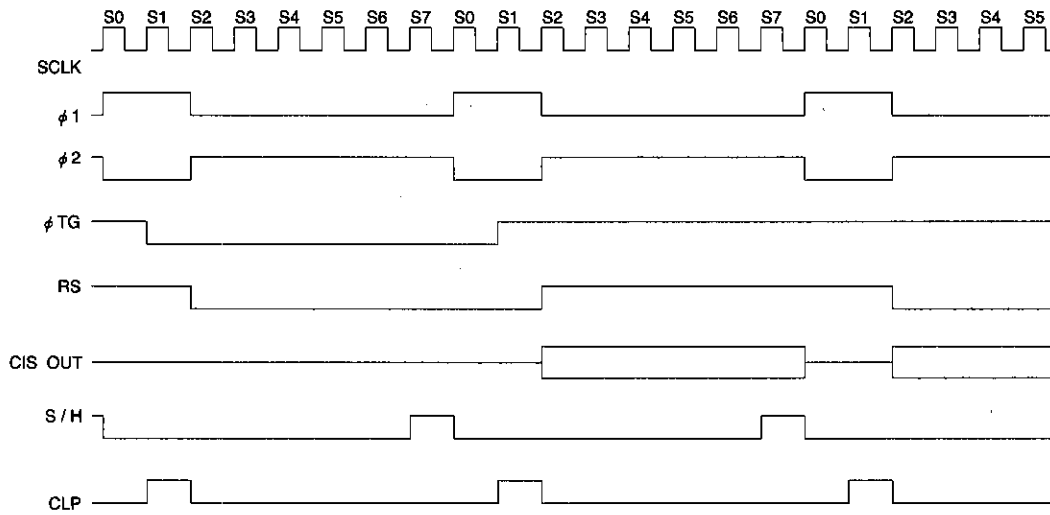


Fig. 6 CIS drive timing diagram -2

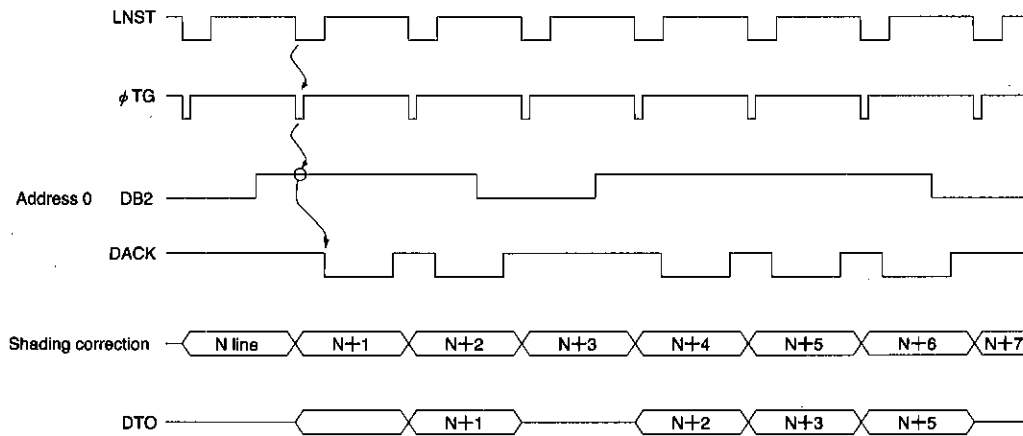


Fig. 7 Line control timing diagram

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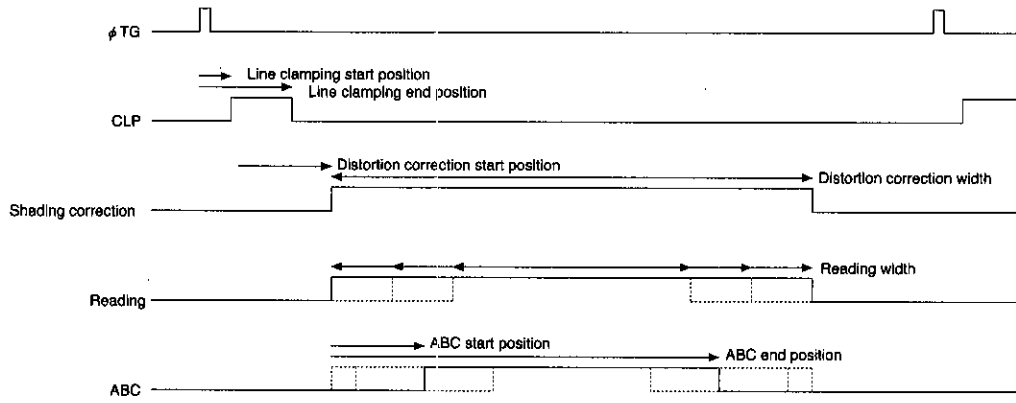


Fig. 8 Scan timing diagram

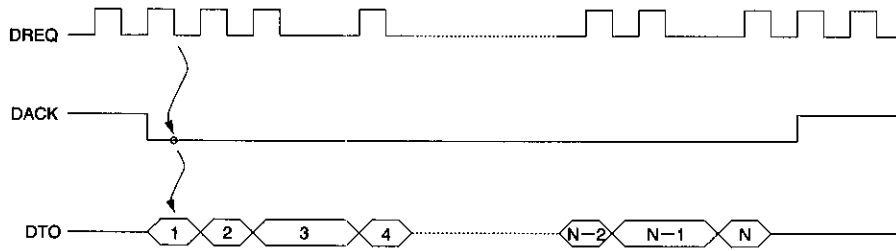


Fig. 9 Output timing diagram (serial mode)

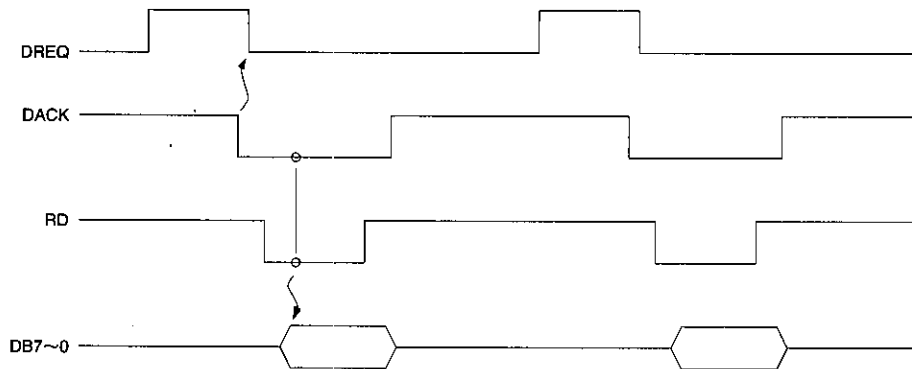


Fig. 10 Output timing diagram (parallel mode)

● Application example

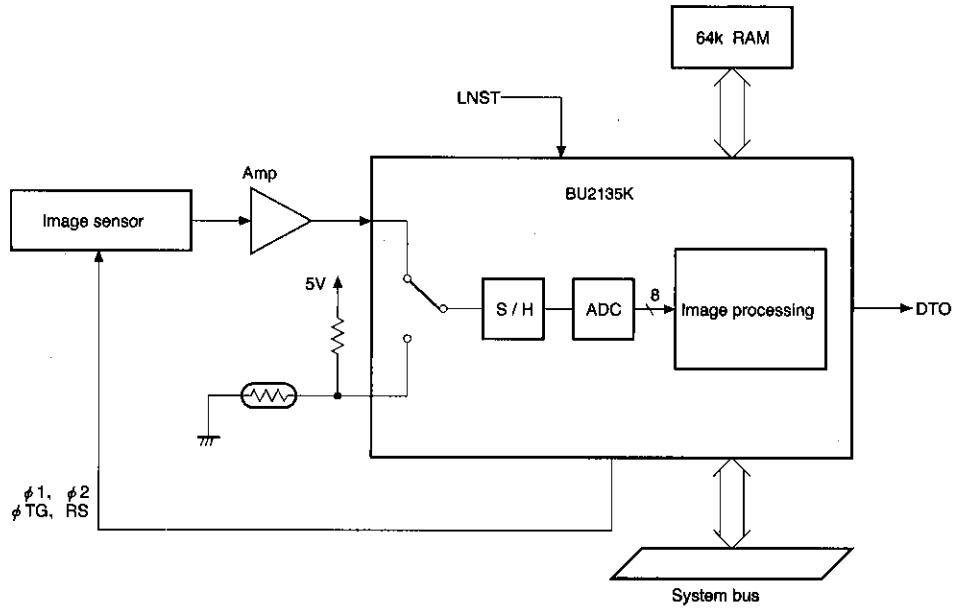


Fig. 11

● External dimensions (Units: mm)

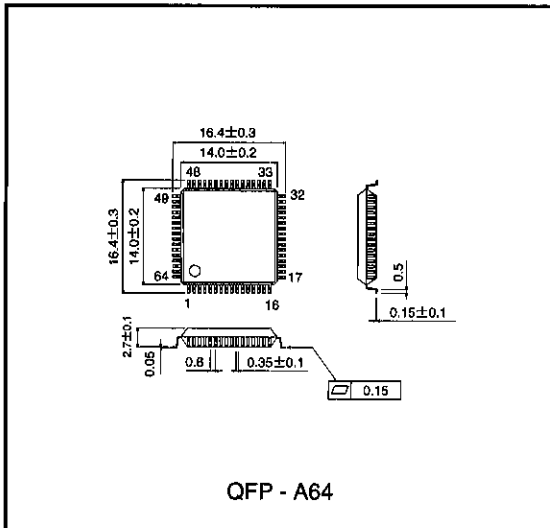


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