Take the Advantage with HDSLink (TSS923/933)

Introduction

A natural way to exchange data between systems is the serial link. Systems become more and more powerful asking a very high speed link. HDSLink provides a simple and low-cost solution to high speed data transmission. This solution is composed of two very efficient point to point communication modules (one transmitter and one receiver) that transfer data over high speed serial link (fiber, twisted-pair, coax) up to 400 Mbits/second. HDSLink uses Radiation Tolerant process for higher performances in very disturbing environment and also two kind of codings. A 8B/10B coding totally Fibre Channel compliant. A 8B/16B coding specially developed to secure communications in very disturbing area allowing data correction.

HDSLink Overview

- Fibre Channel Compliant
- IBM®ESCON™ compliant
- ATM compatible
- 8B/10B coded or 10-bit bypass
- 8B/16B coded or 10-bit bypass
- Data rate
  - 8B/10B : 190 to 400 Mbps
  - 8B/16B : 190 to 400 Mbps
- TTL synchronous I/O
- No external PLL components
- Triple ECL 100K serial outputs
- Dual ECL 100K inputs
- Low power
- Built-In Self-Test
- Single +5V supply
- HOTLINK™ compatible

Functional Description

The TSS923 HDSLink Transmitter and TSS933 HDSLink Receiver transfer data over different kind of media up to 400 Mbps.
Using 8B/10B or 8B/16B coding, height bits of user data are loaded into the transmitter and are encoded. Serial data is shifted out of the three differential PECL (Positive ECL) serial ports at the bit rate (which is in this case ten times the byte rate).
The receiver accepts the serial flow at its differential inputs and using a completely integrated digital phase-locked-loop clock synchronizer recovers the timing information necessary for data extraction. The data flow is de-serialized, decoded and checked. Then the recovered byte is presented in parallel way to the host with the synchronized byte rate clock. The 8B/10B or 8B/16B encoder/decoder can be bypassed in systems that already scramble the transmitted data. For 8B/10B coding, when bypass mode is used, the ten data bit sampled at the inputs are directly serialized and transmitted. For 8B/16B coding, when bypass mode is used, the ten data bit sampled at the inputs are presented to the Hamming encoder then the result is serialized and transmitted. Signals are available to create a seamless interface with both asynchronous or clocked FIFOs. A built-in Self Test pattern generator and checker allows testing functionality of the entire modules.
HDSLink devices are ideal for variety of applications such as interconnecting of workstations, servers, mass storage, and video transmission equipment. They can also be used in very disturbing area (nuclear areas, space) where communications need to be protected against an hostile environment.

HOTLink™ compatibility

HDSLink used in 8B/10B mode is entirely compatible with HOTLink™ except on the following points :

- BIST sequence.
- Test mode programming.

Security criteria of the transmission in 8B/10B mode :

- Five consecutive identical bits are not allowed in the frame.
- no true DC component.

Security criteria of the transmission in 8B/16B mode:

- Correction of one error detected in a word and detection of two errors.
- Three consecutive identical bits are not allowed in the frame.
- no true DC component.

Other specific security advantages of HDSLink :

- Radiation Tolerant (> 30 krad)
- A loss of REFCLK will not effect the receiver if this one is already synchronized on the received serial flow even for low frequency variation of the received flow.

Programming comparison between HOTLink™ and HDSLink

For the Transmitter

MODE	$\overline{BISTEN}$	$\overline{ENAENN}$	CYPRESS **CY7B923** (HOTLink)	TEMIC **TSS923** (HDSLink)
0	0	1	PBIST 8B/10B(1)	Encode 8B/10B
	0	0	LSFR 8B/10B(2)	Encode 8B/10B
	Left Open	1	N.A.(3)	PBIST 8B/16B
	Left Open	0	N.A.	LSFR 8B/16B
	1	X	Encode 8B/10B	Encode 8B/10B
Float	0	1	Clock test and PBIST 8B/10B	Clock Test and Encode 8B/16B
	0	0	Clock Test and LSFR 8B/10B	Clock Test and Encode 8B/16B
	Left Open	1	N.A.	Clock Test and PBIST 8B/10B
	Left Open	0	N.A.	Clock Test and LSFR 8B/10B
	1	X	Clock Test and Encode 8B/10B	Clock Test and Encode 8B/10B
1	0	1	PBIST 8B/10B	Bypass 8B/16B
	0	0	LSFR 8B/10B	Bypass 8B/16B
	Left Open	1	N.A.	PBIST 8B/10B
	Left Open	0	N.A.	LFSR 8B/10B
	1	X	Bypass 8B/10B	Bypass 8B/10B

(1) : "0" and "1" alternated on the line
(2) : Line Feed Back Register which generates a 511-byte pattern including data codes and special characters
(3) : Not Applicable

A pin left open means that no signal is applied on this pin. This pin is then internally tied to Vcc/2.
It is important to notice that HOTLink™ and HDSLink are entirely compatible from state of pin point of view.

It means also that you can directly replace HOTLink™ by HDSLink. But if you want to take advantages of HDSLink, your design has to take into account the tri-state capability of $\overline{\text{BISTEN}}$ pin.

For the receiver

MODE	$\overline{\text{BISTEN}}$	CYPRESS **CY7C933**	TEMIC **TSS933** (HDSLink)
0	0	LSFR 8B/10B (2)	Decode 8B/16B
	Left Open	N.A. (3)	GPA 8B/16B (1)
	1	Decode 8B/10B	Decode 8B/10B
Left Open	0	Clock Test and LSFR 8B/10B	Clock Test and Decode 8B/16B
	Left Open	N.A.	Clock Test and LSFR 8B/10B
	1	Clock Test and Decode 8B/10B	Clock Test and Decode 8B/10B
1	0	LSFR 8B/10B	Bypass 8B/16B
	Left Open	N.A.	LSFR 8B/10B
	1	Bypass 8B/10B	Bypass 8B/10B

(1) : "0" and "1" alternated on the line
(2) : Line Feed Back Register which generates a 511-byte pattern including data codes and special characters
(3) : Not Applicable

A pin left open means that no signal is applied on this pin. This pin is then internally tied to Vcc/2.
It is important to notice that HOTLink™ and HDSLink are entirely compatible from state of pin point of view.

It means also that you can directly replace HOTLink™ by HDSLink. But if you want to take advantage of HDSLink, your design has to take into account the tri-state mode capability of the $\overline{\text{BISTEN}}$ pin.

Coding comparison between HOTLink™ and HDSLink

HOTLink and HDLink are fully Fibre Channel compliant concerning 8B/10B coding. Only HDSLink has capabilities to generate 8B/16B coding. This coding is organized as 8B/10B coding including special characters for control depending level applied on SC/$\overline{\text{D}}$ pin. Whatever the coding chosen mode D0.0 to D31.7 and K28.0 to K30.7 are represented including Idle, R_RDY, EOFxx, C-SOF, P-SOF and Exceptions characters. You will find in Annex 1 the 8B/10B-8B/16B coding tables.

Design and application considerations

Using decoupling capacitor

Faster edges and higher clock rates require a "good" decoupling of power supplies. What used to work for lower systems and slower logic may not work well when the system speed increases. The common practice of using two different values for decoupling can :

- Increase the RFI/EMI problems
- Reduce the reliability of operation
- Reduce the noise tolerance

With high clock rate, all the parasitic inductance of Multi-layer capacitors, the lead inductance or resistance have to be taken into account. Some basic recommendations can improve the resulting design :

- Chose the capacitor based on self-resonnant characteristics to match the clock rate or expected noise frequency of the design
- a minimum of one capacitor per power pin placed as physically close to the power pins of the IC as possible to reduce the parasitic impedances.
- Add as many capacitors needed for your range of frequencies.
- Keep lead lengths on the capacitors below 6mm between the capacitor endcaps and the ground or power pins.

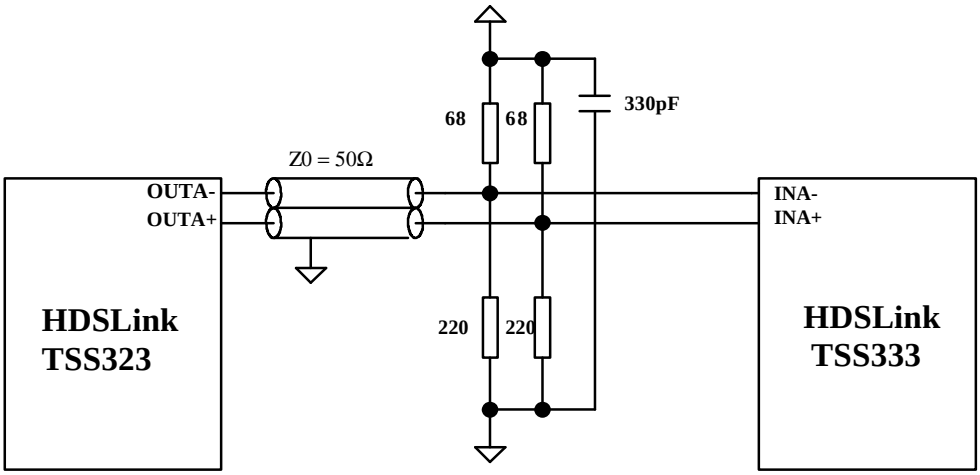
When the clock rate changes over a wide range of frequencies presents the most difficult situation. Generally , most data communications applications use only a single clock rate. When the range of operation of a single part covers a large range of frequencies, placing two capacitors which are within approximately 2:1 of each other in capacitance results in a wider low-impedance area and allows a broadband range of bypass frequencies. Use this multiple decoupling capacitor method only when a wide range of frequencies must be bypassed around a single integrated circuit and adequate range cannot be achieved by a single capacitor.

Driving copper media

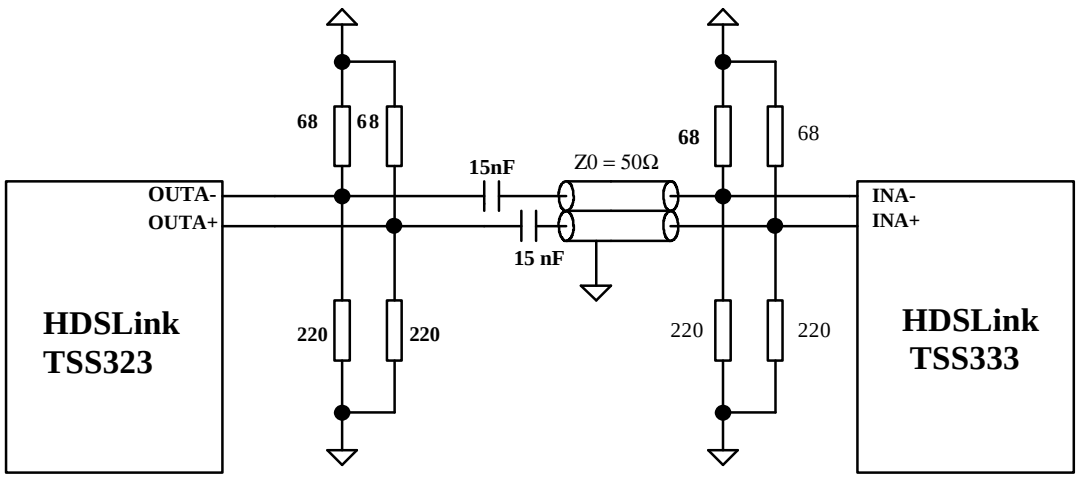
The HDSLink solution is easily capable to interface with both coaxial cable and shielded twisted pair. Coupling to the cable may be done in multiple ways, depending on the media type and distances involved. If the signal never leaves the same board or the same chassis, it is possible to directly couple with the media. The main criteria is there must not have significant Vcc reference between HDSLink Transmitter and Receiver. This maximum difference is around 1V. Under this condition, the Transmitter and Receiver can easily be connected as following figures.

For configuration when it is possible to have significant ground or reference differences an AC coupling solution becomes necessary performed with capacitors. Good low-loss RF grade capacitors should be used . A typical 15nF with high breakdown voltage capacitor would be available with an 1210 surface mount size.
The transformer coupled is similar to capacitor in that it has passband characteristics . Good selection of coupling transformers allows passing of frequencies necessary for HDSLink serial communications.

Direct Coupling



For Capacitor Coupled



HDSLink Oscillator Requirements

The HDSLink modules are designed to operate from a very stable clock source. The current ANSI Fibre Channel standard calls out a frequency accuracy of +/- 100ppm for both source and destination to allow reliable communications. This Fiber Channel requirement is also applicable for 8B/16B mode. To achieve the necessary frequency accuracy and stability it is necessary for the clock source to be based on a quartz crystal or derivated for a very stable clock generator.

Loss of REFCLK

As previously mentioned, the clock sources have to respect Fibre Channel requirements to permit the Receiver synchronization on the received serial data flow. Once this synchronization achieved, HDSLink is capable to continue working properly when a temporary loss of REFCLK occurs and will stay synchronized on the serial data flow even for small and low variation of the reference clock of the transmitter (CKW). REFCLK can be reconnected without disturbing HDSLink if this one respects Fibre Channel requirements. If after synchronization of the Receiver and loss of REFCLK signal, the serial data flow is so disturbed that the receiver loses its synchronization, the CKR signal frequency will drop to low value : around 5.5MHz for 8B/16B mode and 7.5MHz for 8B/10B mode. To restart the synchronization cycle of the Receiver, the REFCLK signal will have to be provided again. This property to be "loss of REFCLK" tolerant is particularly useful when HDSLink is employed into a very disturbing area.

Bypass Capacitors

At the frequencies that HDSLink modules operate, the proper usage of power supply bypassing becomes critical. Strategically sized and placed capacitors are used both to provide AC path between Vcc and ground and to source current when the power supply cannot respond quickly enough due to the parasitic of the power distribution system. The base of any power distributing systems is the circuit board. It is strongly advised to use full power and ground planes , rather than attempting to distribute power and ground on the same layers used for signal distribution. To properly bypass the HDSLink modules, it is necessary to know exactly the role of each power pin.

The Transmitter has three pins assigned to Vcc and two assigned to ground. All three of these Vcc power pins are connected internally and must be connected externally to the same power rail. Pin 4 is named Vccn or Noisy Vcc because it provides power to the ECL output transistors. This pin is usually a noise source loaded in a balanced fashion. If these same outputs are operating single-ended with unbalanced loads, then a varying amount of current will flow though this pin as the outputs switch. To moderate this effect both outputs of the differential driver must have the same load. Pin 9 is called Vccq or Quiet Vcc. This pin provides the power to the CMOS logic core and the TTL compatible input buffers.Pin 22 is also called Vccq or Quiet Vcc. This pin provides power to the analog core (PLL...)
The Receiver has three pins assigned as Vcc and three assigned as ground. Pin 9 is called Vccn or Noisy Vcc. This pin provides power to the TTL-compatible output buffers. Pin 21 is named Vccq or Quiet Vcc. This pin provides power to the CMOS logic core. Pin 24 of the receiver is also called Vccq or Quiet Vcc and provides power to the analog core.

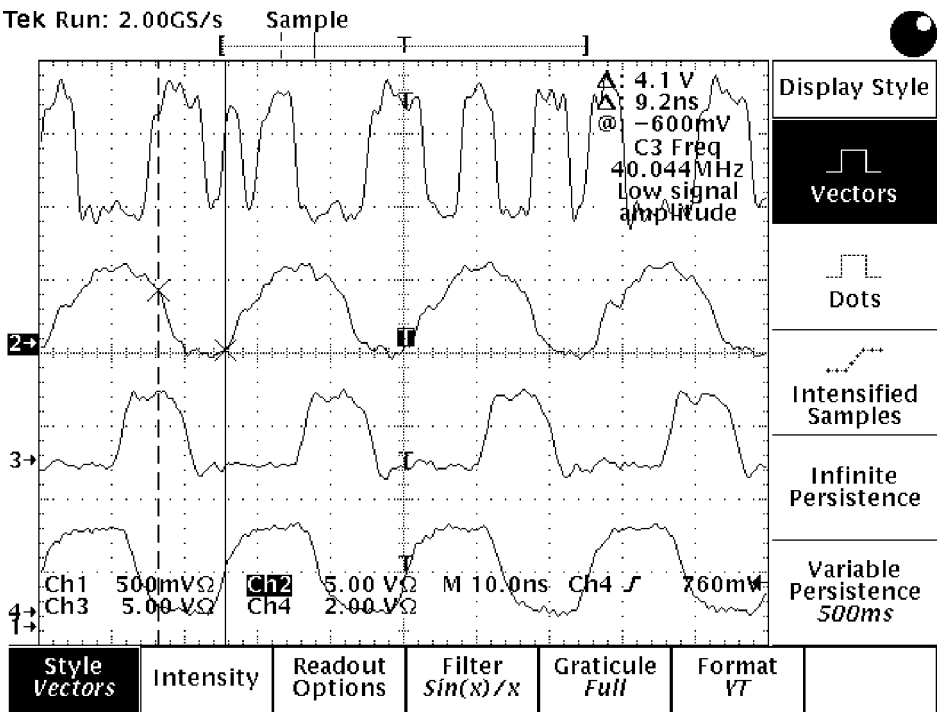
Measurement Precautions

The current ANSI Fibre Channel specifies that the minimum system bandwidth for testing as 1.8 time the baud rate . For testing with HDSLink parts (400Mbaud), this translates to a minimum system bandwidth of 720MHz. This is translated into a viewable rise time using Equation : tr = 0.35/bw. It means the oscilloscope having a 720MHz bandwidth can display signals with rise-time no faster than 500 ps, without having more than 3dB of attenuation. Care should be taken when using probes due to their characteristics. For high-impedance probes, their significant capacitive load affects measurement by slowing down the circuit and degrading the rise-time of the probe. For active high-impedance probes they can non-linear responses to equalize the probe response. It will display more high-frequency components than are actually in the measured signal. Passive low-impedance probes are designed to connect to a 50Ω transmission line system and do not require compensation.
For any measurement a good ground is mandatory. At the frequencies used with HDSLink a long looping ground lead is about as good as no ground. The reflections caused by the scope probe and the ground inductance and the parasitic capacitance limit the probe bandwidth. To correctly observe serial data rate it is usually necessary to use coaxial scop-tip sockets soldered directly to a circuit board.

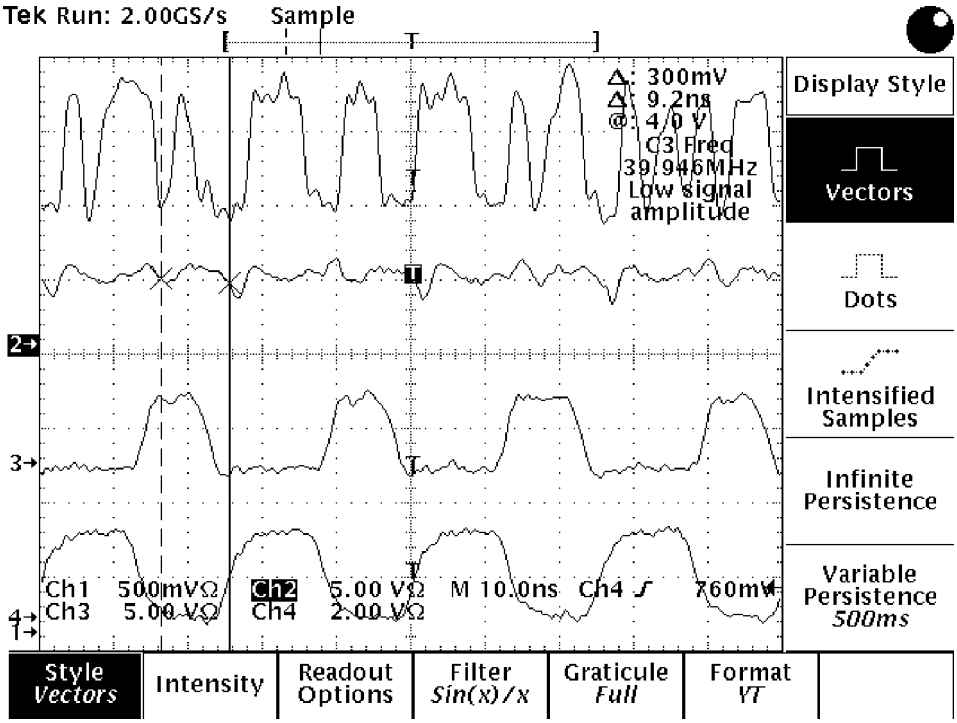
Viewing HDSLink Performances

HDSlink is fully compatible with HOTLink™ and represents the best couple Transmitter/Receiver for high speed link whatever the environment conditions (8B/10B - 8B/16B - Radiations Tolerant). You will find in the following pages some pictures recorded on our evaluation board which show HDSLink performances at ambient temperature. It is clear we have not taken all the precautions described before to record these pictures. The goal was to give an overview of all the HDSLink capabilities.

Picture number 1 : 8B/10B mode at 40MHz with REFCLK with $\overline{ENA}$ = $\overline{ENN}$ = 1 (Sync character transmitted)
From top : OUTA+, REFCLK, CKR, CKW

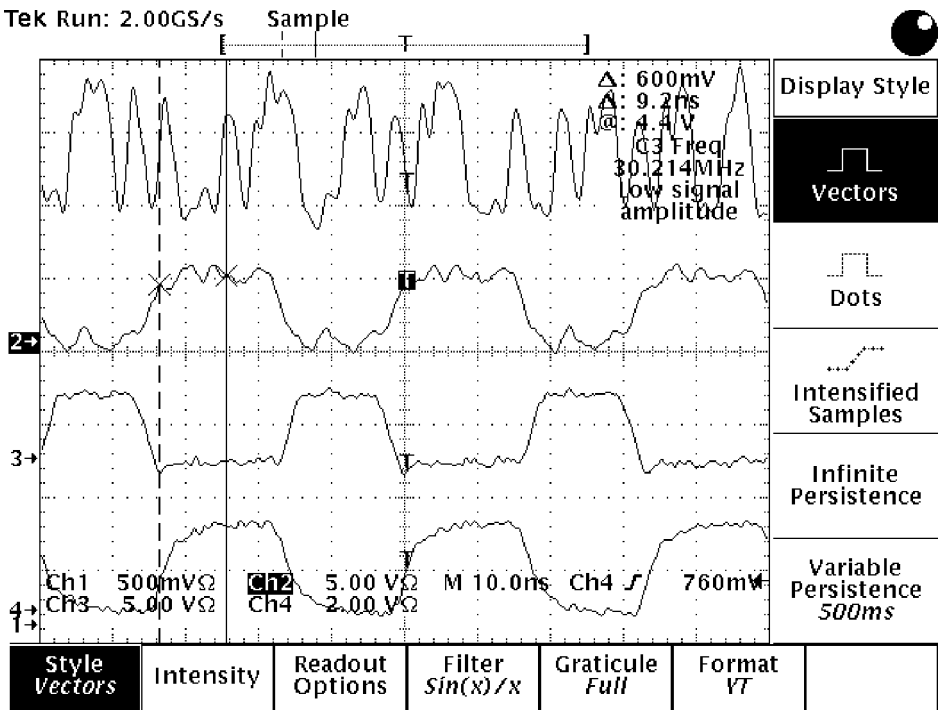


Picture number 2: HDSLink in the same situation than first picture but with REFCLK disconnected
From top : OUTA+, REFCLK, CKR, CKW

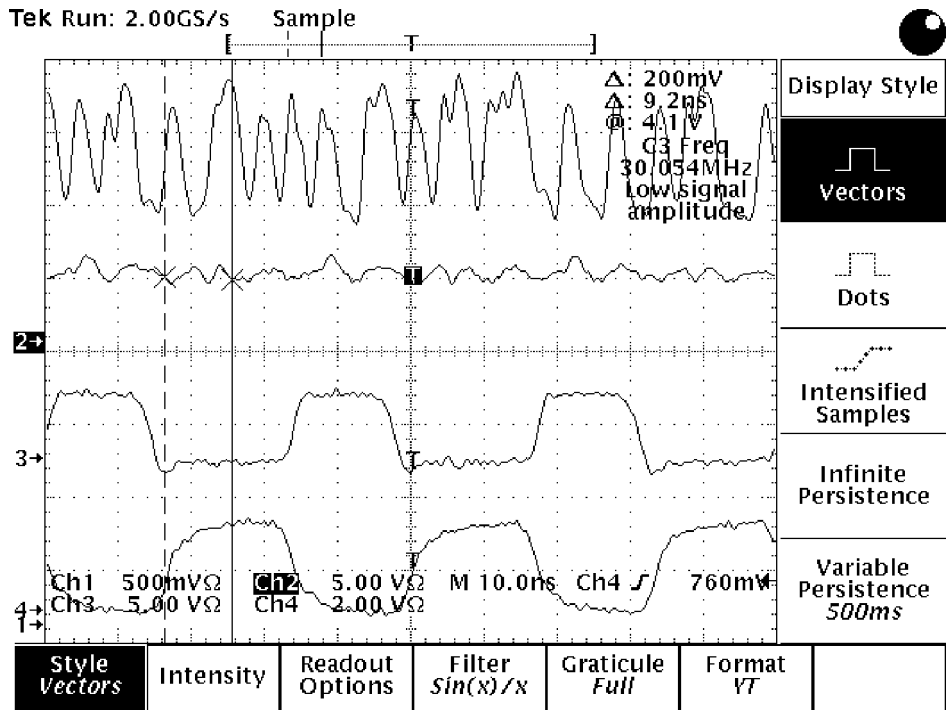


We observe without REFCLK, the synchronization of the receiver is maintained on the serial data flow

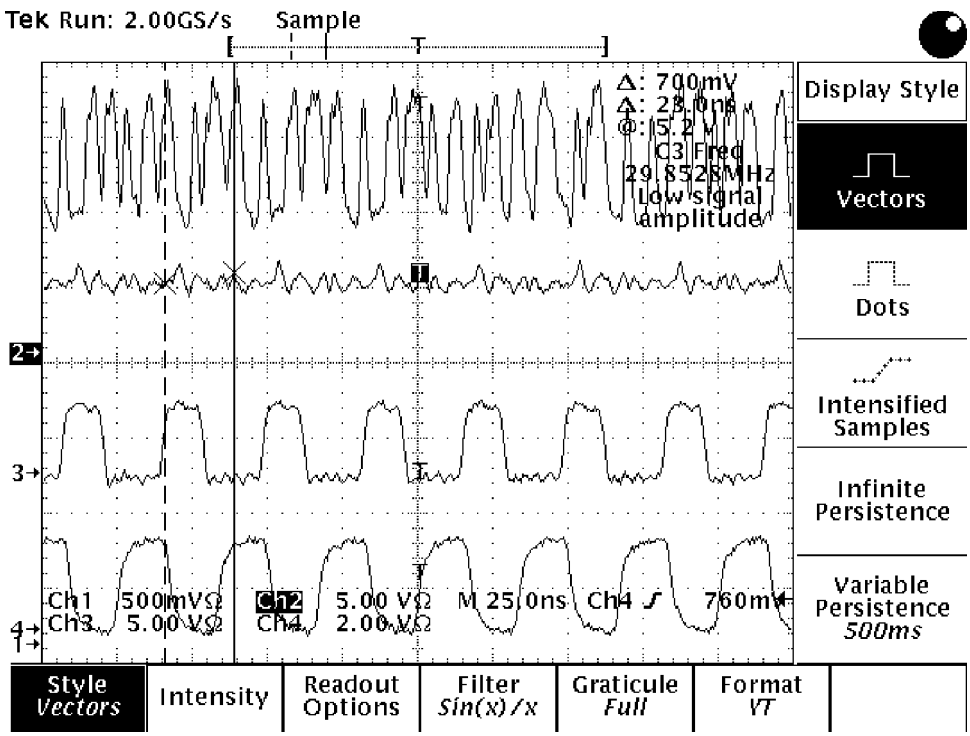
Picture number 3 : 8B/16B BIST mode with REFCLK at 30MHz
From top : OUTA+, REFCLK, CKR, CKW



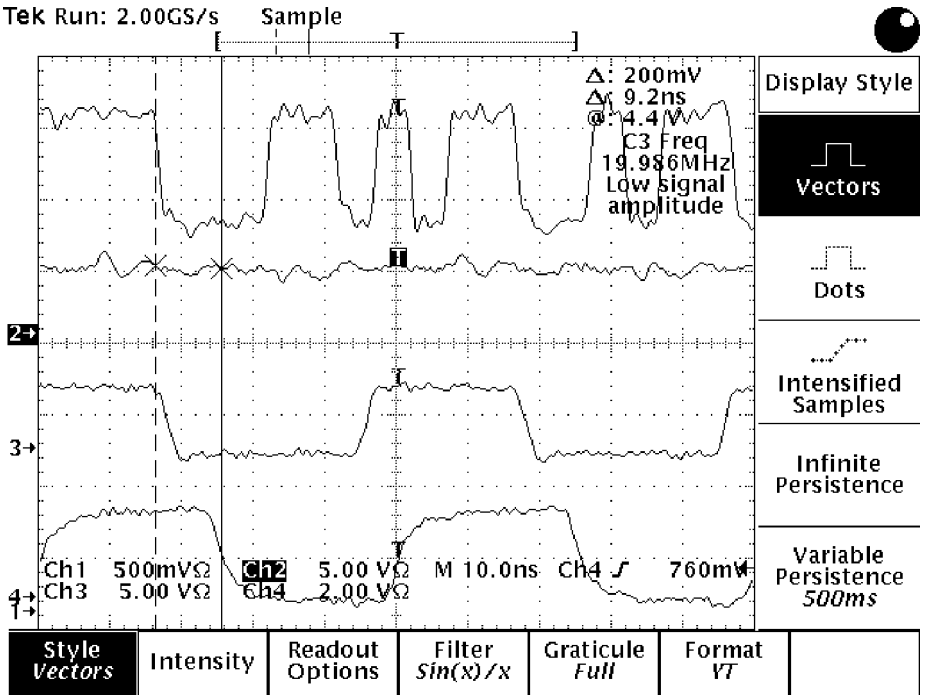
Picture number 4 : 8B/16B BIST mode with REFCLK disconnected at 30MHz
From top : OUTA+, REFCLK, CKR, CKW



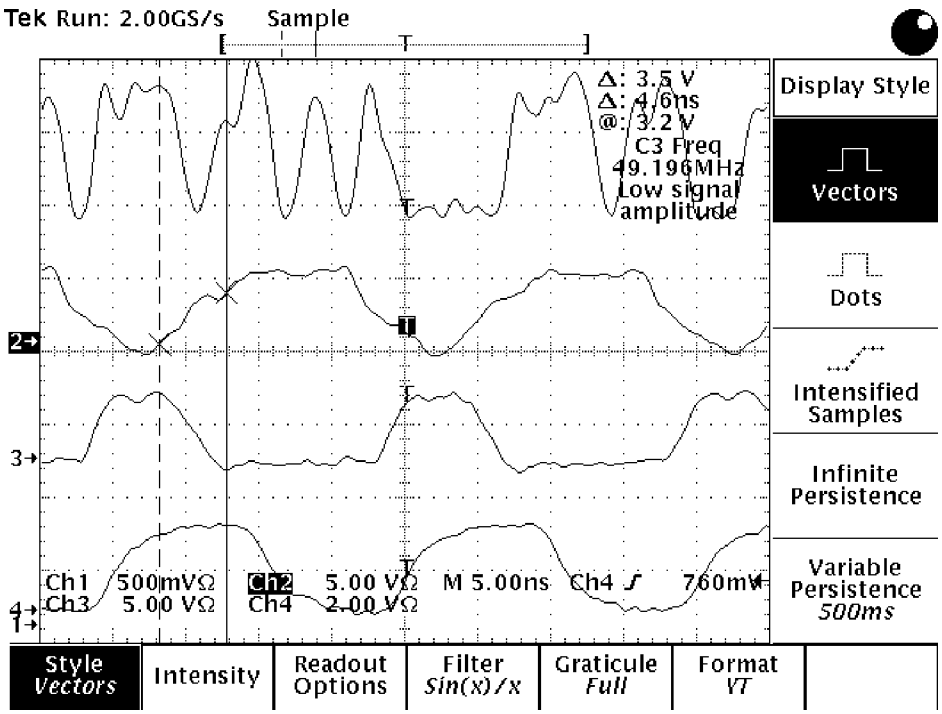
Picture number 5 : 8B/16B BIST mode with REFCLK disconnected (larger scale) at 30MHz
From top : OUTA+, REFCLK, CKR, CKW



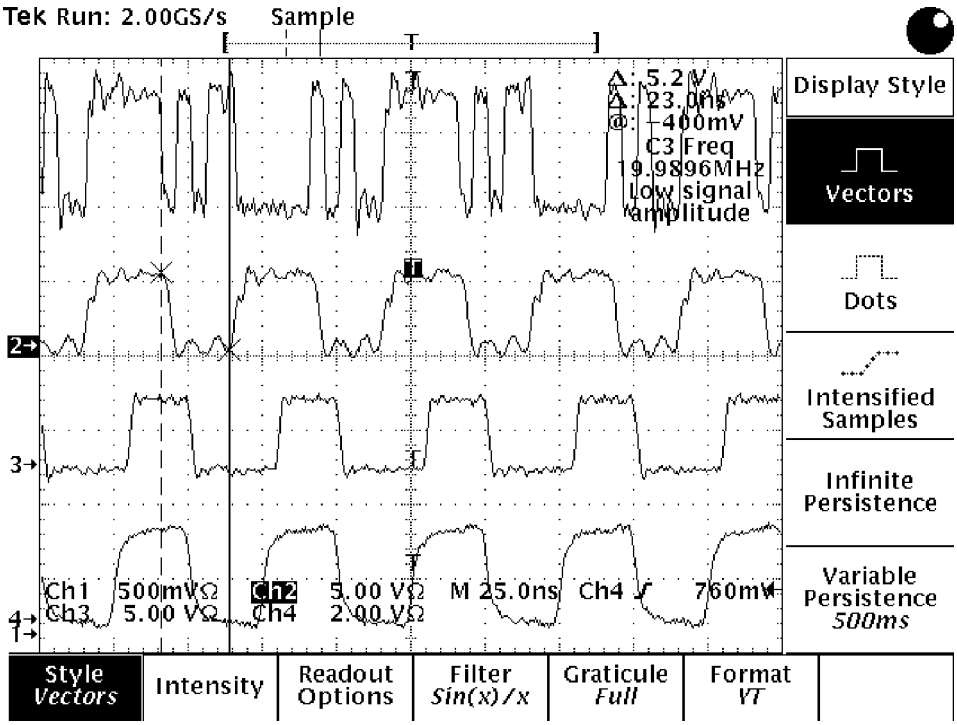
Picture number 6 : 8B/10B mode SYNC characters transmitted with REFCLK disconnected (20MHz)
From top : OUTA+, REFCLK, CKR, CKW



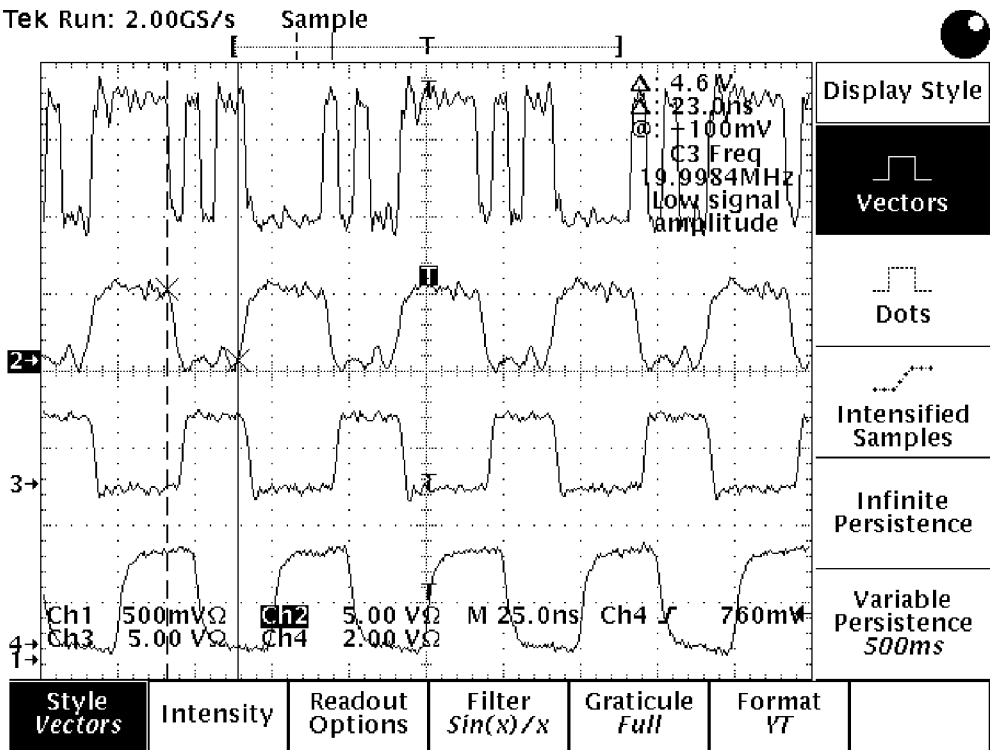
Picture number 7 : 8B/10B BIST mode with REFCLK at 50MHz
From top : OUTA+, REFCLK, CKR, CKW



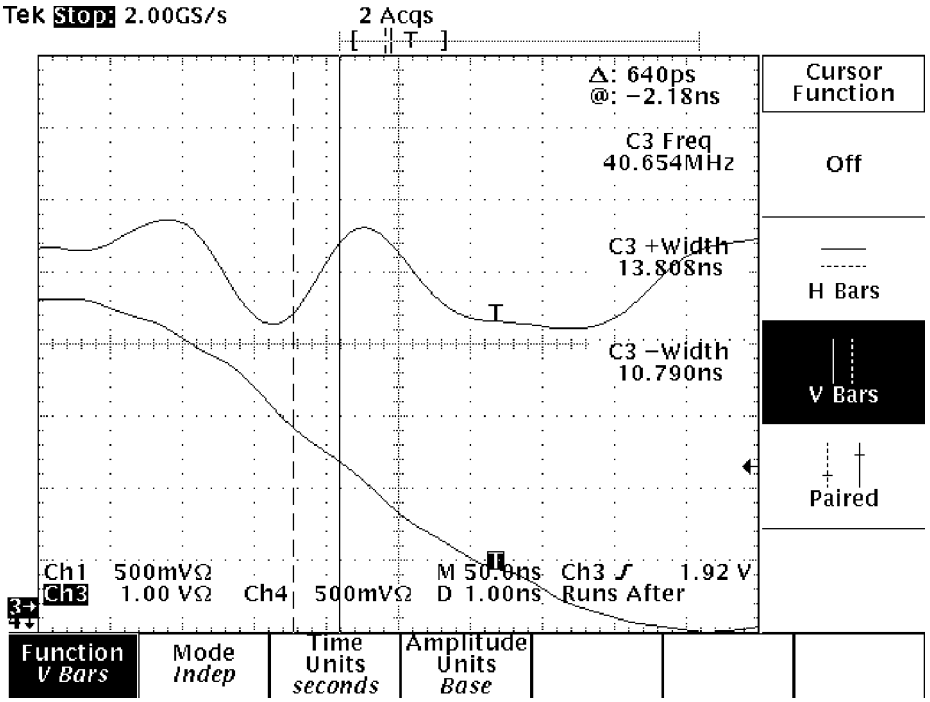
Picture number 8 : 8B/10B mode with receiver synchronized on serial data flow before action on REFrame



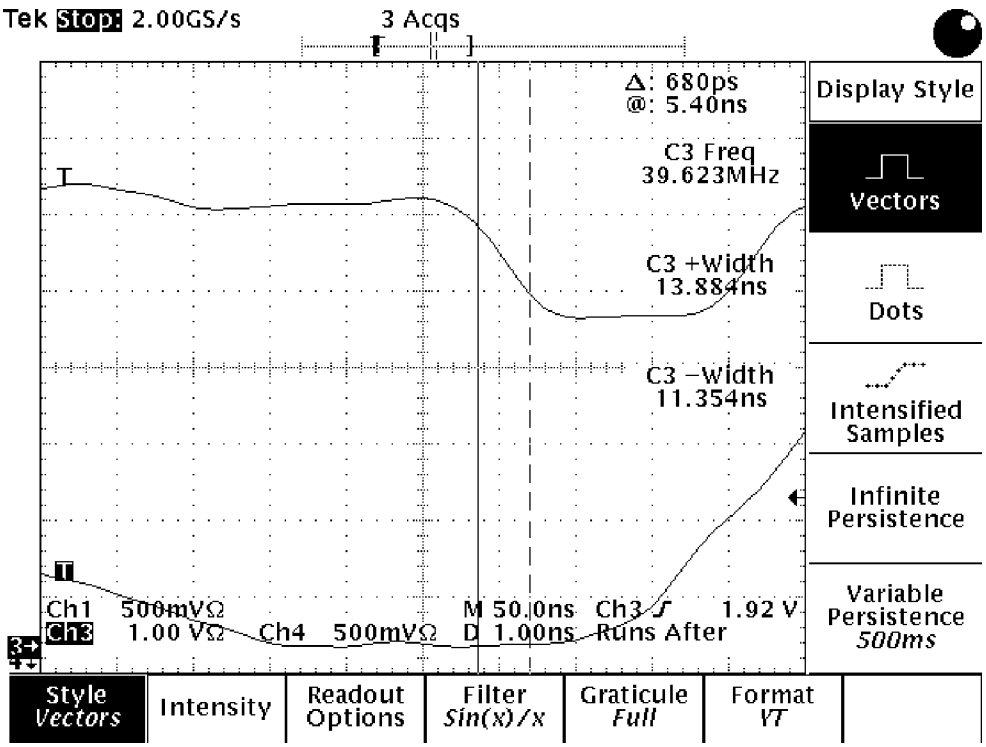
Picture number 9 : After action on REFrame : look at the alignment between CKR and REFCLK



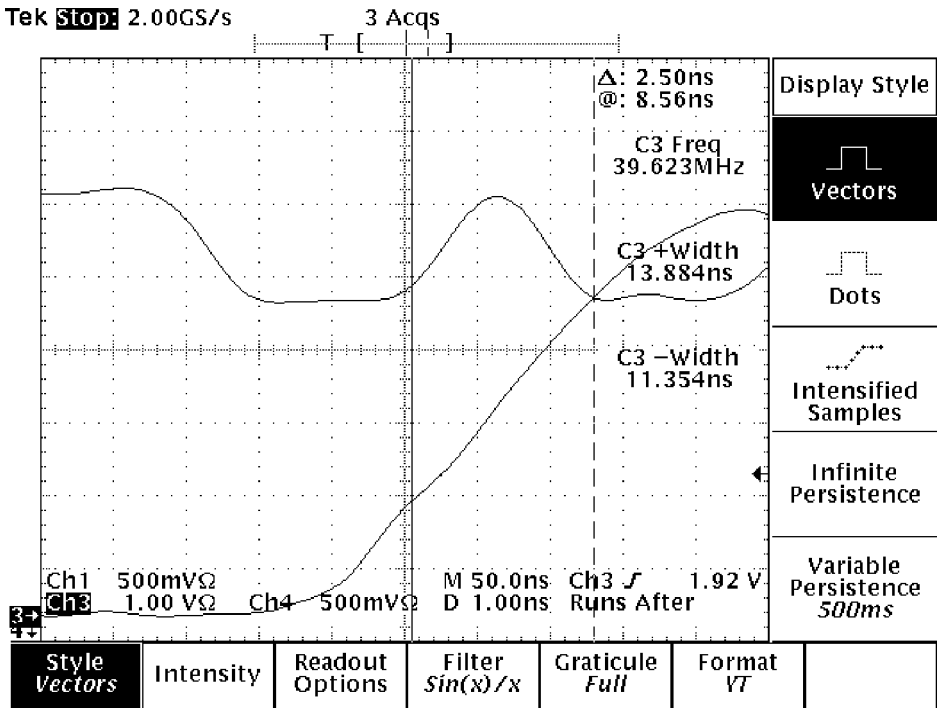
Picture number 10 : rising egde timing with CKW at 40MHz with 50 Ohm load on OUTA+ : 640ps
From top : OUTA+



Picture number 11 : falling edge with CKW at 40MHz with 50 Ohm load on OUTA+: 680ps
From top : OUTA+



Picture number 12 : bit time at 40MHz with 50 Ohm load on OUTA+ : 2.5ns
From top : OUTA+



Annex: a] Transmitted and Received Words on the Line

The first received bit is the MSB bit in the 8B/10B Mode and the LSB bit in the 8B/16B Mode

DATA CHARACTERS (SC/$\overline{D}$ Low)

			8B/10B Encoder/Decoder				8B/16B Encoder/Decoder	
	Bits		Disparity <0		Disparity >0		9B/11B Outputs	Hamming Outputs
Data Byte Name	*765*	*43210*	*abcdei*	*fghj*	*abcdei*	*fghj*	*Information Bits*	*Information and Control bits (p,o,n..c,b,a)*
D0.0	000	00000	100111	0100	011000	1011	00000 110101	1101101100010010
D1.0	000	00001	011101	0100	100010	1011	00000 011011	1001101010100110
D2.0	000	00010	101101	0100	010010	1011	00000 110111	1001001110010110
D3.0	000	00011	110001	1011	110001	0100	00000 011111	1100101000110110
D4.0	000	00100	110101	0100	001010	1011	00000 101101	1101000110110010
D5.0	000	00101	101001	1011	101001	0100	00000 101011	1100100110100110
D6.0	000	00110	011001	1011	011001	0100	00000 101111	1001100100110110
D7.0	000	00111	111000	1011	000111	0100	00000 111011	0101001110100110
D8.0	000	01000	111001	0100	000110	1011	00001 011010	0101101010100101
D9.0	000	01001	100101	1011	100101	0100	00001 001100	1101100010110001
D10.0	000	01010	010101	1011	010101	0100	00001 010110	1001101010010101
D11.0	000	01011	110100	1011	110100	0100	00001 100110	1100100110010101
D12.0	000	01100	001101	1011	001101	0100	00001 111010	1001001110100101
D13.0	000	01101	101100	1011	101100	0100	00001 111100	1000101110110001
D14.0	000	01110	011100	1011	011100	0100	00001 110110	0101001110010101
D15.0	000	01111	010111	0100	101000	1011	00001 101110	0101100100110101
D16.0	000	10000	011011	0100	100100	1011	00010 110101	0101001110011010
D17.0	000	10001	100011	1011	100011	0100	00010 010101	1001101010011010
D18.0	000	10010	010011	1011	010011	0100	00010 110011	0100101110001110
D19.0	000	10011	110010	1011	110010	0100	00010 011001	0101101010101010
D20.0	000	10100	001011	1011	001011	0100	00010 100101	1100100110011010
D21.0	000	10101	101010	1011	101010	0100	00010 101101	0101100100111010
D22.0	000	10110	011010	1011	011010	0100	00010 100011	1101000110001110
D23.0	000	10111	111010	0100	000101	1011	00010 111001	1001001110101010
D24.0	000	11000	110011	0100	001100	1011	00011 101100	1001100100111001
D25.0	000	11001	100110	1011	100110	0100	00011 011100	1100101000111001
D26.0	000	11010	010110	1011	010110	0100	00011 110100	1001001110011001
D27.0	000	11011	110110	0100	001001	1011	00011 010100	0101101010011001
D28.0	000	11100	001110	1011	001110	0100	00011 101000	1100100110101001
D29.0	000	11101	101110	0100	010001	1011	00011 011000	1001101010101001
D30.0	000	11110	011110	0100	100001	1011	00011 110010	1000101110001101
D31.0	000	11111	101011	0100	010100	1011	00011 011010	1101001000101101

			8B/10B Encoder/Decoder				8B/16B Encoder/Decoder	
	Bits		Disparity <0		Disparity >0		9B/11B Outputs	Hamming Outputs
Data Byte Name	*765*	*43210*	*abcdei*	*fghj*	*abcdei*	*fghj*	*Information Bits*	*Information and Control bits (p,o,n..c,b,a)*
D0.1	001	00000	100111	1001	011000	1001	00100 010101	1101001011010010
D1.1	001	00001	011101	1001	100010	1001	00100 010011	1100101011000110
D2.1	001	00010	101101	1001	010010	1001	00100 010111	1001101001010110
D3.1	001	00011	110001	1001	110001	1001	00100 011011	0101101001100110
D4.1	001	00100	110101	1001	001010	1001	00100 100111	1100100101010110
D5.1	001	00101	101001	1001	101001	1001	00100 100011	1001100111000110
D6.1	001	00110	011001	1001	011001	1001	00100 110111	0101001101010110
D7.1	001	00111	111000	1001	000111	1001	00100 111011	1001001101100110
D8.1	001	01000	111001	1001	000110	1001	00101 110110	1001001101010101
D9.1	001	01001	100101	1001	100101	1001	00101 010110	0101101001010101
D10.1	001	01010	010101	1001	010101	1001	00101 100010	0101100111000101
D11.1	001	01011	110100	1001	110100	1001	00101 011010	1001101001100101
D12.1	001	01100	001101	1001	001101	1001	00101 101100	1101000101110001
D13.1	001	01101	101100	1001	101100	1001	00101 111100	0100101101110001
D14.1	001	01110	011100	1001	011100	1001	00101 101010	1100100101100101
D15.1	001	01111	010111	1001	101000	1001	00101 111010	0101001101100101
D16.1	001	10000	011011	1001	100100	1001	00110 101001	1100100101101010
D17.1	001	10001	100011	1001	100011	1001	00110 001011	0100100011101110
D18.1	001	10010	010011	1001	010011	1001	00110 111001	0101001101101010
D19.1	001	10011	110010	1001	110010	1001	00110 011001	1001101001101010
D20.1	001	10100	001011	1001	001011	1001	00110 100001	0101100111001010
D21.1	001	10101	101010	1001	101010	1001	00110 110011	1000101101001110
D22.1	001	10110	011010	1001	011010	1001	00110 110101	1001001101011010
D23.1	001	10111	111010	1001	000101	1001	00110 010101	0101101001011010
D24.1	001	11000	110011	1001	001100	1001	00111 000110	0100100011011101
D25.1	001	11001	100110	1001	100110	1001	00111 001010	1000100011101101
D26.1	001	11010	010110	1001	010110	1001	00111 010100	1001101001011001
D27.1	001	11011	110110	1001	001001	1001	00111 011000	0101101001101001
D28.1	001	11100	001110	1001	001110	1001	00111 100100	1100100101011001
D29.1	001	11101	101110	1001	010001	1001	00111 100010	1101000101001101
D30.1	001	11110	011110	1001	100001	1001	00111 110100	0101001101011001
D31.1	001	11111	101011	1001	010100	1001	00111 110010	0100101101001101

			8B/10B Encoder/Decoder				8B/16B Encoder/Decoder	
	Bits		Disparity <0		Disparity >0		9B/11B Outputs	Hamming Outputs
Data Byte Name	*765*	*43210*	*abcdei*	*fghj*	*abcdei*	*fghj*	*Information Bits*	*Information and Control bits (p,o,n..c,b,a)*
D0.2	010	00000	100111	0101	011000	0101	01000 100111	0101010110010110
D1.2	010	00001	011101	0101	100010	0101	01000 000111	1001110010010110
D2.2	010	00010	101101	0101	010010	0101	01000 101011	1001010110100110
D3.2	010	00011	110001	0101	110001	0101	01000 001011	0101110010100110
D4.2	010	00100	110101	0101	001010	0101	01000 101101	1000110110110010
D5.2	010	00101	101001	0101	101001	0101	01000 011111	1001011000110110
D6.2	010	00110	011001	0101	011001	0101	01000 101001	1101110100100010
D7.2	010	00111	111000	0101	000111	0101	01000 011011	1100011010100110
D8.2	010	01000	111001	0101	000110	0101	01001 100110	1001010110010101
D9.2	010	01001	100101	0101	100101	0101	01001 000110	0101110010010101
D10.2	010	01010	010101	0101	010101	0101	01001 101010	0101010110100101
D11.2	010	01011	110100	0101	110100	0101	01001 001010	1001110010100101
D12.2	010	01100	001101	0101	001101	0101	01001 100100	1101110100010001
D13.2	010	01101	101100	0101	101100	0101	01001 010110	1100011010010101
D14.2	010	01110	011100	0101	011100	0101	01001 101100	0100110110110001
D15.2	010	01111	010111	0101	101000	0101	01001 011110	0101011000110101
D16.2	010	10000	011011	0101	100100	0101	01010 000101	0101110010011010
D17.2	010	10001	100011	0101	100011	0101	01010 010101	1100011010011010
D18.2	010	10010	010011	0101	010011	0101	01010 101001	0101010110101010
D19.2	010	10011	110010	0101	110010	0101	01010 001001	1001110010101010
D20.2	010	10100	001011	0101	001011	0101	01010 100101	1001010110011010
D21.2	010	10101	101010	0101	101010	0101	01010 011101	0101011000111010
D22.2	010	10110	011010	0101	011010	0101	01010 100011	1000110110001110
D23.2	010	10111	111010	0101	000101	0101	01010 011011	0100111000101110
D24.2	010	11000	110011	0101	001100	0101	01011 000100	1001110010011001
D25.2	010	11001	100110	0101	100110	0101	01011 011010	1000111000101101
D26.2	010	11010	010110	0101	010110	0101	01011 100100	0101010110011001
D27.2	010	11011	110110	0101	001001	0101	01011 111010	0100011100101101
D28.2	010	11100	001110	0101	001110	0101	01011 011100	1001011000111001
D29.2	010	11101	101110	0101	010001	0101	01011 011000	1100011010101001
D30.2	010	11110	011110	0101	100001	0101	01011 101100	1100010100111001
D31.2	010	11111	101011	0101	010100	0101	01011 101000	1001010110101001

			8B/10B Encoder/Decoder				8B/16B Encoder/Decoder	
	Bits		Disparity <0		Disparity >0		9B/11B Outputs	Hamming Outputs
Data Byte Name	*765*	*43210*	*abcdei*	*fghj*	*abcdei*	*fghj*	*Information Bits*	*Information and Control bits (p,o,n..c,b,a)*
D0.3	011	00000	100111	0011	011000	1100	01100 010111	1100011001010110
D1.3	011	00001	011101	0011	100010	1100	01100 010011	1001011011000110
D2.3	011	00010	101101	0011	010010	1100	01100 010101	1000111011010010
D3.3	011	00011	110001	1100	110001	0011	01100 011001	0100111011100010
D4.3	011	00100	110101	0011	001010	1100	01100 100111	1001010101010110
D5.3	011	00101	101001	1100	101001	0011	01100 100011	1100010111000110
D6.3	011	00110	011001	1100	011001	0011	01100 101101	0100110101110010
D7.3	011	00111	111000	1100	000111	0011	01100 101011	0101010101100110
D8.3	011	01000	111001	0011	000110	1100	01101 000100	1101010011010001
D9.3	011	01001	100101	1100	100101	0011	01101 000010	1100110011000101
D10.3	011	01010	010101	1100	010101	0011	01101 000110	1001110001010101
D11.3	011	01011	110100	1100	110100	0011	01101 001010	0101110001100101
D12.3	011	01100	001101	1100	001101	0011	01101 010100	0100111011010001
D13.3	011	01101	101100	1100	101100	0011	01101 010010	0101011011000101
D14.3	011	01110	011100	1100	011100	0011	01101 100110	0101010101010101
D15.3	011	01111	010111	0011	101000	1100	01101 011010	1100011001100101
D16.3	011	10000	011011	0011	100100	1100	01110 000001	1100110011001010
D17.3	011	10001	100011	1100	100011	0011	01110 000101	1001110001011010
D18.3	011	10010	010011	1100	010011	0011	01110 001001	0101110001101010
D19.3	011	10011	110010	1100	110010	0011	01110 100011	0100110101001110
D20.3	011	10100	001011	1100	001011	0011	01110 010001	0101011011001010
D21.3	011	10101	101010	1100	101010	0011	01110 100101	0101010101011010
D22.3	011	10110	011010	1100	011010	0011	01110 011001	1100011001101010
D23.3	011	10111	111010	0011	000101	1100	01110 101001	1001010101101010
D24.3	011	11000	110011	0011	001100	1100	01111 000100	0101110001011001
D25.3	011	11001	100110	1100	100110	0011	01111 001000	1001110001101001
D26.3	011	11010	010110	1100	010110	0011	01111 010100	1100011001011001
D27.3	011	11011	110110	0011	001001	1100	01111 010000	1001011011001001
D28.3	011	11100	001110	1100	001110	0011	01111 100000	1100010111001001
D29.3	011	11101	101110	0011	010001	1100	01111 101000	0101010101101001
D30.3	011	11110	011110	0011	100001	1100	01111 100100	1001010101011001
D31.3	011	11111	101011	0011	010100	1100	01111 100010	1000110101001101

			8B/10B Encoder/Decoder				8B/16B Encoder/Decoder	
	Bits		Disparity <0		Disparity >0		9B/11B Outputs	Hamming Outputs
Data Byte Name	*765*	*43210*	*abcdei*	*fghj*	*abcdei*	*fghj*	*Information Bits*	*Information and Control bits (p,o,n..c,b,a)*
D0.4	100	00000	100111	0010	011000	1101	10000 111011	1010001110100110
D1.4	100	00001	011101	0010	100010	1101	10000 110111	0110001110010110
D2.4	100	00010	101101	0010	010010	1101	10000 101011	0011100110100110
D3.4	100	00011	110001	1101	110001	0010	10000 101111	0110100100110110
D4.4	100	00100	110101	0010	001010	1101	10000 011111	0011101000110110
D5.4	100	00101	101001	1101	101001	0010	10000 010111	1010101010010110
D6.4	100	00110	011001	1101	011001	0010	10000 011011	0110101010100110
D7.4	100	00111	111000	1101	000111	0010	10000 011101	0111001010110010
D8.4	100	01000	111001	0010	000110	1101	10001 111110	0011001100110101
D9.4	100	01001	100101	1101	100101	0010	10001 111010	0110001110100101
D10.4	100	01010	010101	1101	010101	0010	10001 110110	1010001110010101
D11.4	100	01011	110100	1101	110100	0010	10001 011100	1011001010110001
D12.4	100	01100	001101	1101	001101	0010	10001 101110	1010100100110101
D13.4	100	01101	101100	1101	101100	0010	10001 011010	1010101010100101
D14.4	100	01110	011100	1101	011100	0010	10001 100110	0011100110010101
D15.4	100	01111	010111	0010	101000	1101	10001 010110	0110101010010101
D16.4	100	10000	011011	0010	100100	1101	10010 111011	0010101100101110
D17.4	100	10001	100011	1101	100011	0010	10010 111101	0011001100111010
D18.4	100	10010	010011	1101	010011	0010	10010 111001	0110001110101010
D19.4	100	10011	110010	1101	110010	0010	10010 110101	1010001110011010
D20.4	100	10100	001011	1101	001011	0010	10010 101011	1011000100101110
D21.4	100	10101	101010	1101	101010	0010	10010 101101	1010100100111010
D22.4	100	10110	011010	1101	011010	0010	10010 011001	1010101010101010
D23.4	100	10111	111010	0010	000101	1101	10010 100101	0011100110011010
D24.4	100	11000	110011	0010	001100	1101	10011 101000	0011100110101001
D25.4	100	11001	100110	1101	100110	0010	10011 101100	0110100100111001
D26.4	100	11010	010110	1101	010110	0010	10011 101010	0111000100101101
D27.4	100	11011	110110	0010	001001	1101	10011 100110	0011000100011101
D28.4	100	11100	001110	1101	001110	0010	10011 011000	0110101010101001
D29.4	100	11101	101110	0010	010001	1101	10011 011100	0011101000111001
D30.4	100	11110	011110	0010	100001	1101	10011 010010	0011001010001101
D31.4	100	11111	101011	0010	010100	1101	10011 010100	1010101010011001

			8B/10B Encoder/Decoder				8B/16B Encoder/Decoder	
	Bits		Disparity <0		Disparity >0		9B/11B Outputs	Hamming Outputs
Data Byte Name	*765*	*43210*	*abcdei*	*fghj*	*abcdei*	*fghj*	*Information Bits*	*Information and Control bits (p,o,n..c,b,a)*
D0.5	101	00000	100111	1010	011000	1010	10100 111011	0110001101100110
D1.5	101	00001	011101	1010	100010	1010	10100 100101	0111000111010010
D2.5	101	00010	101101	1010	010010	1010	10100 011011	1010101001100110
D3.5	101	00011	110001	1010	110001	1010	10100 000101	1011100011010010
D4.5	101	00100	110101	1010	001010	1010	10100 100011	0110100111000110
D5.5	101	00101	101001	1010	101001	1010	10100 100111	0011100101010110
D6.5	101	00110	011001	1010	011001	1010	10100 010011	0011101011000110
D7.5	101	00111	111000	1010	000111	1010	10100 010111	0110101001010110
D8.5	101	01000	111001	1010	000110	1010	10101 111010	1010001101100101
D9.5	101	01001	100101	1010	100101	1010	10101 101010	0011100101100101
D10.5	101	01010	010101	1010	010101	1010	10101 010110	1010101001010101
D11.5	101	01011	110100	1010	110100	1010	10101 110110	0110001101010101
D12.5	101	01100	001101	1010	001101	1010	10101 011010	0110101001100101
D13.5	101	01101	101100	1010	101100	1010	10101 100010	1010100111000101
D14.5	101	01110	011100	1010	011100	1010	10101 011100	0111001001110001
D15.5	101	01111	010111	1010	101000	1010	10101 100100	1011000111010001
D16.5	101	10000	011011	1010	100100	1010	10110 011001	0110101001101010
D17.5	101	10001	100011	1010	100011	1010	10110 111001	1010001101101010
D18.5	101	10010	010011	1010	010011	1010	10110 010101	1010101001011010
D19.5	101	10011	110010	1010	110010	1010	10110 110101	0110001101011010
D20.5	101	10100	001011	1010	001011	1010	10110 011011	0010001011101110
D21.5	101	10101	101010	1010	101010	1010	10110 101001	0011100101101010
D22.5	101	10110	011010	1010	011010	1010	10110 010011	1011001001001110
D23.5	101	10111	111010	1010	000101	1010	10110 100001	1010100111001010
D24.5	101	11000	110011	1010	001100	1010	10111 011000	1010101001101001
D25.5	101	11001	100110	1010	100110	1010	10111 111000	0110001101101001
D26.5	101	11010	010110	1010	010110	1010	10111 010100	0110101001011001
D27.5	101	11011	110110	1010	001001	1010	10111 110100	1010001101011001
D28.5	101	11100	001110	1010	001110	1010	10111 010010	0111001001001101
D29.5	101	11101	101110	1010	010001	1010	10111 100000	0110100111001001
D30.5	101	11110	011110	1010	100001	1010	10111 010110	0010001011011101
D31.5	101	11111	101011	1010	010100	1010	10111 100100	0011100101011001

			8B/10B Encoder/Decoder				8B/16B Encoder/Decoder	
	Bits		Disparity <0		Disparity >0		9B/11B Outputs	Hamming Outputs
Data Byte Name	*765*	*43210*	*abcdei*	*fghj*	*abcdei*	*fghj*	*Information Bits*	*Information and Control bits (p,o,n..c,b,a)*
D0.6	110	00000	100111	0110	011000	0110	11000 111001	1011011100100010
D1.6	110	00001	011101	0110	100010	0110	11000 110101	0111011100010010
D2.6	110	00010	101101	0110	010010	0110	11000 101011	0110010110100110
D3.6	110	00011	110001	0110	110001	0110	11000 100111	1010010110010110
D4.6	110	00100	110101	0110	001010	0110	11000 011011	0011011010100110
D5.6	110	00101	101001	0110	101001	0110	11000 011101	0010111010110010
D6.6	110	00110	011001	0110	011001	0110	11000 001011	1010110010100110
D7.6	110	00111	111000	0110	000111	0110	11000 001101	1011010010110010
D8.6	110	01000	111001	0110	000110	0110	11001 010110	0011011010010101
D9.6	110	01001	100101	0110	100101	0110	11001 110100	1011011100010001
D10.6	110	01010	010101	0110	010101	0110	11001 000110	1010110010010101
D11.6	110	01011	110100	0110	110100	0110	11001 100110	0110010110010101
D12.6	110	01100	001101	0110	001101	0110	11001 011110	1010011000110101
D13.6	110	01101	101100	0110	101100	0110	11001 001100	0111010010110001
D14.6	110	01110	011100	0110	011100	0110	11001 001010	0110110010100101
D15.6	110	01111	010111	0110	101000	0110	11001 101010	1010010110100101
D16.6	110	10000	011011	0110	100100	0110	11010 001001	0110110010101010
D17.6	110	10001	100011	0110	100011	0110	11010 101001	1010010110101010
D18.6	110	10010	010011	0110	010011	0110	11010 011101	1010011000111010
D19.6	110	10011	110010	0110	110010	0110	11010 100101	0110010110011010
D20.6	110	10100	001011	0110	001011	0110	11010 010011	0010111010001110
D21.6	110	10101	101010	0110	101010	0110	11010 000011	1011010010001110
D22.6	110	10110	011010	0110	011010	0110	11010 010101	0011011010011010
D23.6	110	10111	111010	0110	000101	0110	11010 000101	1010110010011010
D24.6	110	11000	110011	0110	001100	0110	11011 101010	0010110100101101
D25.6	110	11001	100110	0110	100110	0110	11011 101100	0011010100111001
D26.6	110	11010	010110	0110	010110	0110	11011 101000	0110010110101001
D27.6	110	11011	110110	0110	001001	0110	11011 100100	1010010110011001
D28.6	110	11100	001110	0110	001110	0110	11011 011000	0011011010101001
D29.6	110	11101	101110	0110	010001	0110	11011 011100	0110011000111001
D30.6	110	11110	011110	0110	100001	0110	11011 001000	1010110010101001
D31.6	110	11111	101011	0110	010100	0110	11011 000100	0110110010011001

			8B/10B Encoder/Decoder				8B/16B Encoder/Decoder	
	Bits		Disparity <0		Disparity >0		9B/11B Outputs	Hamming Outputs
Data Byte Name	*765*	*43210*	*abcdei*	*fghj*	*abcdei*	*fghj*	*Information Bits*	*Information and Control bits (p,o,n..c,b,a)*
D0.7	111	00000	100111	0001	011000	1110	11100 010011	0110011011000110
D1.7	111	00001	011101	0001	100010	1110	11100 100011	0011010111000110
D2.7	111	00010	101101	0001	010010	1110	11100 001011	0110110001100110
D3.7	111	00011	110001	1110	110001	0001	11100 101011	1010010101100110
D4.7	111	00100	110101	0001	001010	1110	11100 010111	0011011001010110
D5.7	111	00101	101001	1110	101001	0001	11100 100111	0110010101010110
D6.7	111	00110	011001	1110	011001	0001	11100 001101	0111010001110010
D7.7	111	00111	111000	1110	000111	0001	11100 100101	0010110111010010
D8.7	111	01000	111001	0001	000110	1110	11101 001010	1010110001100101
D9.7	111	01001	100101	1110	100101	0001	11101 101010	0110010101100101
D10.7	111	01010	010101	1110	010101	0001	11101 001100	1011010001110001
D11.7	111	01011	110100	1110	110100	1000	11101 100110	1010010101010101
D12.7	111	01100	001101	1110	001101	0001	11101 011010	0011011001100101
D13.7	111	01101	101100	1110	101100	1000	11101 010010	1010011011000101
D14.7	111	01110	011100	1110	011100	1000	11101 011100	0010111001110001
D15.7	111	01111	010111	0001	101000	1110	11101 000110	0110110001010101
D16.7	111	10000	011011	0001	100100	1110	11110 100101	1010010101011010
D17.7	111	10001	100011	0111	100011	0001	11110 110011	0010011101001110
D18.7	111	10010	010011	0111	010011	0001	11110 101001	0110010101101010
D19.7	111	10011	110010	1110	110010	0001	11110 011001	0011011001101010
D20.7	111	10100	001011	0111	001011	0001	11110 000101	0110110001011010
D21.7	111	10101	101010	1110	101010	0001	11110 000011	0111010001001110
D22.7	111	10110	011010	1110	011010	0001	11110 001001	1010110001101010
D23.7	111	10111	111010	0001	000101	1110	11110 010001	1010011011001010
D24.7	111	11000	110011	0001	001100	1110	11111 001010	0010010011101101
D25.7	111	11001	100110	1110	100110	0001	11111 100100	0110010101011001
D26.7	111	11010	010110	1110	010110	0001	11111 001000	0110110001101001
D27.7	111	11011	110110	0001	001001	1110	11111 100000	0011010111001001
D28.7	111	11100	001110	1110	001110	0001	11111 010010	0010111001001101
D29.7	111	11101	101110	0001	010001	1110	11111 010100	0011011001011001
D30.7	111	11110	011110	0001	100001	1110	11111 010000	0110011011001001
D31.7	111	11111	101011	0001	010100	1110	11111 000100	1010110001011001

b] Transmitted Character and Control Sequences (SC/$\overline{D}$ High)

				8B/10B Mode				8B/16B Mode	
		D_i Inputs		Disparity <0		Disparity >0		9B/11B Outputs	Hamming Outputs
Data Byte Name	*Code Name*	*765*	*43210*	*abcdei*	*fghj*	*abcdei*	*fghj*	*Information 11-bits*	*Information and Control bits (p,o,n..c,b,a)*
K28.0	C0.0	000	00000	001111	0100	110000	1011	00000010111	0101101010010110
K28.1	C1.0	000	00001	001111	1001	110000	0110	00000111101	0100101110110010
K28.2	C2.0	000	00010	001111	0101	110000	1010	00111010000	1100101011001001
K28.3	C3.0	000	00011	001111	0011	110000	1100	00011111000	0101001110101001
K28.4	C4.0	000	00100	001111	0010	110000	1101	00100111101	1000101101110010
K28.5	C5.0	000	00101	001111	1010	110000	0101	00011000010	1101100010001101
K28.6	*C6.0*	000	00110	001111	0110	110000	1001	00111100000	1001100111001001
K28.7	*C7.0*	000	00111	001111	1000	110000	0111	00111111000	1001001101101001
K23.7	*C8.0*	000	01000	111010	1000	000101	0111	01000101111	1100010100110110
K27.7	*C9.0*	000	01001	110110	1000	001001	0111	01100000111	0101110001010110
K29.7	*C10.0*	000	01010	101110	1000	010001	0111	01100001001	1101010011100010
K30.7	*C11.0*	000	01011	011110	1000	100001	0111	01100001011	1001110001100110
Idle	*C0.1*	001	00000	-K28.5+, D21.4, D21.5,D21.5				K28.5, D21.4, D22.4, D22.4	
R_RDY	*C1.1*	000	00001	-K28.5+, D21.4, D10.2, D10.2				K28.5, D21.4, D14.3, D14.3	
EOFxx	*C2.1*	001	00010	-K28.5, Dn.xx0		+K28.5, Dn.xx1		K28.5	
CVS	*C0.7*	111	00000	100111	1000	011000	0111	11100111101	0010011101110010
-K28.5	*C1.7*	111	00001	001111	1010	001111	1010	K28.5	
+K28.5	*C2.7*	111	00010	110000	0101	110000	0101	K28.5	
DVS	*C4.7*	111	00100	110111	0101	001000	1010	CVS	
Other Invalid Words				CVS				CVS	

c] Received Character and Control Sequences (SC/$\overline{D}$ High)

		Outputs			8B/10B Mode				8B/16B Mode	
			Q_i		Disparity <0		Disparity >0		11B/9B Inputs	Hamming Inputs
Data Byte Name	Code Name	RVS	765	43210	abcdei	fghj	abcdei	fghj	abcdeifghj	*Information and Control Bits*
K28.0	C0.0	0	000	00000	001111	0100	110000	1011	00000010111	0101101010010110
K28.1	C1.0	0	000	00001	001111	1001	110000	0110	00000111101	0100101110110010
K28.2	C2.0	0	000	00010	001111	0101	110000	1010	00111010000	1100101011001001
K28.3	C3.0	0	000	00011	001111	0011	110000	1100	00011111000	0101001110101001
K28.4	C4.0	0	000	00100	001111	0010	110000	1101	00100111101	1000101101110010
K28.5	C5.0	0	000	00101	001111	1010	110000	0101	00011000010	1101100010001101
K28.6	*C6.0*	0	000	00110	001111	0110	110000	1001	00111100000	1001100111001001
K28.7	*C7.0*	0	000	00111	001111	1000	110000	0111	00111111000	1001001101101001
K23.7	*C8.0*	0	000	01000	111010	1000	000101	0111	01000101111	1100010100110110
K27.7	*C9.0*	0	000	01001	110110	1000	001001	0111	01100000111	0101110001010110
K29.7	*C10.0*	0	000	01010	101110	1000	010001	0111	01100001001	1101010011100010
K30.7	*C11.0*	0	000	01011	011110	1000	100001	0111	01100001011	1001110001100110
C-SOF	*C7.1*	0	001	00111	K28.1 followed by K28.7					
P-SOF	*C7.2*	0	010	00111	K28.5 followed by K28.7					
CVS	*C0.7*	1	111	00000	non-existent Code					
-K28.5	*C1.7*	1	111	00001	-K28.5+ received & disparity >0				Never	
+K28.5	*C2.7*	1	111	00010	+K28.5- received & disparity <0				Never	
DVS	*C4.7*	1	111	00100	Valid Code and Disparity Error				Never	