Microprocessor-Compatible Multiplexers Facilitate Video Switching Designs

Gareth Powell

For many new communications systems—such as ISDN (Integrated Services Digital Network), cable TV, and local area networks (LANs)—traditional switching techniques have become inadequate. To meet the demands of these applications, semiconductor switching devices must now handle wider bandwidths and offer more on-chip features to achieve low chip-count solutions. Higher integration, smaller packages, easier device paralleling/combining, and improved dynamic performance are essential features for designing large-capacity switching systems.

Analog video information is frequently digitized for processing in frame grabbers, TV standard converter (e.g., NTSC to PAL), time-base correction, special effects, or merely as a means of reducing noise levels and enhancing resolution. However, the price paid for the advantages of the digital technique is the substantially wider bandwidth occupied by the digitized signal. Thus, in a typical 8-bit conversion, the sampling rate must be at least three times the chrominance subcarrier frequency of 4.43 MHz: that is, 13.3 MHz. Thus, the bit rate is 8 x 13.3 = 106.44 Mbps. This bandwidth requirement precludes the use of a majority of components and switching techniques commonly employed in video systems.

Video switching applications, such as high-definition TV, digital video equipment, and broadcast studio switches have forced improvements in semiconductor switch performance. This application note presents the benefits of the DG534A and DG538A in a diverse range of wideband switching applications, highlighting the devices' performance features and providing useful circuit design techniques.

Device Description

The DG538A is a wideband single-ended 8-to-1 or differential 4-channel multiplexer. Several DG538As can easily be configured to create a more complex matrix or to handle crosspoint functions. The DG534A, similar to the DG538A with half the number of channels, is a 4-to-1 single-ended or a 2-to-1 differential multiplexer.

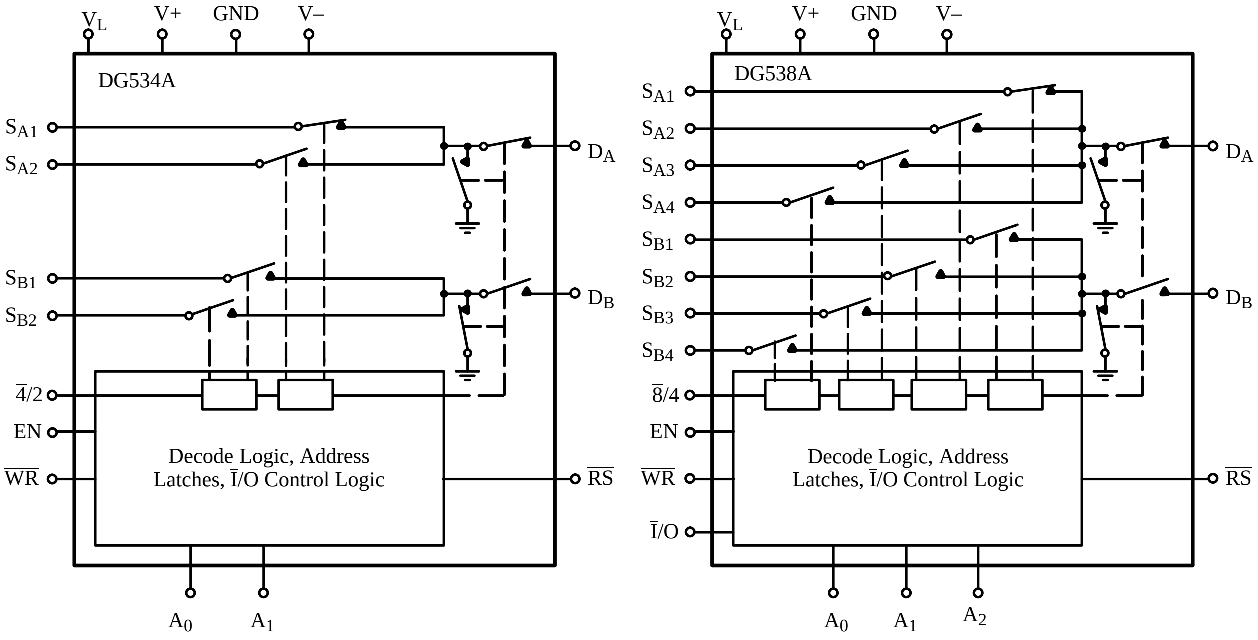

V_L
V+
GND
V–
DG534A
S_{A1}
S_{A2}
D_A
S_{B1}
S_{B2}
D_B
$\overline{4}/2$
EN
$\overline{WR}$
Decode Logic, Address Latches, $\overline{I}$/O Control Logic
$\overline{RS}$
A_0
A_1
V_L
V+
GND
V–
DG538A
S_{A1}
S_{A2}
S_{A3}
S_{A4}
S_{B1}
S_{B2}
S_{B3}
S_{B4}
D_A
D_B
$\overline{8}/4$
EN
$\overline{WR}$
$\overline{I}$/O
Decode Logic, Address Latches, $\overline{I}$/O Control Logic
$\overline{RS}$
A_0
A_1
A_2

Figure 1. DG534A and DG538A Functional Schematics

D/CMOS processing enables these devices to be optimized for high-frequency signal handling with low on-resistance while on-chip CMOS circuitry provides all the level shifting, logic interfacing, and latching functions that permit easy system design. The switch structure utilizes lateral n-channel DMOS transistors configured in a "T" arrangement, as shown in Figure 1. The "T" switches are arranged into two groups. Each group is selected by the second-stage "L" switches. This two-level switching configuration minimizes channel capacitance and off-state signal crosstalk (maximizes off-isolation).

For comparison, Figure 2 shows the single-channel crosstalk characteristics of the DG538A video multiplexer and the industry-standard DG508A. Note the 35-dB performance improvement of the DG538A versus the standard CMOS 8-channel multiplexer.

The DG538A data sheet specifies all-hostile crosstalk. This is a much more rigorous test specification than single-channel crosstalk since it requires all seven "off" channels to be tied together. More crosstalk signal is seen at the switch under these test conditions because there are seven parallel paths, as opposed to only one, and the crosstalk contribution of the package and the PC board are also more apparent. Nevertheless, the all-hostile crosstalk of the DG534A and DG538A approaches –70 dB at 5 MHz, easily meeting most video switching requirements.

It is not merely the "T" and "L" configurations that give improved crosstalk. Careful on-chip layout and optimum device sizing were also required. A small device exhibits lowintrinsic capacitances, but has greater on-resistance and, hence, will give a greater insertion loss. However, by employing DMOS (double diffused MOS) FETs for the switches, an excellent compromise between $r_{DS(on)}$ and intrinsic capacitances is achieved.

Figure 5 shows a cross section of an n-channel device made with the D/CMOS process, incorporating DMOS and PMOS transistors. The fabrication of the "T" switch is shown.

The short-channel feature of the DMOS devices offers 8 to 10 times less channel capacitance than a conventional lateral NMOS transistor for a given $r_{DS(ON)}$. Figure 5 also shows the n- and p-channel devices that form the CMOS logic interface, level shifting, and latches.

The cross section shows many pn junctions which would become forward biased if signals applied to the device were more negative than the "p" substrate. For this reason, when handling ac signals, the substrate is connected to a negative voltage (V–) to allow signals to swing below ground.

Using a negative supply also optimizes device capacitances. The body effect on DMOS devices causes the on-state capacitance to change as a function of V–. For a fixed analog signal, C_{ON} reduces exponentially as the source-to-substrate voltage increases (see Figure 3). Other performance benefits can be attained by choosing a particular V– (see Figure 19).

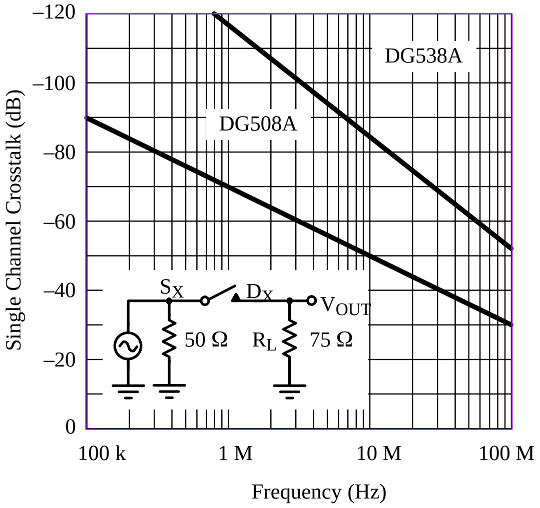


Figure 2. DG538A/DG508A Single-Channel Crosstalk vs. Frequency

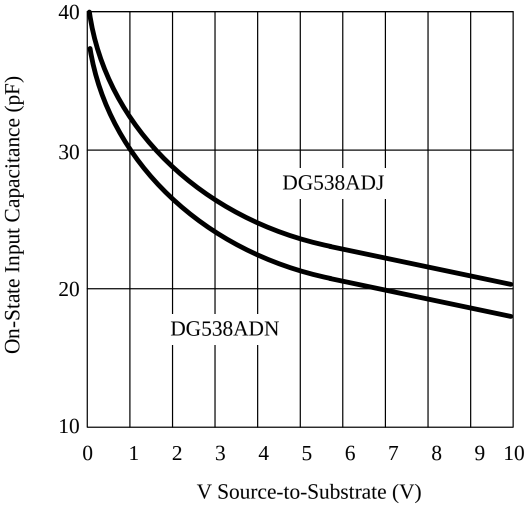


Figure 3. DG538A On-State Input Capacitance vs. Source-to-Substrate/Voltage

In the event of an overvoltage (analog signal going more than a diode drop beyond V–), the pn junction between the source or drain and the substrate will forward bias, causing a large current to flow. This fault current will not damage the device as long as the current flow is less than 20 mA. However, low-impedance source circuitry is typical of many applications; for example, the characteristic impedance of video systems is 75 Ω. Thus, a means of current limiting should be employed in circuits where overvoltage transients are possible. Figure 4 shows a transient protection scheme that uses a diode in V–. This diode (normally forward biased) becomes reverse biased with overvoltage transients, thus eliminating fault current flow.

Positive overvoltages (> V+) are a different problem. The switch will merely turn off (no enhancement) if signals approach or exceed V+. The DMOS drain diffusion has a fairly high breakdown voltage (typically > 30 V). Large avalanche currents can flow during breakdown, therefore, either the signals must be externally clamped to avoid exceeding breakdown voltage, or a means of external fault current limiting should be adopted. Since the source diffusion will only develop a voltage during the switch “on” state, under normal supply conditions this breakdown (source-to-substrate) is unlikely to occur due to the device turning off when the source voltage, V_S, approaches V+. Therefore, external positive overvoltage protection is only required when transients or overvoltages are expected to be in excess of +30 V.

Addressing and Logic

A DG538A device can be configured as a single-ended or as a differential multiplexer by applying the appropriate logic to the $\overline{8}$/4 pin. When this pin is high (the differential condition), address A_2 is not used. Note that DA and DB must be externally connected for the single-ended mode.

The logic trip-point reference for the internal comparators is derived from logic voltage, V_L, i.e., when V_L = +5 V, true TTL compatibility is achieved. In this case, the logic levels required to activate the various control pins($\overline{8}$/4, $\overline{I}$/O, EN, A_X, $\overline{WR}$, $\overline{RS}$) are 0.8 V and 2 V. Variation of V_L enables the switching threshold to be shifted (Figure 6).

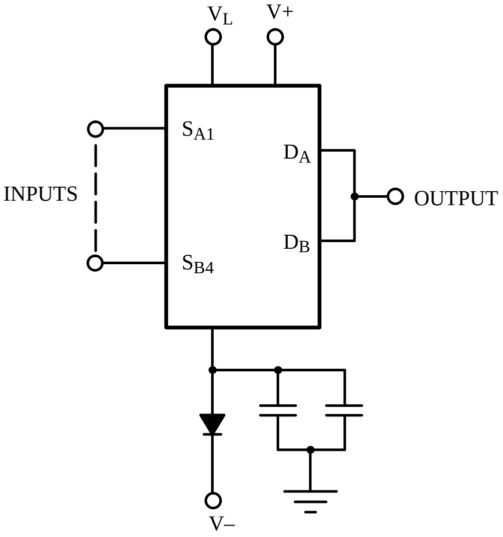


Figure 4. Negative Overvoltage Transient Protection

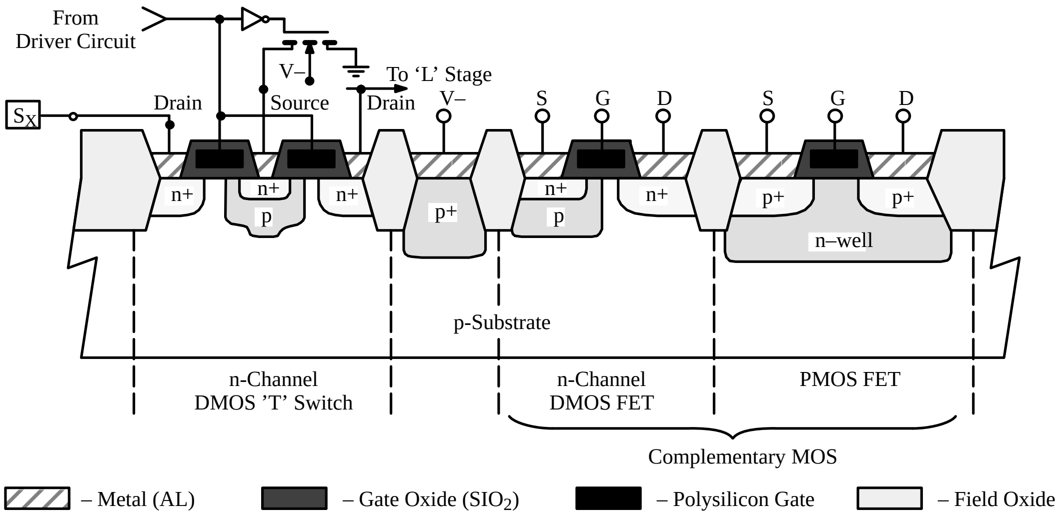


Figure 5. Cross Section of the D/CMOS Process

The DG538A and DG534A have tri-state latches on their address pins, allowing three modes of operation:

1. **Input Data.** In this mode, the multiplexer accepts data applied to A_X causing appropriate switch selection. This mode is selected by the following logic conditions:

$\bar{\text{I}}$/O = 0 (input mode)
$\overline{\text{WR}}$ = 0 (latches transparent)
EN = 1 (device enabled)
$\overline{\text{RS}}$ = 1

2. **High Impedance.** In this mode, the address pins assume a high impedance (open circuit) state. It is selected by

$\bar{\text{I}}$/O = 0
$\overline{\text{WR}}$ = 1 (data latched state)
EN = X
$\overline{\text{RS}}$ = 1

The tri-state (high-impedance) mode of operation is particularly useful in microprocessor-controlled systems. It enables many devices to be paralleled on a common control bus without significant loading. This feature helps fulfill the demands of large matrix systems.

By decoding the microprocessor's address bus, the DG538A/DG534A can be activated to respond to logic control signals transmitted by the microprocessor on its data bus, only when required to do so.

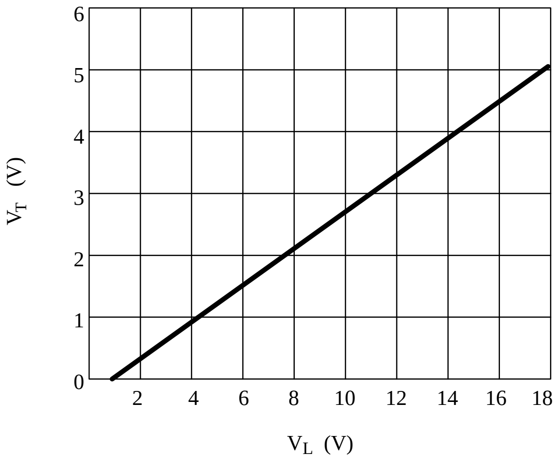


Figure 6. DG538A Switching Threshold vs. Logic Supply Voltage (V_L)

3. **Output Data.** The last data written to the latches are reflected as logic outputs on A_0, A_1, and A_2. This is achieved when

$\bar{\text{I}}$/O = 1 (output mode)
$\overline{\text{WR}}$ = 1
EN = 1
$\overline{\text{RS}}$ = 1

The "data readback" feature is convenient in handshaking functions where "route-selected" status monitoring is required. This also eliminates additional peripheral devices for this function. Data readback may also be used to preserve the switch configuration during and after a power failure to the microprocessor. Normally after power failure, the microprocessor must go through a complete system reset routine. Provided power to the DG538A/DG534A has not been disrupted, when the microprocessor's power is re-established, it can poll the multiplexers and resume immediate control. This capability simplifies microprocessor software requirements and reduces service interruptions.

In the address output state, the address outputs can source or sink 0.4 mA. Logic high from the address output is V_L. When operating V_L at voltages higher than +5 V, it is important to consider the possibility of damaging effects on TTL devices connected to the address bus.

To ease microprocessor interfacing, additional control pins are featured.

- **$\overline{\text{WR}}$**. This input activates the data latches for strobing-in an address word when $\overline{\text{WR}}$ goes low (i.e., transparent latches). The strobing signal is normally obtained by decoding the microprocessor address data. This pin eliminates the need for external latches or peripheral devices such as $\bar{\text{I}}$/O ports for connection to the microprocessor's bus.

- **$\overline{\text{RS}}$**. This input initiates a direct reset command that clears all data latches and opens all switches. This pin can be used as a "master reset." It is of particular significance during system power-up since the microprocessor's reset control pin may be used to clear all switches prior to channel/routing selection. Thus, the software used to sequentially clear all multiplexers is unnecessary.

Figure 7 illustrates the ease of microprocessor interface with the DG538A and shows an alternate use for the $\overline{\text{RS}}$ function as a chip-select control in a 32-to-1 video switching application. The $\overline{\text{RS}}$ function overrides all other control signals. Note that $\overline{\text{RS}}$ is not a latched input. An external D-type latch is required so that A_4 can be connected directly to the data bus. A_0 to A_3 are latched internally to the DG538A.

The 8085 microprocessor data bus (after having its low-order address lines demultiplexed) connects directly to the address inputs (A_0 to A_2) on all the DG538As and on A_3 and A_4. The system responds to stimuli on the data bus only when a write command is received. A write signal is produced by first decoding three (or more) lines of the high-order address lines using a 3-to-8 decoder and then gating (OR) one of the decoder output lines with the microprocessor's $\overline{WR}$ output. This enables switch selection only when the appropriate address data is received; otherwise, switch states remain latched and their control inputs are all in the high-impedance mode, leaving the microprocessor's data bus free to execute other routines.

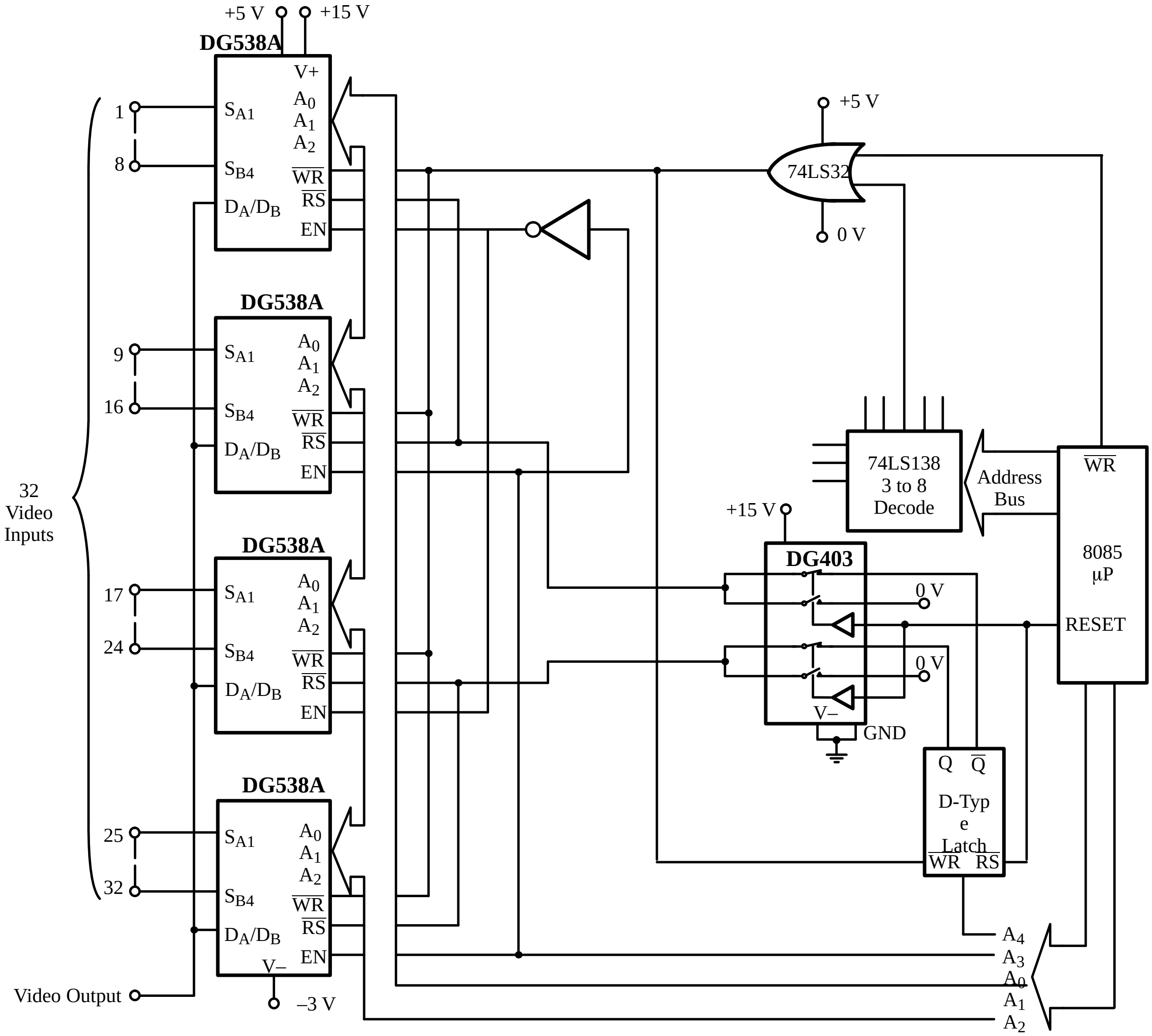

+5 V
+15 V
DG538A
V+
S_A1
S_B4
D_A/D_B
A_0
A_1
A_2
WR
RS
EN
1
8
9
16
17
24
25
32
32 Video Inputs
Video Output
V–
–3 V
+5 V
74LS32
0 V
74LS138 3 to 8 Decode
Address Bus
WR
8085 µP
RESET
+15 V
DG403
0 V
0 V
V–
GND
Q
Q
D-Type Latch
WR
RS
A_4
A_3
A_0
A_1
A_2

Figure 7. A 32-Channel Single-Ended Wideband Multiplexer Controlled by an 8085

Table 1. Microprocessor Timing Compatibility

Parameter		DG538A/4	8085A	8085A-2	Z80	6800
t_{WW} Width of Control Low ($\overline{WR}$)	(ns)	200 (min)	400 (min)	230 (min)	360 (min)	470 (min)
t_{DW} Data Valid to Trailing Edge of Write	(ns)	100 (min)	420 (min)	230 (min)	200 (min)	575 (min)
t_{WD} Data alid to Trailing Edge of Write	(ns)	50 (min)	100 (min)	60 (min)	100 (min)	150 (min)

Switch inputs 1 to 32 can be selected by a 5-bit word transmitted on the data bus coinciding with a write signal.

Even though the $\overline{RS}$ pins on the four DG538A devices are used for chip select, a direct reset or no-channel-selected condition is easily achieved using a CMOS analog switch (DG403), as shown in Figure 7.

An important consideration for direct microprocessor interface is input timing compatibility. Table 1 shows minimum input timing requirements of the DG538A/DG534A compared with the corresponding minimum output timing specifications of some popular microprocessors.

Methods of interface to other microprocessors are shown in Figure 8. An address decoder (for a memory-mapped type of operation) is required for all interface circuits. Various gating arrangements are required, depending on the microprocessor's peripheral control output architecture.

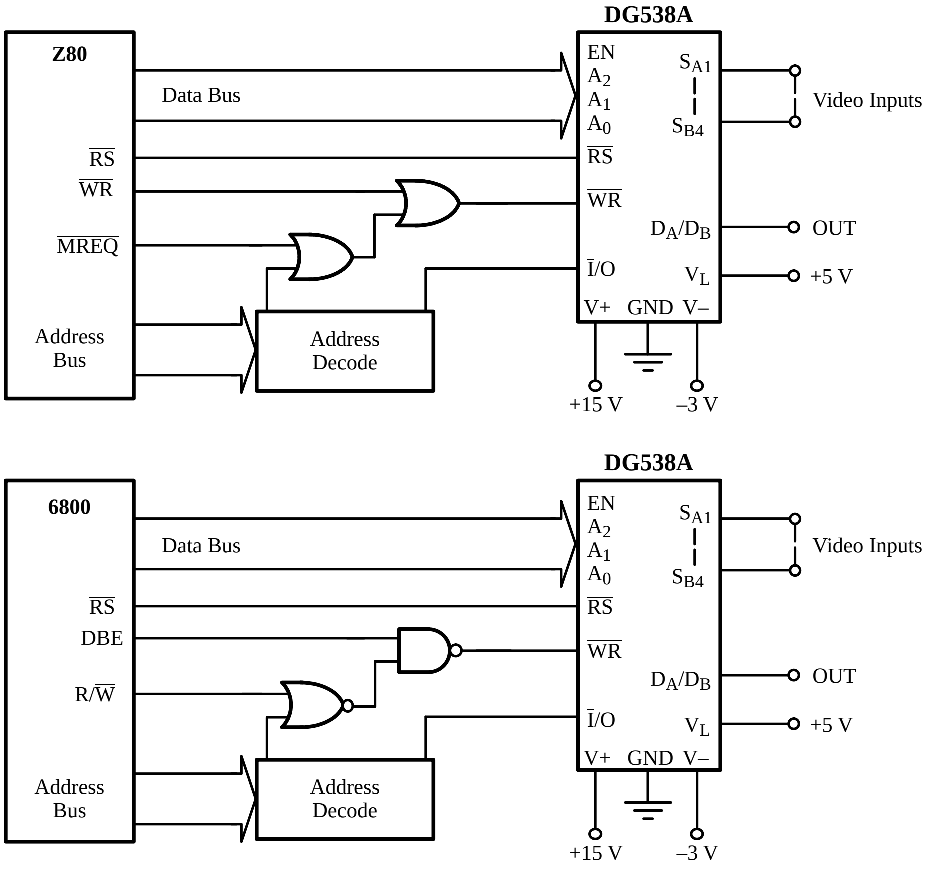

DG538A
Z80
Data Bus
RS
WR
MREQ
Address Bus
Address Decode
EN
A2
A1
A0
RS
WR
I/O
SA1
SB4
Video Inputs
DA/DB
OUT
VL
+5 V
V+ GND V–
+15 V
–3 V
DG538A
6800
Data Bus
RS
DBE
R/W
Address Bus
Address Decode
EN
A2
A1
A0
RS
WR
I/O
SA1
SB4
Video Inputs
DA/DB
OUT
VL
+5 V
V+ GND V–
+15 V
–3 V

Figure 8. Other Microprocessor Interfaces

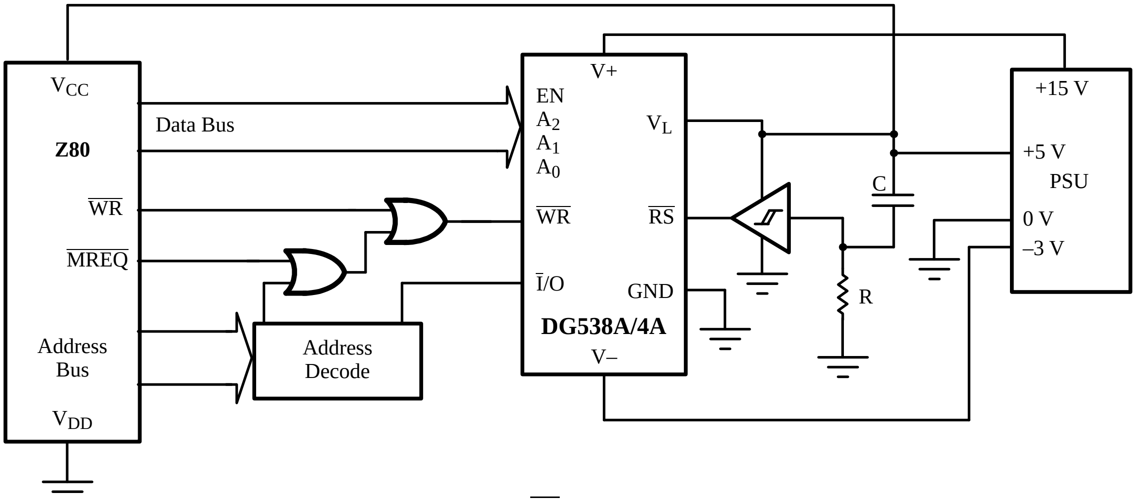


Figure 9. Using $\overline{RS}$ as a Power-Up Fail-Safe

In some cases, it might be convenient to use $\overline{RS}$ as a power-up failsafe. The circuit shown in Figure 9 illustrates a method for using $\overline{RS}$ as a power-up delay circuit. This allows microprocessor buses or control logic sources to stabilize after power-up before the DG538A responds to control signals. During power-up, indeterminate logic states and/or transients might be present on control or data lines. The RC values are set to ignore spurious control signals.

Characteristics

The DG538A and DG534A data sheets include detailed operating characteristics, typical parameters, and limit values. The important dynamic characteristics, such as crosstalk and bandwidth, are plotted against frequency (to 100 MHz) to help designers predict system performance, since these parameters are measures of the on-state and off-state multiplexer performance.

Specialized video specifications not included on the data sheet are presented here to provide a better understanding of the devices' performance and suitability for a wide range of video and general wideband switching applications.

Bandwidth is a measure of the on-state performance and is defined as the frequency at which the signal falls –3 dB from the low-frequency insertion loss figure. Figure 10 shows the typical frequency characteristics of the DG538A measured on an HP8573A network analyzer.

Since a multiplexer channel exhibits on-resistance, $r_{DS(on)}$, and on-state capacitance, $C_{(on)}$, increasing signal frequencies are progressively attenuated. However, it is a common misconception that the bandwidth can be calculated from the $r_{DS(on)}$ and $C_{(on)}$ specifications given on the data sheet.

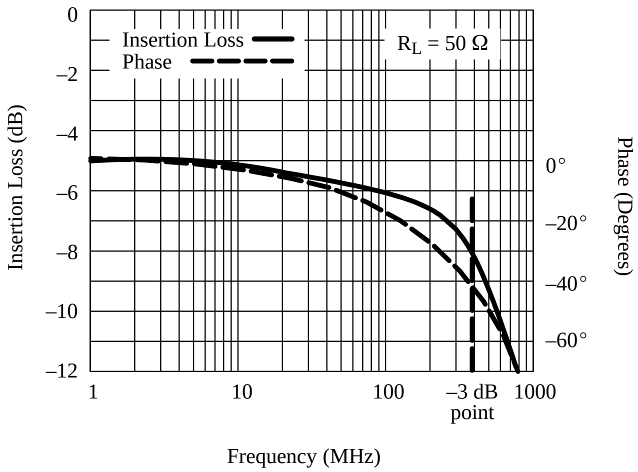
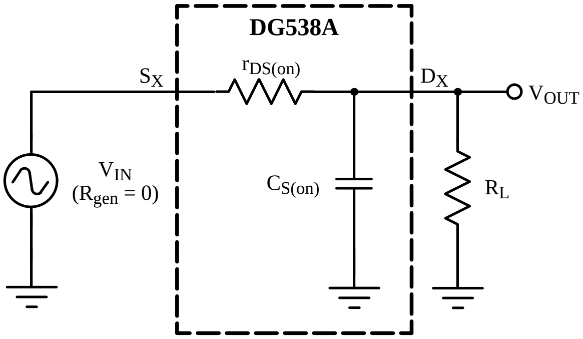
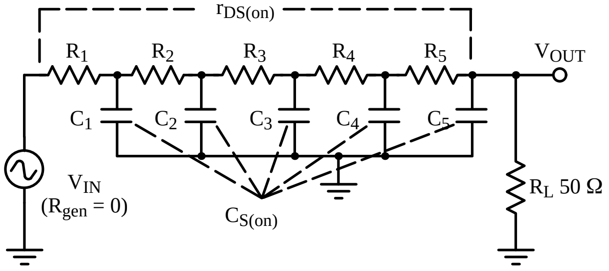


Figure 10. DG538A Bandwidth and Phase Response


DG538A
$r_{DS(on)}$
S_X
D_X
V_{OUT}
V_{IN}
(R_{gen} = 0)
$C_{S(on)}$
R_L

Insertion Loss (dB) = 20 log (V_{OUT}/V_{IN})

Figure 11. Erroneous Model for Frequency Response Calculations


$r_{DS(on)}$
R_1
R_2
R_3
R_4
R_5
V_{OUT}
C_1
C_2
C_3
C_4
C_5
V_{IN}
(R_{gen} = 0)
$C_{S(on)}$
R_L 50 Ω

R_1 to R_5 = 8 Ω (Since $r_{DS(on)}$ = 40 Ω)
C_1 to C_5 = 4.6 pF (Since $C_{S(on)}$ = 23 pF)

Figure 12. Five-Stage RC Model

The –3 dB frequency for the model shown in Figure 11 is given by the formula:

$$-3\ \text{dB} = \frac{1}{2\pi\left(\frac{R_L \times r_{DS(on)}}{R_L + r_{DS(on)}}\right)C_{(on)}}$$

Substituting $R_L = 50\ \Omega$, $r_{DS(on)} = 50\ \Omega$, and $C_{(on)} = 23$ pF give an $f_{-3\ dB} \approx 310$ MHz.

The measured frequency response for the same 50 Ω load (Figure 10) shows a –3 dB point of over 500 MHz. This apparent discrepancy results because the $r_{DS(on)}$ and $C_{(on)}$ are distributed among the five DMOS FETs that form the “T” and “L” switches.

A SPICE simulation of the model shown in Figure 12 gave a 510 MHz –3 dB point, which is much closer to the measured value (see Figure 13).

Note that the equivalent five-stage RC circuit shown in Figure 12 is not a complete model of the DG538A transmission path. However, it does illustrate the effect of distributed parameters. An actual model would be far more complex, with other reactive elements that incorporate package capacitances, inductances, etc.

In the absence of a better model, the circuit shown in Figure 12 is useful for predicting bandwidths in crosspoint systems where the frequency response will be affected by paralleling devices (Figure 14).

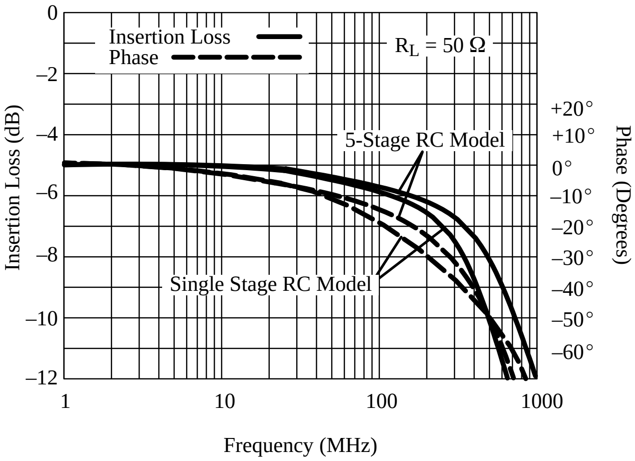


Figure 13. Bandwidth and Phase Response for the Models of Figures 11 and 12

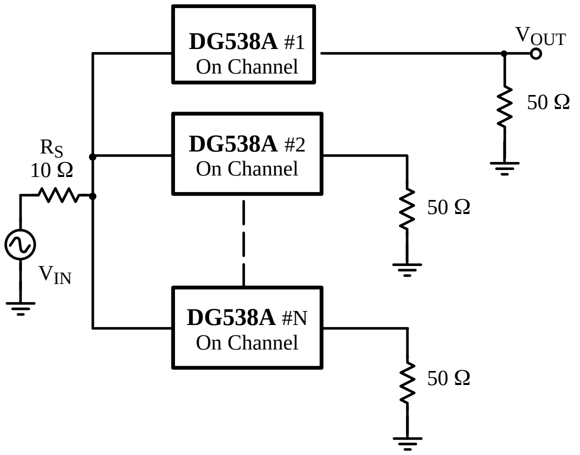

DG538A #1
On Channel
V_{OUT}
50 Ω
R_S
10 Ω
DG538A #2
On Channel
50 Ω
V_{IN}
DG538A #N
On Channel
50 Ω

Figure 14. Equivalent Diagram of an 8   N Crosspoint Using DG538As When One V_{IN} Is Selected to All Outputs

Table 2.

Number of Parallel Channels	–3 dB Bandwidth [20 Log (V_{OUT}/V_{IN})]	
	Single RC Stage (Figure 11)	**5 Stage RC (Figure 12)**
1	280 MHz	400 MHz
2	250 MHz	340 MHz
4	225 MHz	260 MHz
8	185 MHz	200 MHz
16	170 MHz	160 MHz

A 10 Ω source impedance is included in Figure 14. This source impedance simulates the low-output impedance of a video buffer amplifier generally employed at the input to the matrix. The simulation results of the circuit, using single-stage and five-stage models for different numbers of parallel channels, are shown in Table 2.

The “flat” response over the bandwidth of interest is an important requirement for video applications. The Independent Television Companies Association (ITCA) specifies the following gain/frequency limits for a video switching matrix.

Mid- to high-frequency response:

± 0.1 dB between 100 kHz and 5.5 MHz

± 0.25 dB between 5.5 MHz and 8 MHz

Above 8 MHz:

“Response shall fall continuously and smoothly”

Although this specification is for 625-line PAL systems used in the United Kingdom, it is a typical specification and similar to other standards, such as NTSC and SECAM.

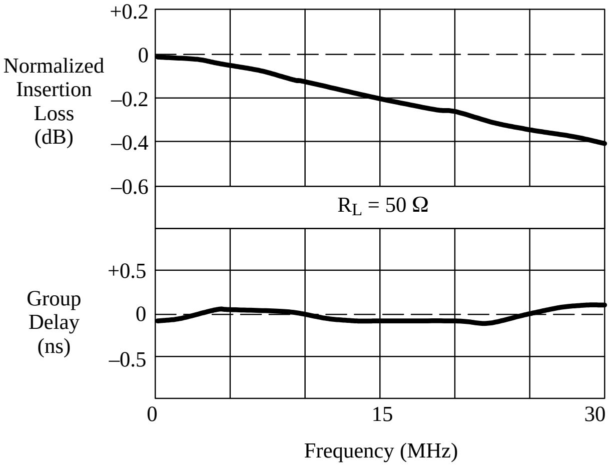


Figure 15. DG538A/DG534A Group Delay and Normalized Insertion Loss Response to 30 MHz

High-definition TV has much tighter tolerances since it requires bandwidths to 25 MHz. The 0- to 30-MHz frequency response of the DG538A and DG534A, shown in Figure 15, is well within the required limits.

Group Delay, sometimes called envelope delay or deviation from linear phase, is the phase-shift rate of change through a circuit or equipment with respect to frequency, or alternatively, non-linearity of the group frequency response. In a transient waveform which has a continuous spectrum, the group delay becomes the transmission time of a packet of spectral components. It follows, therefore, that if the group delay is constant for all the required bandwidth, there will be no difference in the arrival times of the various spectral components which make up the bandwidth.

Because many different frequency components make up a video waveform, this parameter is of particular relevance in video applications. The measured group delay response of the DG538A is shown in Figure 15. It satisfies the most demanding video requirements. The plot shows less than 500 ps over a 30 MHz frequency range.

Non-Linearity Distortions

Color video can be divided into two groups: component video [separate red (R), green (G), and blue (B) signals] and composite video, which contains color and brightness (chroma and luma) information in a single waveform.

Composite video has various specifications that relate to the interaction of chroma and luma. In particular, differential gain and differential phase must be specified for video components or systems. To illustrate these distortions, consider the basic composite TV signal.

Figure 16 shows a typical color TV signal. The sync pulses, occurring every 64 µs, synchronize horizontal line deflection.

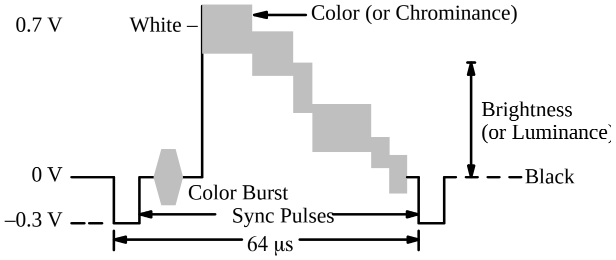


Figure 16. Basic Composite TV Signal

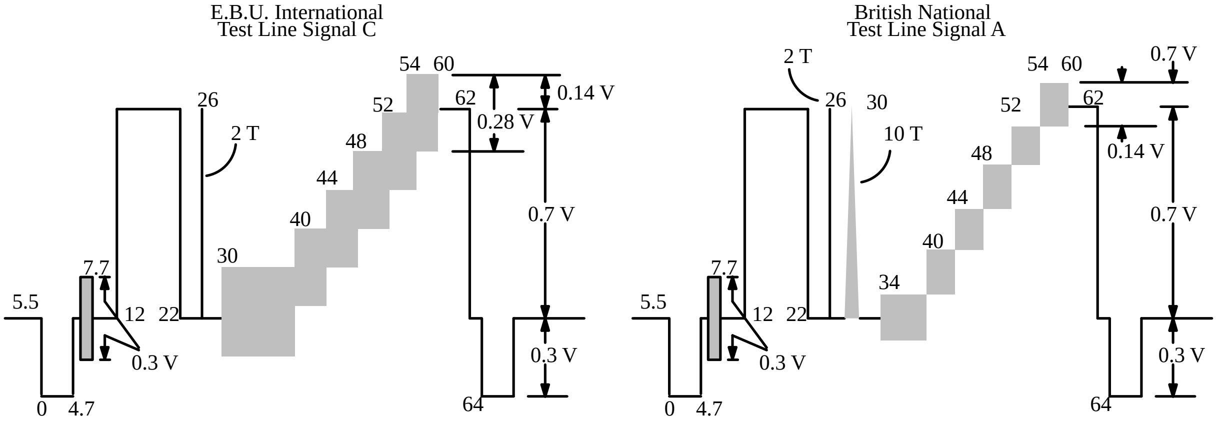

E.B.U. International
Test Line Signal C
5.5
0
4.7
7.7
12
22
0.3 V
26
2 T
30
40
44
48
52
54
60
62
64
0.14 V
0.28 V
0.7 V
0.3 V
British National
Test Line Signal A
5.5
0
4.7
7.7
12
22
0.3 V
2 T
26
30
10 T
34
40
44
48
52
54
60
62
64
0.7 V
0.14 V
0.7 V
0.3 V

Figure 17. Standard Test Waveforms

The color signal contains both luminance and chrominance. When this signal is processed by a domestic TV receiver, the red, green, and blue components are recovered and used to modulate three individual electron beams.

The amplitude of the chroma contains the color intensity (color saturation), and its phase difference with respect to the color burst determines the blend (hue) of color.

- **Differential Phase.** Measured in degrees, this is the phase shift of the color subcarrier resulting from a change in the amplitude of the associated luminance component. Differential phase shows up in NTSC pictures as a change in hue, a color change more noticeable in a shaded area of the picture.

Frequency related phase shifts (as opposed to differential phase) will cause no change in picture quality since both color burst and chrominance are equally shifted.

- **Differential Gain.** Expressed as a percentage, this is a form of distortion resulting from changes in the amplitude of the chrominance signal as a function of luminance amplitude.

The effect on NTSC and PAL pictures is a change in color saturation with changing luminance level. The eye is fairly tolerant to differential gain since the resulting picture changes are fairly subtle. For instance, a brightly colored car traveling from a sunny area of the picture to a shaded area would appear as though its body color intensity had suddenly changed.

Specialized equipment is employed to measure differential phase and gain. Specifications, such as ITCA, require standard test signals and dedicated test equipment and techniques. Recognized standard test waveforms are shown in Figure 17.

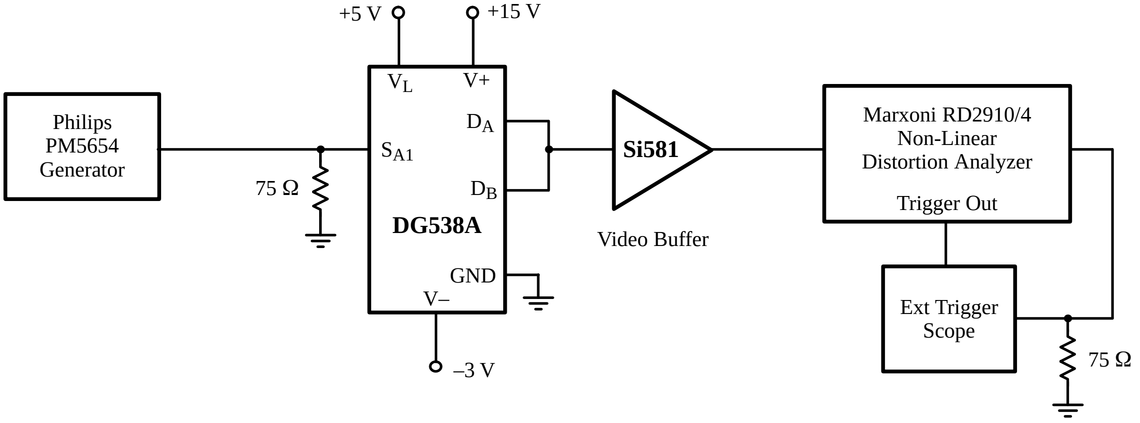

+5 V
+15 V
Philips
PM5654
Generator
75 Ω
V_L
V+
S_{A1}
D_A
D_B
DG538A
GND
V–
–3 V
Si581
Video Buffer
Marxoni RD2910/4
Non-Linear
Distortion Analyzer
Trigger Out
Ext Trigger
Scope
75 Ω

Figure 18. Differential Phase and Gain Test Configuration

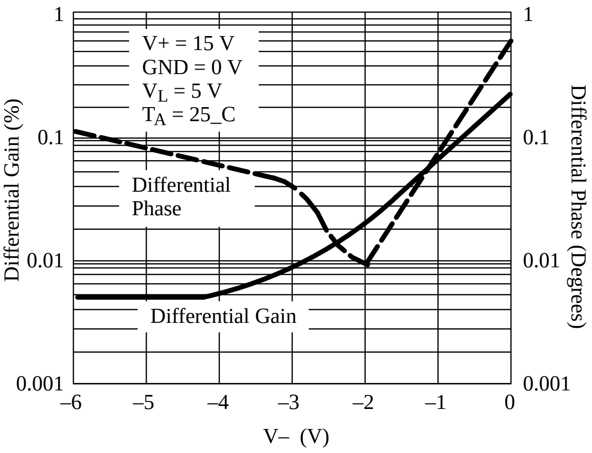


Figure 19. Differential Gain/Phase vs. V–

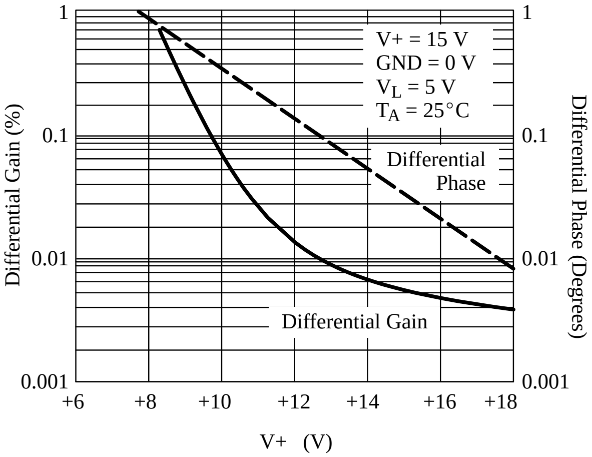


Figure 20. Differential Gain/Phase vs. V+

Chrominance amplitude variation over the five Average Picture Levels (APLs) indicates differential gain. Differential gain is expressed as the greatest change (in %) of the chrominance amplitude with respect to its amplitude at black level. Similarly, differential phase is the greatest change in chrominance phase shift referred to the phase of the chrominance at black level. Test configuration and equipment used to characterize the DG538A for differential phase and gain are shown in Figure 18.

The equipment shown in Figure 18 must be correctly terminated, or signal amplitudes are affected giving erroneous results. A video buffer (Si581) provides a 75-Ω resistance to the signal generator, and the signal through the switch meets the standard 1-V_{p-p} amplitude. Since most applications use a video buffer following the multiplexer, this configuration is very realistic. The inherent non-linearity of the circuit (bypassing the DG538A) is first measured, and then subtracted from the measured value when the device under test is inserted.

Supply Variation Effects on Non-linearity Distortion

Supply voltage variation causes various transmission impedance changes. Therefore, both differential phase and gain are heavily dependent on power supply values. Figures 19 and 20 show the typical variation of differential phase and gain versus positive and negative supply. These curves enable optimization of performance by careful choice of supplies.

Generally, high-performance video switching systems require less than 0.5% differential gain and 0.5° differential phase. Therefore, limits of 0.1% and 0.1° could be applied to a single switch component. Figure 21 shows the power supply operating area that achieves < 0.1% and 0.1° performance for DG538A devices.

Handling Precautions

All MOS devices can be damaged by the presence of excessively high electric fields in the gate-oxide region. Such fields can cause the gate oxide to rupture, rendering the device unusable. Mishandling MOS devices may cause catastrophic damage from the build-up of static electricity in the human body, which can reach many thousands of volts.

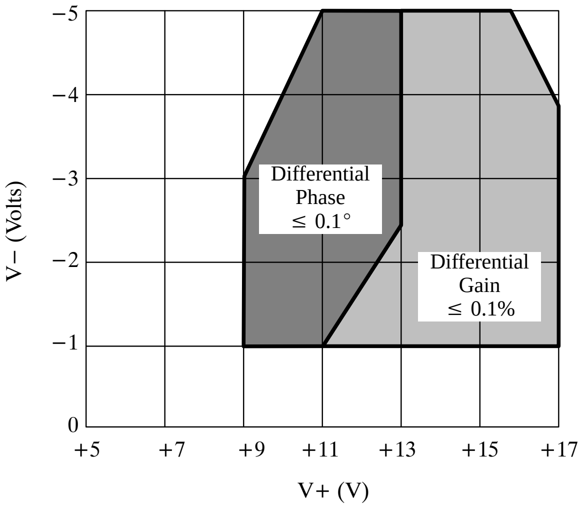


Figure 21. DG538A Supply Ranges to Maintain <0.1% and 0 Differential Gain and Phase

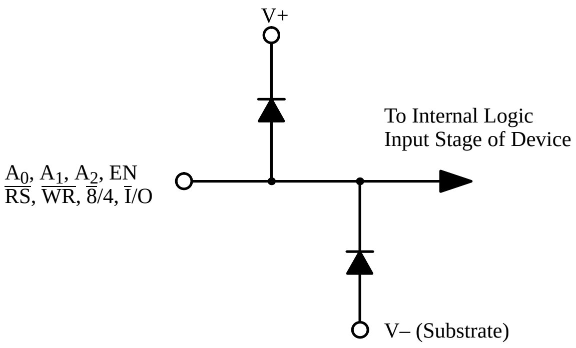


Figure 22. ESD Protection Circuit

To reduce electrostatic discharge (ESD) susceptibility in the DG534A/DG538A, all logic inputs are protected by the circuit shown in Figure 22.

Typically, the diode clamps provide ESD protection up 2 KV on any logic input pin. Standard static handling and assembly precautions should, nevertheless, be used to ensure maximum reliability. Anti-static clothing, conductive table-tops, grounded-tip soldering irons, and ensuring that all voltage sources are turned off during the insertion or removal of devices or PCBs are recommended.

Power-Up Sequence

A pn junction exists between V_L and V+, which, in the event of V_L being present before V+ (i.e. $V_L > V+$,), will become forward biased. Under these conditions, large currents may flow. To avoid this condition, the power-up sequence should ensure that V_L does not come up before V+. Normally, this will not present a problem if V+ and V_L are derived from the same power supply.

Printed Circuit Board (PCB) Layout and Decoupling

Selecting components optimized for high-frequency signals does not guarantee adequate circuit performance. Good layout techniques are also very important. At high frequencies, stray capacitance between long adjacent signal lines can provide low impedance paths that couple with one another. Power supply lines can couple rf signals from one circuit to another. Components or sockets that protrude on a PCB surface may act as small antennas which pick up or radiate rf signals. To avoid these problems, be sure signal paths between components are as short as possible and make extensive use of ground planes and shielding between adjacent signal paths.

The DG534A and DG538A have ground pins isolating adjacent channels. These, when connected to grounded shielding paths, give excellent ac performance.

Power supplies should be bypassed by the use of decoupling capacitors mounted as close to the device supply pins as possible. This is of particular importance for the DG534A/DG538A since the device substrate connects directly to V–. Two capacitors on each power supply are recommended. A ceramic capacitor of 0.01 to 0.1 μF, provides high-frequency signal bypassing, and a tantalum capacitor (1 to 10 μF) is adequate to bypass low frequencies. Further decoupling can be achieved by adding a low-value series resistor (e.g. 51 Ω) in the supply line.

Components should be assembled on a PCB in a low profile. The DG538A, for example, is available as a 28-pin quad surface-mount package or a 28-pin dual-in-line package. The latter has poorer crosstalk performance because it has a larger lead frame and because the device pins are connected through the board. Using sockets should be avoided because they degrade device performance significantly.

Applications

Applications for the DG538A and DG534A are many and varied, ranging from high-frequency signal switching to lower-frequency, low-level signal routing.

Video Systems

The DG534A and DG538A multiplexers are ideal for many wideband switching applications, such as high-resolution financial data networks, forward-looking infrared (FLIR) detectors (night vision systems), CAT (computer aided tomography) scanners, and NMR (nuclear magnetic resonance) medical imaging.

Figure 23 shows the DG538A as an 8-to-1 video source selector. This circuit has many applications in industrial process monitoring systems or in security systems where eight separate video cameras connect to a single monitor in a sequence. The circuit uses three bits to automatically select each source in turn. An override feature can be incorporated to disable the counter and provide manual channel selection.

An example of a differential configuration application is shown in Figure 24. This circuit may be used in component video systems such as TV camera signal routing. Two devices are required for routing four separate RGB sources and their corresponding audio, sync, or timecode signals. Note that the channel select or address bus is common to all devices.

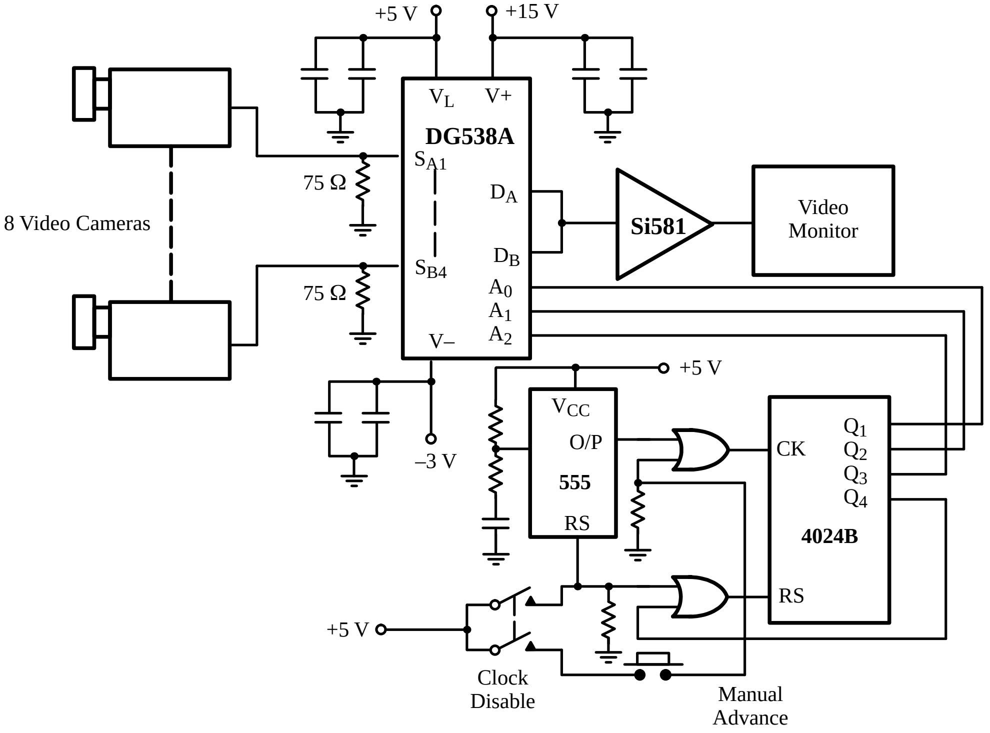

+5 V
+15 V
VL
V+
DG538A
SA1
SB4
DA
DB
A0
A1
A2
V–
75 Ω
75 Ω
8 Video Cameras
Si581
Video Monitor
+5 V
VCC
O/P
555
RS
–3 V
CK
Q1
Q2
Q3
Q4
4024B
RS
+5 V
Clock Disable
Manual Advance

Figure 23. Basic Closed-Circuit TV System

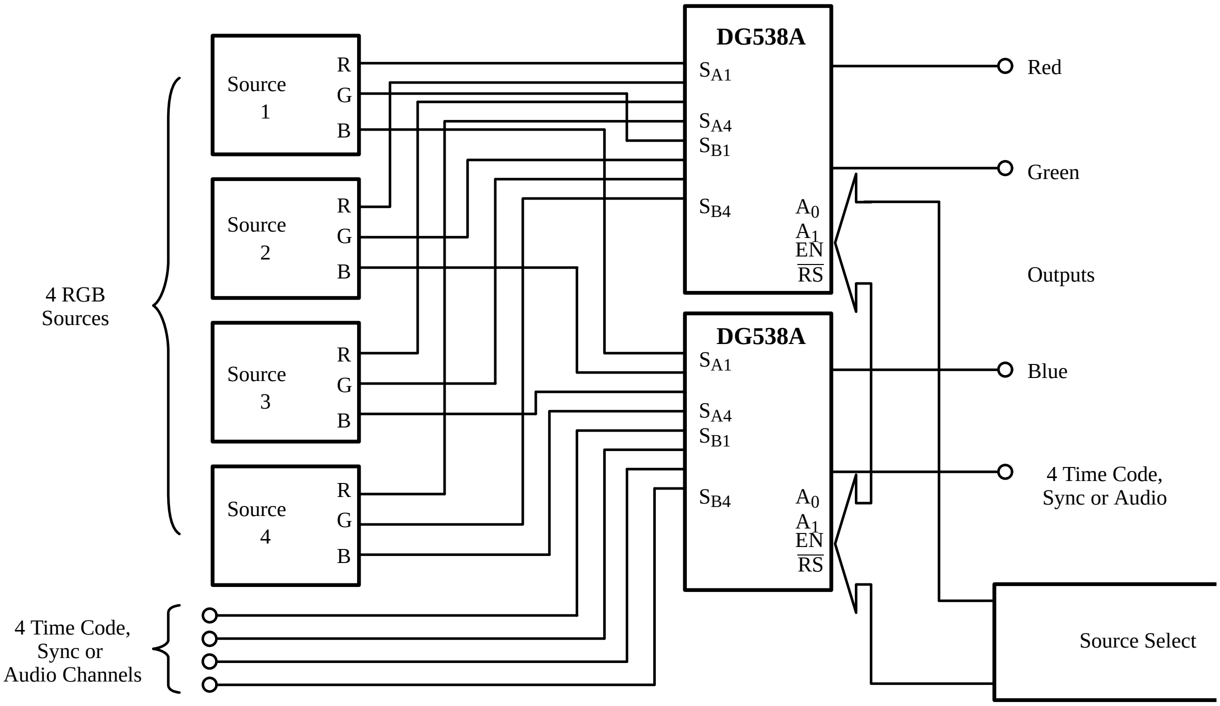

Source 1
Source 2
Source 3
Source 4
R
G
B
4 RGB Sources
4 Time Code, Sync or Audio Channels
DG538A
SA1
SA4
SB1
SB4
A0
A1
EN
RS
DG538A
Red
Green
Outputs
Blue
4 Time Code, Sync or Audio
Source Select

Figure 24. An RGB Plus Timecode, Sync, or Audio Switching System

A majority of video applications require crosspoint configurations, where a number of inputs must be switched to a number of outputs. Applications requiring this type of matrix switching (both analog and digital) range from PCM (Pulse Code Modulation) or telecommunications data switching to financial information routing. A basic crosspoint configuration (8 x 4) is shown in Figure 25. The data-write control strobes address information to each DG538A. In turn, the actual address data (for the required route) is present on the address or route-assign bus. Video output buffers are normally used to drive lengths of 75 Ω coax cable.

In Figure 25, the loading of switch capacitances and buffer input impedances on a given video source will vary, depending on the number of outputs. For example, when a

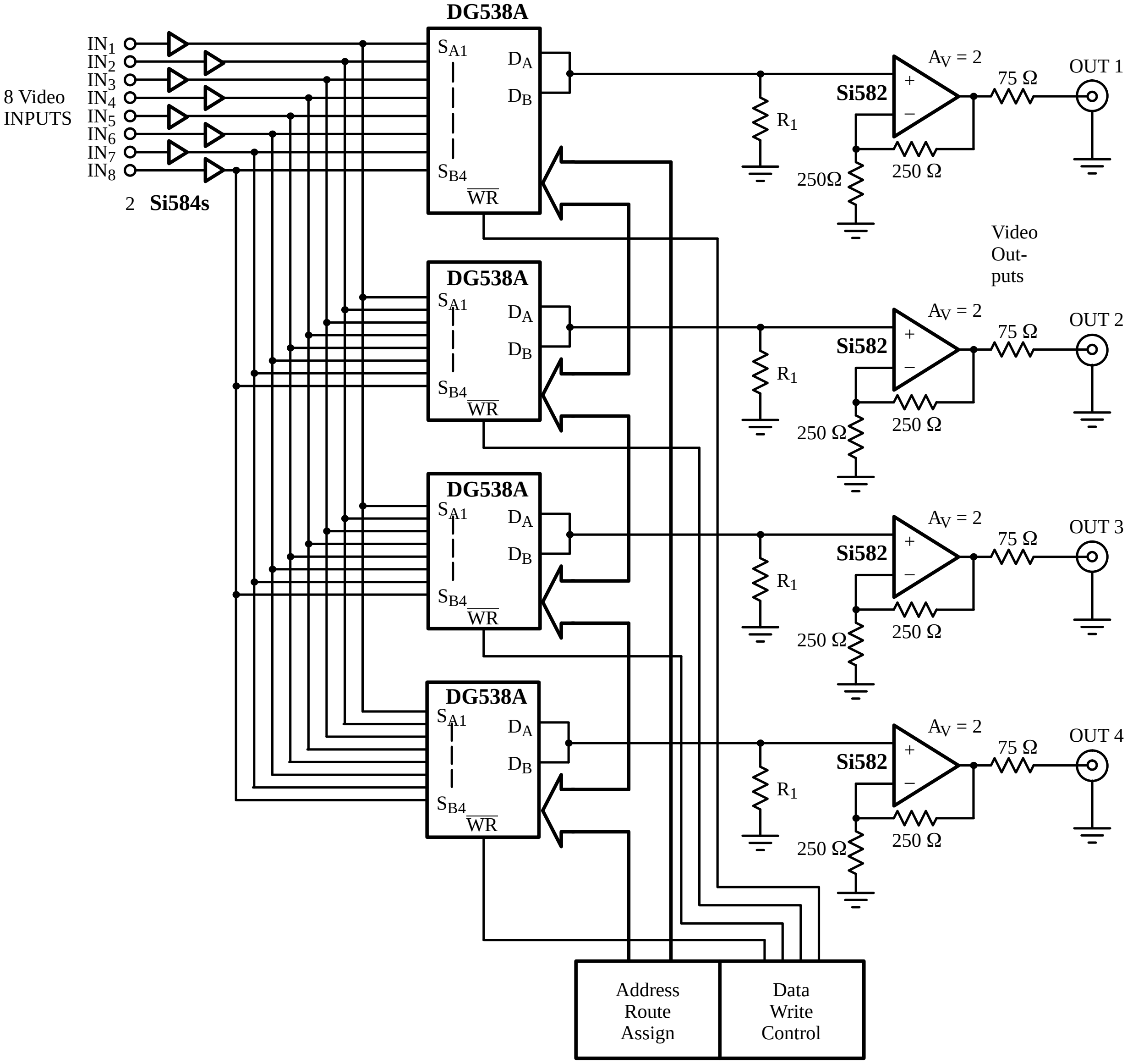

DG538A
IN_1
IN_2
IN_3
IN_4
IN_5
IN_6
IN_7
IN_8
8 Video INPUTS
2 Si584s
S_{A1}
S_{B4}
D_A
D_B
$\overline{WR}$
R_1
250Ω
250 Ω
Si582
$A_V = 2$
75 Ω
OUT 1
OUT 2
OUT 3
OUT 4
Video Out-puts
Address Route Assign
Data Write Control

Figure 25. An 8 4 Crosspoint Switch

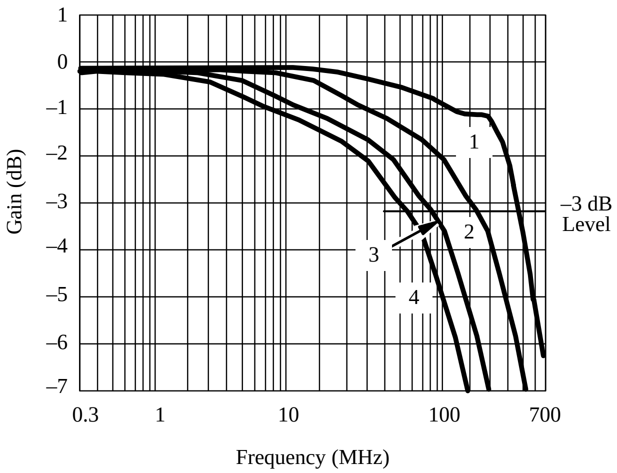


Figure 26. Frequency Response of 8 4 Matrix

single source is switched to all four outputs, it is loaded by 4 x $C_{S(on)}$ (∼92 pF) plus 4 x C_{in} of buffer. This increased loading affects the frequency response and phase shift of the output signal. Note that R_1 is used to set the bandwidth/insertion loss relationship.

Figure 26 illustrates this effect by showing the frequency response of a single output signal for an increasing number of channels connected to the source. Additional channels (2, 3, and 4) are loaded with 10 kΩ to simulate the input impedance of video buffers.

Figure 27 shows measured frequency response of a typical crosspoint circuit using four DG538ADJs and both an Si581 wideband buffer and an Si582 wideband op-amp. This circuit arrangement forms the nucleus of any video or wideband crosspoint system, and provides practically transparent switching of video signals to standards sufficient to meet broadcast or HDTV requirements. The data sheets for the Si581 and Si582 provide greater detail for individual performance characteristics, although the in-circuit performance under “real life” conditions is not so apparent.

The circuit employs a front-end input buffer (Si581) to provide the correct termination impedance and drive the crosspoint circuit. R_S is required to minimize gain peaking caused by the loading capacitance. The response shows an increased peaking at single “on” switch conditions due to the capacitance reduction. Although the value of R_S can be optimized to reduce the peak, the frequency at which it occurs is out-of-band in terms of video. Generally, low pass filtering is employed at some stage to eliminate any out-of-band effects.

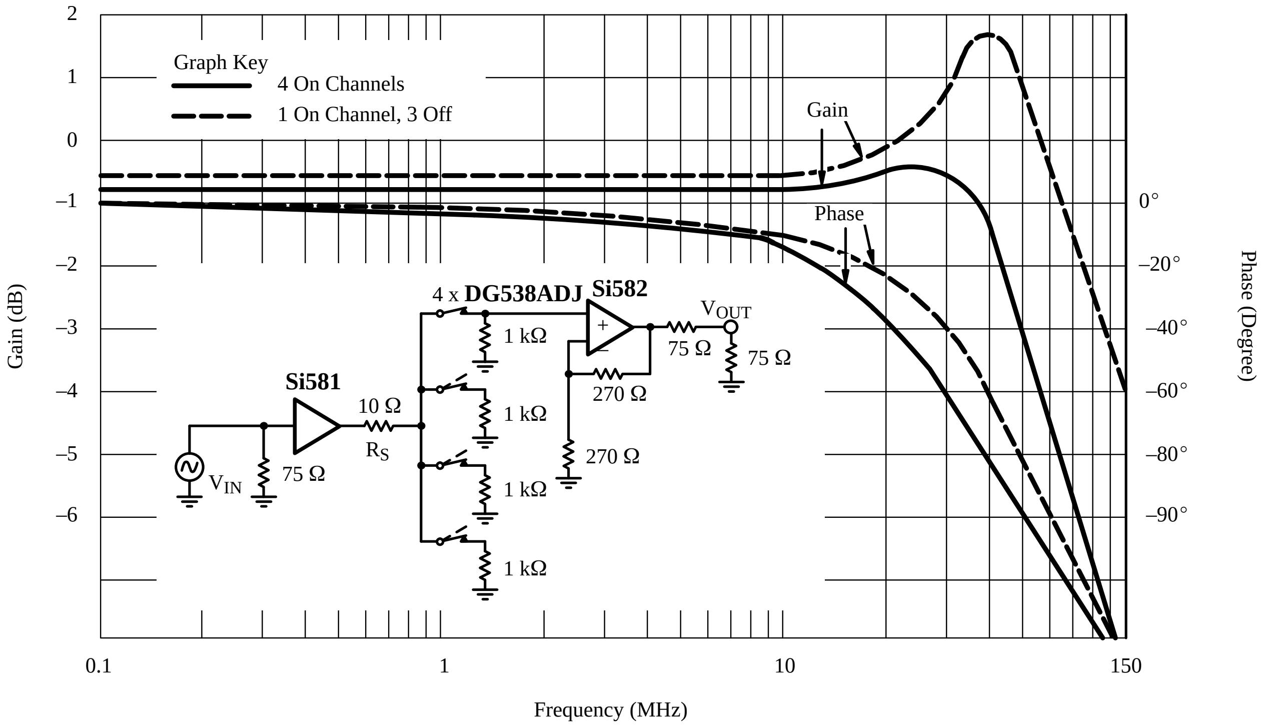


Figure 27. Frequency Response of Four DG538As Buffered with Si581 and Si582

The output amplifier (Si582) provides a gain of two, again for correct matching, since the 75 Ω output impedance driving a 75 Ω load gives a two to one division of the signal. Note that the non-inverting input to the Si582 is padded down to 1 kΩ to optimize switch bandwidth. It is feasible that reduction of this value could be employed to further increase switch bandwidth, although more output gain might then be required to compensate for losses, which in turn causes a reduction in the Si582 bandwidth. Circuit optimization would normally be practically performed in preliminary design stages.

The graph shows that even with worst case loading (i.e. 4 channels "on") the gain flatness and phase shift is well within the required limits of even the most demanding video standards.

It is conceivable that even more outputs could be driven by a single Si581, especially in less demanding applications.

Alternatively, discrete input buffer designs such as source or emitter follower circuits that require only a transistor (FET or bipolar) plus a few passive components could be used for front-ends, although the cost versus performance ratio is questionable, since the performance reduction could necessitate every individual DG538A channel buffered. This obviously increases component costs, board real-estate and power supply requirements.

Follower circuits can be as simple as shown in Figure 28 for certain applications. This circuit exhibits a dc offset which can be removed using the dc restoration (or black level clamp) circuit of Figure 30. This arrangement of buffering and clamping is used for capacitively coupled systems.

Some applications might demand a dc-coupled system that retains all the dc contents of the signal applied to the buffer. For these applications, the follower circuit shown in Figure 29 may be used. This circuit, which exhibits a low dc offset of < 40 mV, uses a Siliconix U440 dual FET to maintain simplicity and efficient use of board space. Lower offsets can be accomplished by using monolithic buffers such as Siliconix' Si581.

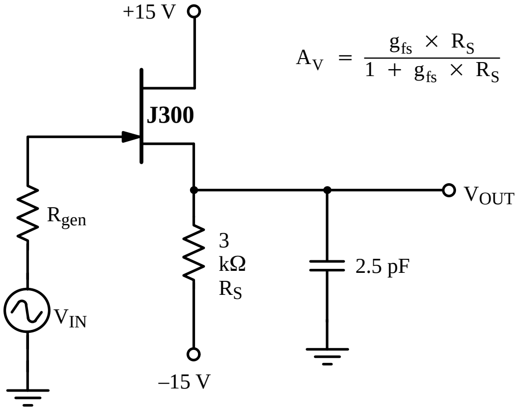


Figure 28. Single FET Source Follower

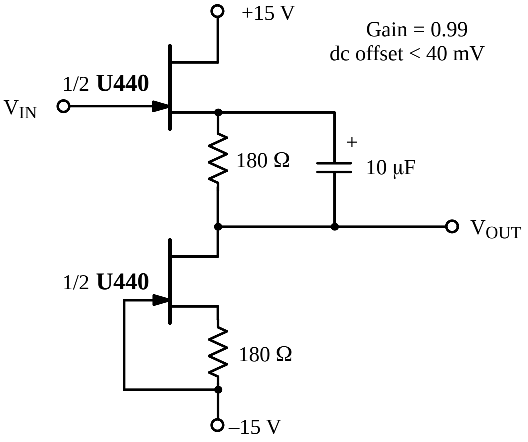


Figure 29. FET Buffer Uses Matched JFETs for Low dc Offset

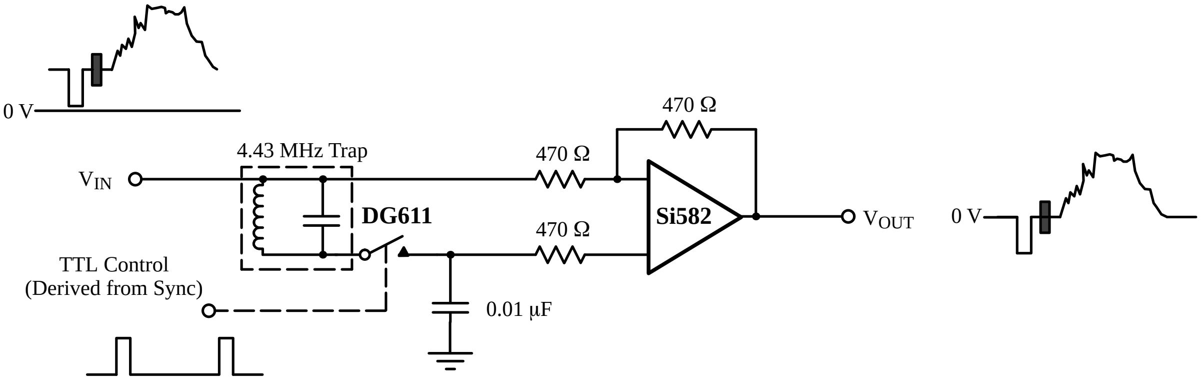


Figure 30. Simple Black-Level Clamp Circuit

In the circuit shown in Figure 28, $f_{-3\ dB} \approx 300$ MHz for $R_{gen} = 75\ \Omega$, while offering a low input capacitance. The output signal for this circuit has some dc offset; however, this is not usually a problem because the output of the matrix is frequently ac coupled with a dc restoration (black-level clamp) circuit employed at a later stage. Figure 30 shows a simple black-level clamp circuit that employs a DG611 high-speed analog switch.

Figure 31 shows a method for transmitting dc power down the video coax. This system can be adopted in remote switching locations where a power source is not available or in hazardous industrial environments where mains-derived power supplies are not permitted. Alternatively, this technique could be adopted in a cable TV application, where the channel switcher or selector could be powered from the incoming video lines. The dc power is coupled to the video coax lines using a 1 mH choke, and it is isolated or removed from the video signal using the capacitors (C_1, C_2, and C_3).

Another popular video-signal manipulation application is digitally controlled gain or attenuation circuits. For example, digitally controlled gain may be required for level trimming different video channels to be switched to a single processing path.

Figure 32 shows a DG538A in a dual 4-by-1 arrangement designed to switch four video sources while providing level compensation and/or gain for each using an Si582 wideband op-amp. Note that this circuit has a fixed feedback resistor with R_g switches rather than the more usually adopted reverse. This is due to the fact that the Si582 is a current feedback op-amp. Generally, the devices give a different frequency response for different values of feedback resistor.

Data Acquisition Front-End Applications

A typical data acquisition system comprises front-end sensor stages followed by signal conditioning stages. The analog sensor signal, after being amplified and filtered, is sampled and digitized using a sample-and-hold circuit and an analog-to-digital converter. The digitized signal is then processed, usually under microprocessor control.

Usually, many analog channels must be processed. Due to the high cost of signal-conditioning, fast sample-and-hold, and flash analog-to-digital converter components, it is more feasible to employ a front-end multiplexer so that each channel can be processed in turn.

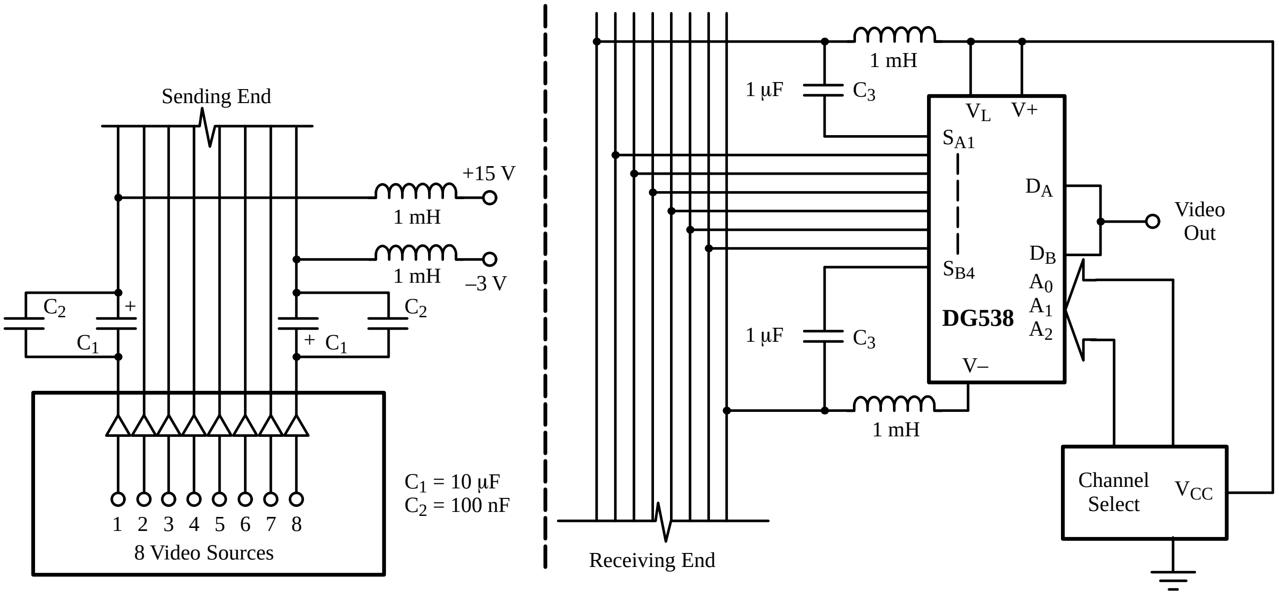


Figure 31. Phantom-Powered Remote Video Switch

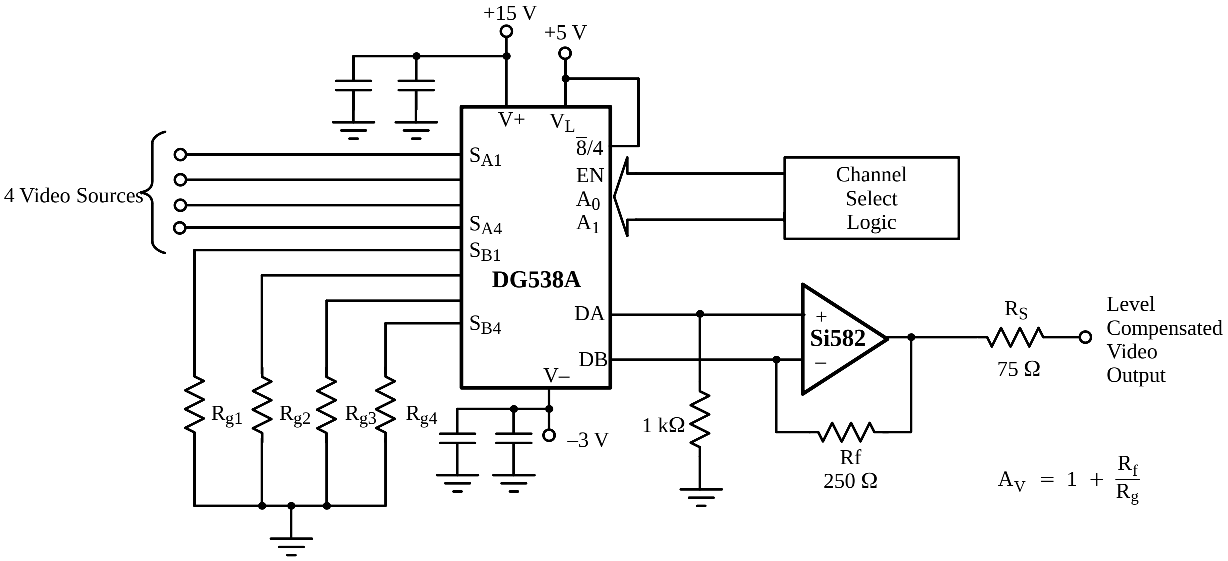

+15 V
+5 V
V+
VL
8/4
EN
A0
A1
SA1
SA4
SB1
SB4
DG538A
DA
DB
V–
4 Video Sources
Channel Select Logic
Si582
+
–
RS
75 Ω
Level Compensated Video Output
Rg1
Rg2
Rg3
Rg4
–3 V
1 kΩ
Rf
250 Ω
AV = 1 + Rf/Rg

Figure 32. Programmable Gain Video Selector

The circuit shown in Figure 33 uses a wideband multiplexer for accurate manipulation of the high-frequency input signals. The "user friendly" control and microprocessor-interface features of the DG538A, combined with its proven high-frequency signal handling, make it ideal for this circuit.

The DG534A and DG538A are also effective devices for switching low-level signals. Commonly, data acquisition systems monitor a number of sensor signals that could be the output of various temperature, pressure, or vibration transducers. Generally, these are low-frequency (often dc), low-level signals. Thermocouples, for example, typically have millivolt outputs with tens of µV/°C resolution. To accurately monitor small temperature changes, the multiplexer must not introduce any dc offset or noise. Since the circuitry must handle small signal levels that are prone to noise/mains pickup, digital crosstalk, etc., apply the same layout rules used for high-frequency designs, such as sufficient grounding and shielding.

The DG538A, with its interchannel ground pin and symmetrical on-chip layout, improves circuit accuracy. A differential signal handling system is an established means of low-level transducer interfacing. This system rejects noise pickup, switching transients, and metallic junction dc offsets as common-mode signals. A highly accurate low-level transducer interface circuit using a DG538A in its differential mode is shown in Figure 34.

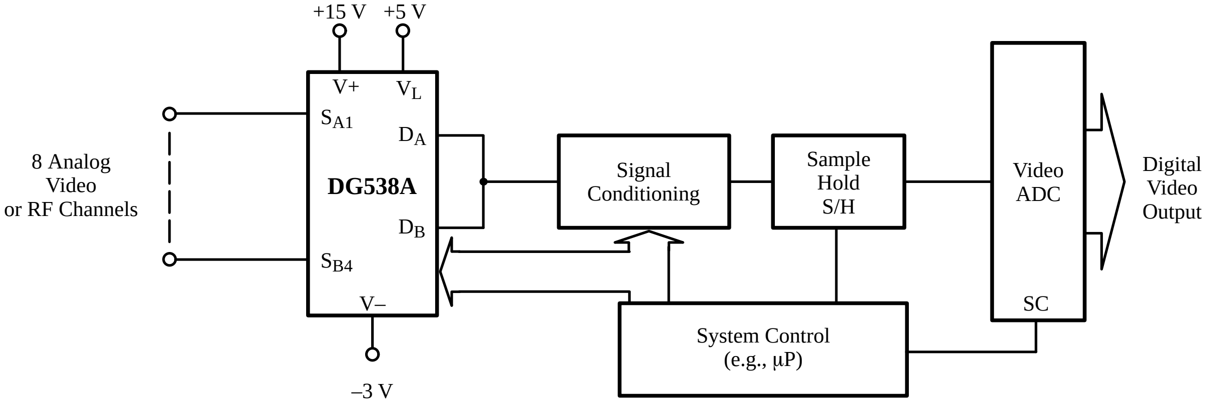

+15 V
+5 V
V+
VL
SA1
DA
DG538A
DB
SB4
V–
–3 V
8 Analog Video or RF Channels
Signal Conditioning
Sample Hold S/H
Video ADC
SC
Digital Video Output
System Control (e.g., µP)

Figure 33. A Basic Multi-Channel Video/rf Processing Circuit

Data Acquisition System Signal Conditioning

Before sampling and digitizing, an analog signal frequently requires “cleaning up” and ranging, a process known as signal conditioning. System front ends will invariably pick up unwanted signals. Signal carrying leads often pass areas that superimpose mains hum, radio-frequency interference, or digital noise on the analog signal to be processed. A well-designed and balanced differential twisted-pair system, such as the one illustrated in Figure 34, will minimize these common-mode signals.

Filtering

Filter circuits are widely used in the signal conditioning stage. Most often, they take the form of low-pass, high-pass, or band-pass configurations that remove unwanted signals outside the required bandwidth. Figure 35 shows a general configuration for an active first-order all-pass circuit that can be used for providing a digitally controlled variable-phase shift, where the phase shift is given by

$$\beta\,(\omega) = 2\tan^{-1}\ \omega RC$$

and the delay is found from

$$t_d = \frac{2RC}{(\omega RC)^2 + 1}$$

Note: $-\omega C = 1/RC$ = cut-off frequency. For constant delay, $\omega < 0.1$ RC.

The circuit shown in Figure 35 may be employed as a phase correction system to equalize phase delays associated with different signal paths. A video crosspoint, for example, will exhibit a varying phase delay due to changing load capacitance on the transmission path when a single input connects to between 1 and n outputs (Figure 25).

Conclusion

This application note has provided information for video, audio, and data acquisition switching system designers. Using the DG534A and DG538A microprocessor-compatible multiplexers from Siliconix simplifies the design task and improves system performance.

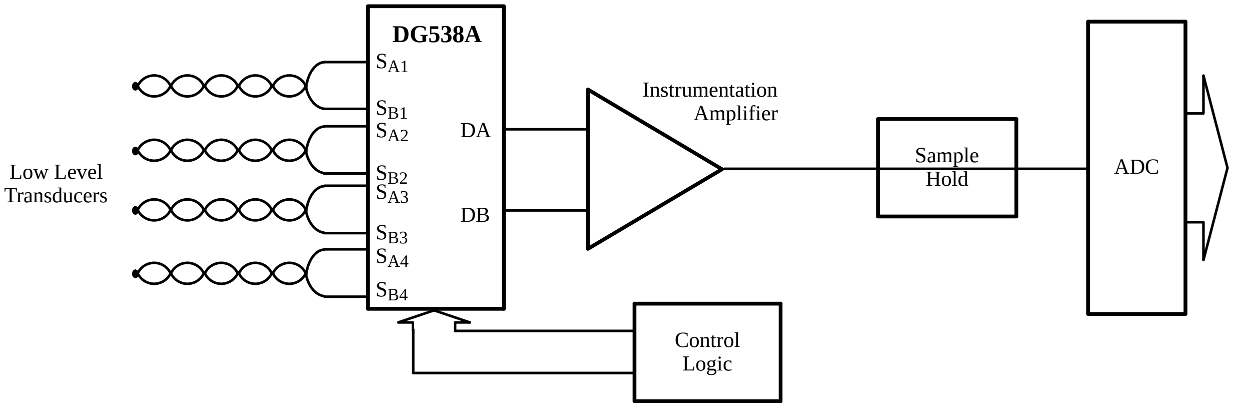
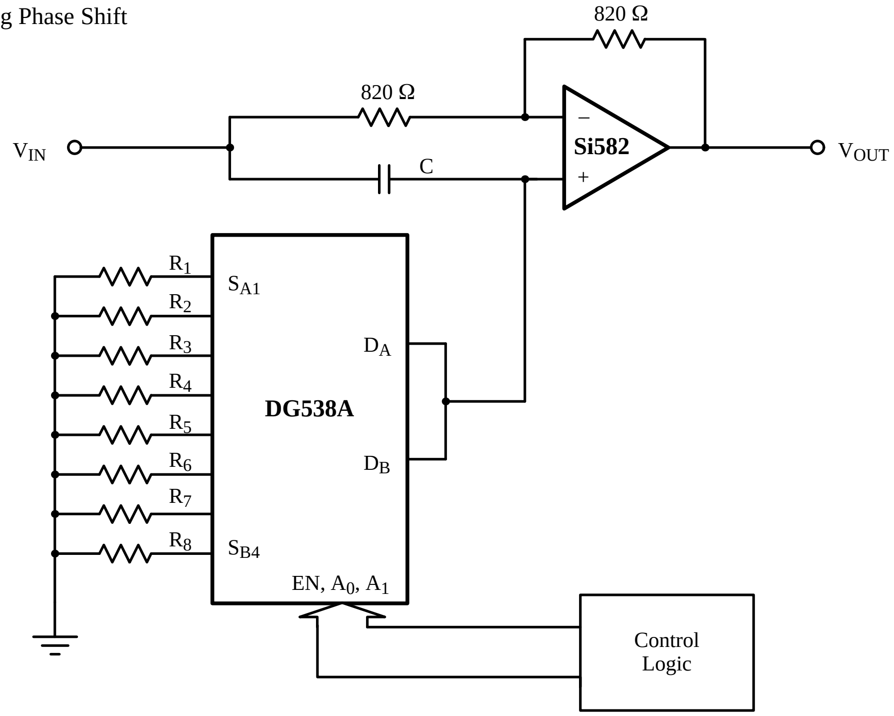


Figure 34. A High-Accuracy Low-Level Signal Processing System

a) Leading Phase Shift


820 Ω
820 Ω
VIN
C
–
Si582
+
VOUT
R1
R2
R3
R4
R5
R6
R7
R8
SA1
DA
DG538A
DB
SB4
EN, A0, A1
Control Logic

b) Lagging Phase Shift

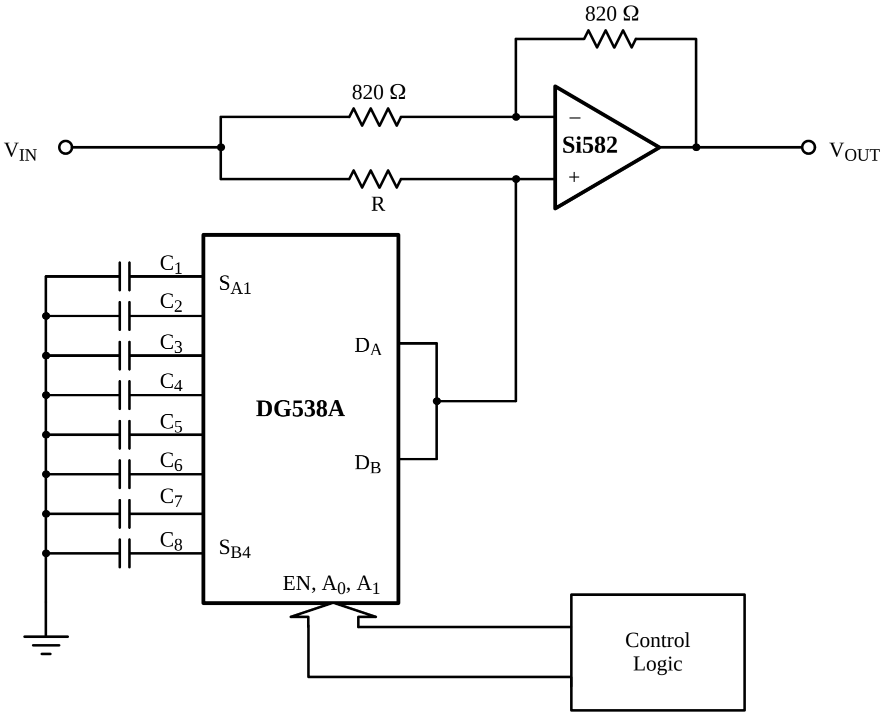

820 Ω
820 Ω
VIN
–
Si582
+
VOUT
R
C1
C2
C3
C4
C5
C6
C7
C8
SA1
DA
DG538A
DB
SB4
EN, A0, A1
Control Logic

Figure 35. A Digitally Controlled Phase Shifter