Complementary Trench Power MOSFETs Define New Levels of Performance

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Introduction

The vertical power MOSFET has become the preeminent switching device in modern power semiconductors, in part due to its capacity for low on-state voltage drops, high avalanche breakdown voltages, square safe operating areas, minimal input drive requirements, and non-latching behavior. Vertical power MOSFETs perform particularly well in switching applications below 100 V or above 100 kHz, where alternative device technologies, such as the IGBT, the bipolar junction transistor, or the thyristor, do not effectively compete. Such operating conditions closely match the needs of the automotive, computer, mobile communication, and portable consumer electronics marketplaces—which comprise some of the highest volume products in the high-tech field. Not surprisingly, the price pressure on high-volume semiconductors components is significant. Improvements in power MOSFET technology must be cost-competitive with existing solutions, by achieving either higher performance at comparable cost or comparable performance at a reduced cost.

The performance of a power MOSFET is primarily measured by an area-normalized specific on-resistance, or $r_{DS}A$ (expressed in units of $m\Omega\text{-}cm^2$). For any given design, this figure of merit describes the inverse relationship between on-resistance and active transistor die area. Below 100 V, the power MOSFETs with the lowest specific on-resistance utilize a *closed cell* geometric design to form a repeated array of paralleled devices, generally square in shape. By increasing the number of cells used in a given device, its total resistance can be decreased.

On-resistance can also be decreased by employing tighter dimensions in its cell structure (thereby increasing the number of cells packed in a given area) or by lowering the breakdown rating of the device. To achieve a favorable tradeoff between breakdown and on-resistance, a double-diffused (DMOS) channel profile is employed to maintain a short channel length without punchthrough breakdown. While sustaining any substantial voltage, most of the potential appears across the epitaxial drain of the DMOS, minimizing depletion spreading into the channel. The breakdown of the device is then set by the epi thickness and doping. Since the epitaxial drain constitutes a series resistive element in the device, higher voltage devices naturally exhibit a higher resistance.[1] Below 100 V, the DMOS on-resistance varies roughly in proportion to $BV^{2.7}$.

Today's commercially available vertical power MOSFETs are of the planar DMOS variety (Figure 1). Currents emanating from the source flow *laterally* along the surface, then turn and flow in a perpendicular direction away from the surface between adjacent body diffusions, through the epitaxial drain, into the substrate, and out the wafer's backside. The channel is formed under the polysilicon gate layer along the planar surface, hence the label "planar." By appropriately scaling the dimensions of this device for higher cell densities and lower operating voltages, significant improvements in its specific on-resistance have been achieved over the last several years (Figure 2).

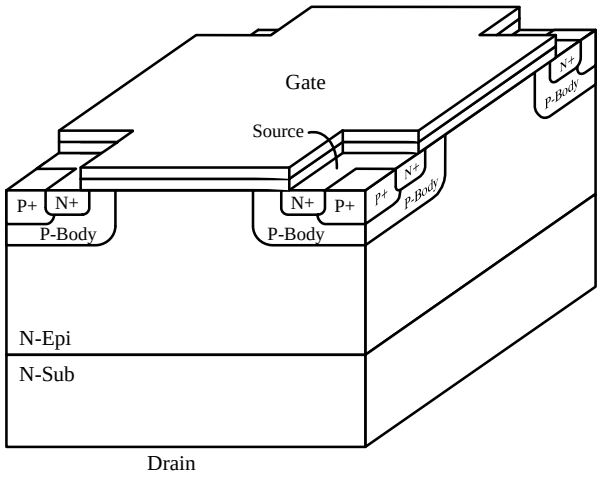

Figure 1. Vertical Planar DMOS Cross Section

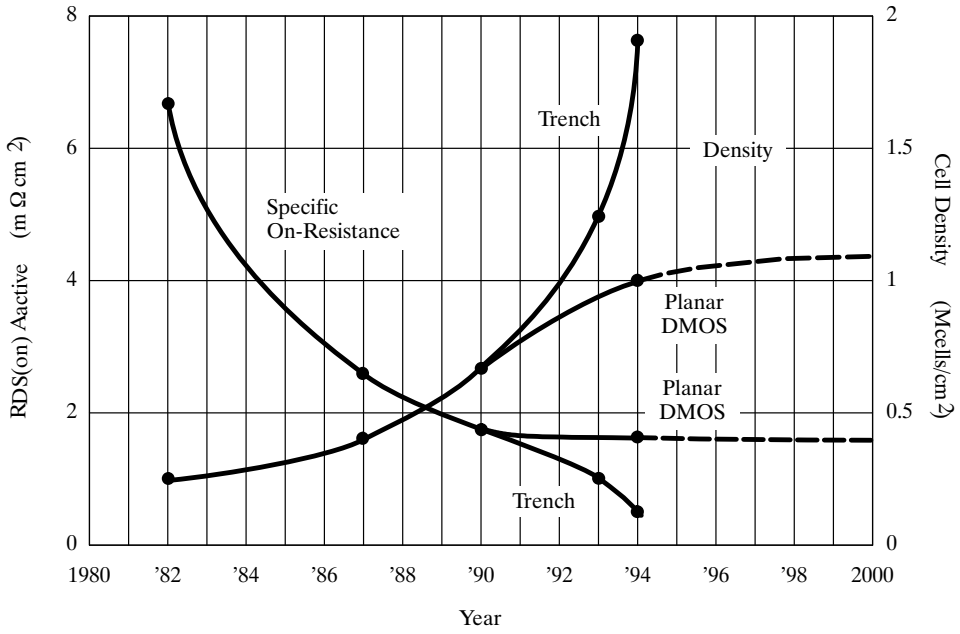

Figure 2. Progress in Vertical Power MOSFETs

At a present-day, state-of-the-art cell density of 6.5 million cells/inch^2, however, further scaling has become increasingly difficult.[2] One of the performance limitations of planar DMOS is the surface area given up to the polysilicon gate electrode. Unfortunately, additional reductions in the size of the gate electrode exacerbate the aforementioned parasitic JFET pinching effect, leading to a higher, not lower, device on-resistance at a small cell pitch (Figure 3).

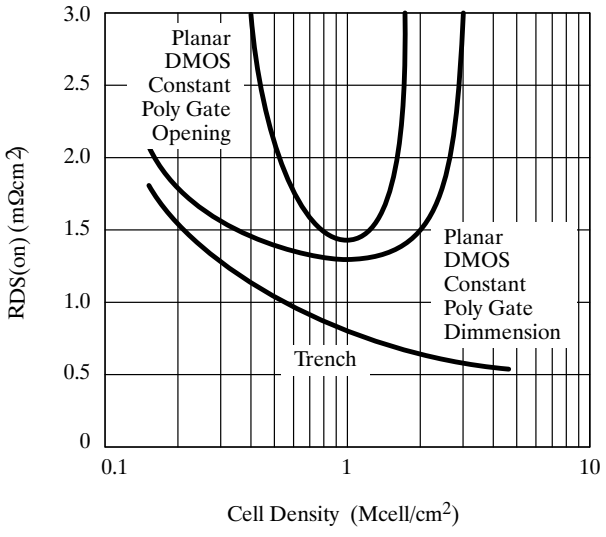

Figure 3. Specific On-resistance vs. Packing Density

The challenge to lower on-resistance and increase cell density is even greater at 60 V, where the epi is more lightly doped and the pinching effect is more pronounced than in a 30-V device. Conversely, if the poly gate dimension is held constant to avoid the pinching effect, and the size of the source/body region (the opening in the poly) is reduced instead, the specific on-resistance still increases at high cell densities, because the transistor gate width per unit area decreases. With such electrical and geometric restrictions, further increases in planar DMOS cell density are not only unwarranted, but likely to be detrimental to performance. Only by eliminating the pinching effect can cell pitch reductions significantly benefit power MOSFET specific on-resistance.

The Trench Gate Power MOSFET

The trench gate or *U-groove* vertical power MOSFET (Figure 4) overcomes the pinching problem associated with planar DMOS. Instead of conducting current along the silicon surface, the channel is formed vertically along the sidewall of a trench etched in the silicon. Using a closed cell pattern similar to that of planar DMOS, the trench forms a grid surrounding islands of silicon. Each silicon island is the location of a double-diffused channel region (or body) and its associated source diffusion. The trench is oxidized, then filled with a conductor and planarized to form the gate of the MOSFET.

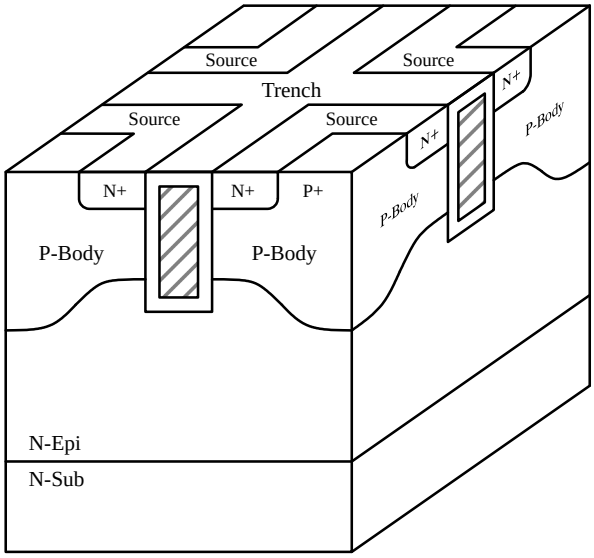

Figure 4. Trench DMOS Power MOSFET Cross Section

While the resulting structure is similar to the MOS capacitors used in megabit DRAMs, the electrical requirements of the trench structure in a vertical power device are more stringent because this structure controls the conduction properties of the device. Moreover, a vertical power MOSFET must be manufactured defect-free, since individual cells cannot be electrically removed from the device in the manner common to large memories with built-in redundancy.

To make trench power MOSFETs manufacturable, Siliconix addressed numerous design, processing, and materials issues. As with any breakthrough technology, such hurdles took many years of development to overcome. Along the way, such issues arose as surfaceshaping, cleaning and drying, elimination and passivation of surface microdefects, gate oxidation-induced stress at sharp corners, control of interface kinetics, doping concentration optimization, etc. Accordingly, device reliability was *designed in* to this device from its inception. All in all, the trench gate MOSFET is capable of improved on-resistance at cell densities never before possible. At 60-V breakdowns, a first-generation design of over 1.25 million cells/cm^2 (8 million cells/inch^2) has been released into manufacturing. Developments at 30 V have topped cell densities of 1.9 million cells/cm^2 (12 million cells/inch^2). By contrast, planar DMOS power MOSFETs exhibit an increase in on-resistance at such cell densities.

N-channel Trench Performance: 60 V and Beyond

The 60-V power MOSFET, the workhorse of the automotive industry, has a breakdown voltage specification primarily motivated by the need to survive a car's load dump condition. While planar DMOS have been used to manufacture these products in the past, the trench power MOSFET can achieve lower resistances in any given package type compared with conventional planar DMOS products. In high-current applications like ABS, power steering, or air conditioning, this device performance advantage translates into fewer components and into the opportunity for enhanced system reliability.

One notable example is the lowest on-resistance 60-V switch available in a TO-220 or D^{2}PAK. Using planar DMOS technology, resistance was limited to 14 mΩ with a 10-V gate drive. The trench gate MOSFET has now redefined this resistance standard to 8 mΩ (as in the SUP75N06-08), a technological breakthrough representing a 43% reduction in resistance and nearly a tripling in cell density. The device characteristics include an absolute maximum gate voltage rating of ±20 V, a continuous drain current of 55 A for a case temperature of 125°C, and a forward trans−conductance of over 30 S. The maximum continuous drain current is rated to 75 A at a case temperature of 175°C, due to package, not device, limitations.

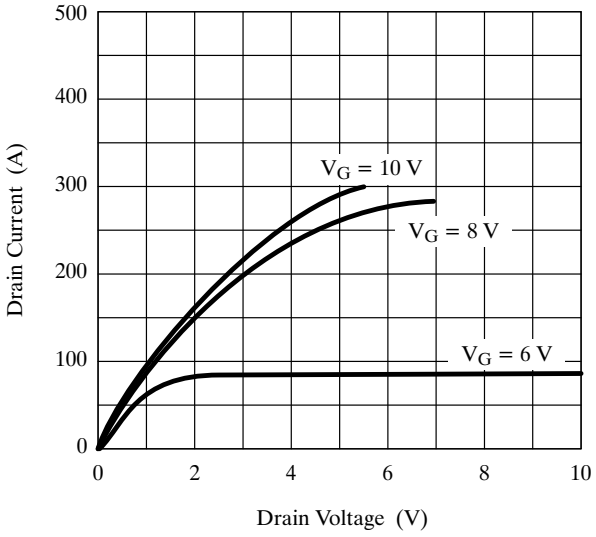

Figure 5. I_D-V_{DS} Family for 8-mΩ 60-V Trench MOSFET

The maximum pulsed avalanche current (1% maximum duty factor) is rated at 60 A but typically exceeds two to three times that amount. Likewise, the intrinsic drain-to-source anti-parallel diode is rated for 75-A operation, so that interruption of current in one leg of an all-n-channel half-bridge driving an inductor can commutate diode recirculation currents equal to the MOSFET's channel current.

One particularly significant characteristic of the device is its ability to conduct high pulsed drain currents. The measured family of I_D-V_{DS} curves shown in Figure 5 for gate biases of 6-, 8-, and 10-V reveals pulsed currents exceeding the 240-A absolute maximum rating of the part. In fact, the V_{GS} = 10 V curve saturates at a current beyond the capability of a Tektronix 371 high power curve tracer.

Since the introduction of the 8-mΩ device, evolution in 60-V planar DMOS has pushed toward the goal of 10 to 12 mΩ. Even at this resistance, theoretical and practical scaling limitations continue to impede further progress. Just to match the on-resistance performance of the first-generation trench devices, the breakdown rating of planar DMOS has to be lowered to 50 V. Of course, a comparable scaling of trench power MOSFETs to the same 50 V rating will result in a lowering of resistance to a value beyond the reach of planar DMOS technology. Further progress in the on-resistance and cell density of a new generation of 60-V trench power MOSFET is also anticipated. Aside from the existing 8-mΩ flagship part, previous power MOSFET resistance mainstays such as 14 and 18 mΩ are also available in 60-V trench power MOSFET technology. All of these parts are rated for a maximum junction temperature of 175°C, a condition consistent with numerous automotive and industrial applications. For customer convenience, the parts are specified on their data sheets at three temperatures, 25°C, 125°C, and 175°C.

While planar DMOS breakdown voltage ratings have been dropped to remain competitive with trench MOSFET on-resistances, trench device technology offering a higher breakdown rating has also been developed. At 75 V (rated), the on-resistance of the present generation trench power MOSFET technology is comparable to the best resistance planar DMOS at 60 V. Instead of capitalizing on the advent of trench technology to lower component resistance, an automotive system designer can opt to increase the voltage margin of a design while holding switch resistance and power losses constant. With a TO-220 on-resistance of 10 mΩ, the 75-V rating allows the N-channel MOSFET to be used in systems employing no local load dump protection. The higher rating is also desirable in uninterrupted power supply (UPS) inverters, where stray inductance can cause voltage spikes to be reflected back onto the primary (battery) side of the transformer (Figure 6). Notice that the high-side (pull up) n-channel devices in the bridge are driven by isolation transformers. Although other floating drive schemes are available, this drive technique is most common when 120- and 270-V AC lines are present, mostly due to safety concerns.

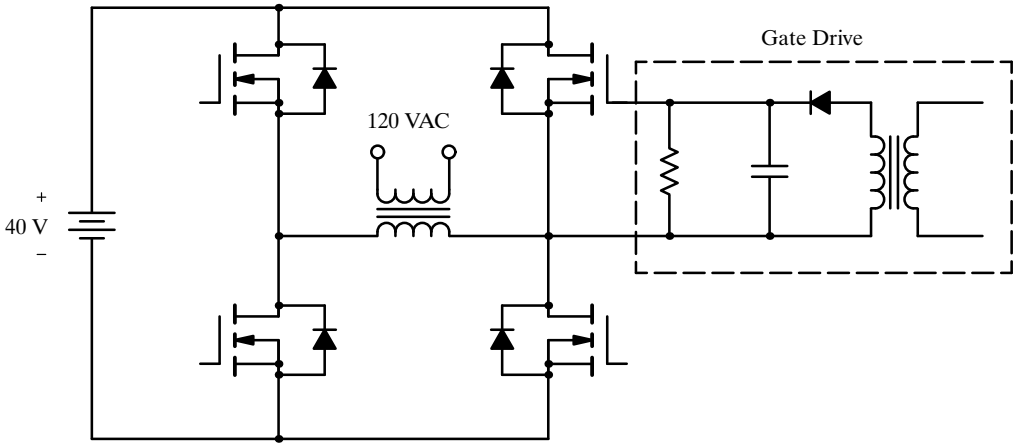

Figure 6. UPS Inverter with Transformer Gate Drive

P-Channel Trench DMOS Technology

High-side devices (connected to the "+" terminal of the battery) are common throughout the automotive environment in lamp and solenoid drivers and in bridge-configured motor drivers.

While n-channel power MOSFETs are well known for their low on-resistance and minimal cost, driving the gate of a high-side n-channel MOSFET is more difficult and costly than driving a p-channel high-side device. The transformer coupled gate drives common in industrial (and consumer) environments are unduly expensive in a car. Unlike an n-channel high-side switch (HSS)—which requires a charge pump, a floating gate buffer and a high-voltage signal level shifter—the p-channel HSS device requires only level shifting to drive its gate. This ease of use is exemplified in the H-bridge brushed permanent magnet motor driver circuit shown in Figure 7. In such a circuit a simple resistor and small-signal 60-V n-channel device accomplish the level shifting function. The p-channel is driven into an on-state synchronous with the low-side diagonal n-channel in the bridge. By driving opposing diagonals, the rotational direction of the motor is reversible. Through pulse width modulation, motor speed is also controllable.

While p-channel power MOSFETs have always been attractive for their ease of use, their on-resistance is higher than that of comparable n-channels. Given the technological advancements of trench power MOSFETs, however, p-channel trench devices under development are rapidly approaching the performance of today's n-channel planar devices (Figure 8). Since charge pump capacitors and control ICs also cost money, the use of a n-channel HSS has a penalty associated with it. Accordingly, the economic value of a p-channel must be considered on a case by case basis.

Figure 9 illustrates the measured family of I_D-V_{DS} curves for a TO-220 sized p-channel trench MOSFET for gate biases of −6, −8 and −10 V. Like its n-channel counterpart, it exhibits a pulsed-mode saturation current in excess of 240 A. More importantly , its room temperature maximum current is limited to 60 A by the package. With a typical resistance of 15.5 mΩ, the device has a resistance around double that of the same size n-channel. Configured in an H-bridge or three-phase bridge together with low-side 8 mΩ n-channel trench MOSFETs, a conducting pair of devices can deliver 20 A to a load while dissipating total of only 9 W. For a 10-V battery, the delivered power is 191 W at an efficiency of 96%. Assuming a 2°C/W thermal impedance to a good heat sink, the 9-W power dissipation of the MOSFET pair constitutes no more than a 18°C rise in junction temperature.

Historically the performance of p-channel MOSFETs has been 2.5 to 3 times worse than that of comparable n-channel devices due to the mobility difference between holes (the majority carrier in a p-channel MOSFET) and electrons (the n-channel majority carrier).

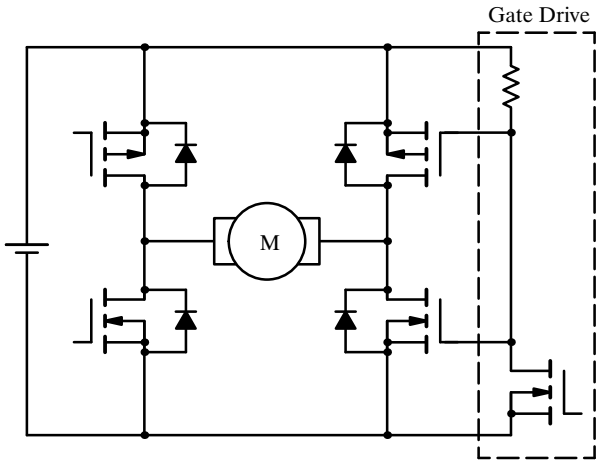

Figure 7. Reversible DC Motor Driver Using Complementary MOSFET

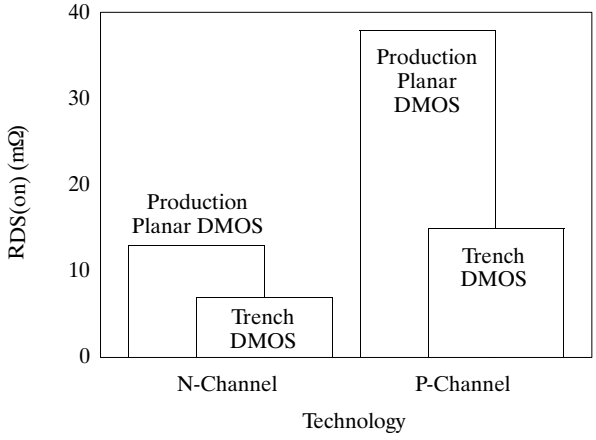

Figure 8. Advances in P-channel Trench Typical On-resistance

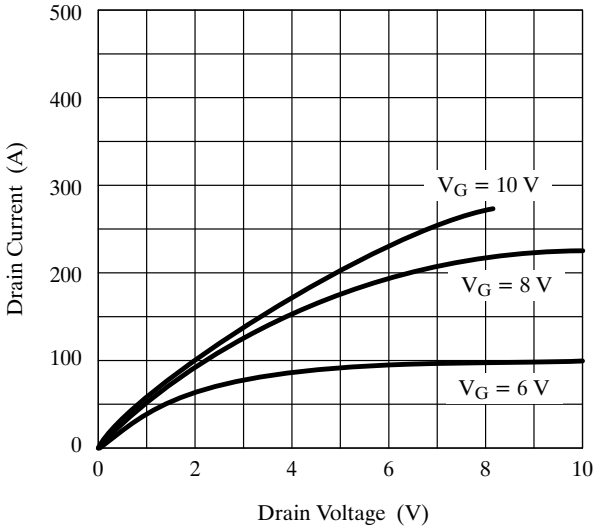

Figure 9. P-channel Trench I_D-V_{DS} Family of Curves

When comparing the resistance of power MOSFETs, this relationship remains a valid assumption as long as the sum of MOSFET channel and epitaxial drain resistance dominates the total resistance of the device. For large-area trench MOSFETs, however, this assumption is not valid. In a situation similar to the condition when planar DMOS are scaled to very low breakdown voltages, exceedingly small channel and drain resistance in a power device make the substrate resistance and package resistance (including bond wires) non-negligible. Interestingly these two components of resistance are not dependent on device polarity. Specifically, the lowest resistivity substrate material is around 3 mΩ-cm^2 for both p-type (boron) and n-type (red-phosphorus or arsenic) doped material. As they constitute an increasing percentage of the total device resistance, the performance of n-channel and p-channel power MOSFETs will asymptotically approach one another.

Surface-Mounted Trench DMOSFETs

While the TO-220 and the D^{2}PAK (TO-263) remain the dominant package types for high-power applications, the role of surface-mount packages has becomes increasingly important in power electronics, particularly in the computer and consumer marketplaces.

Fortunately, trench technology is equally applicable (and important) to surface-mount packages such as the SO-8 (as in the Si4450 LITTLE FOOT). Using 60-V trench device technology, typical SO-8 n-channel die performance of 20 mΩ (with a 24-mΩ spec) has been achieved for a V_{GS} of 10 V (Figure 10). Even at V_{GS} = 6 V, this performance is only degraded to a resistance of 24 mΩ (a 30-mΩ spec). Assuming a maximum junction temperature of only 150°C, this on-resistance translates into a 7.5-A steady state conduction current in a 60-V SO-8 device. The pulsed drain current of this device exceeds 50 A. P-channel on-resistance of approximately twice that of n-channel is likewise expected in an SO-8 package. Figure 11 illustrates the combination of a complementary pair of 60-V trench MOSFETs used to control the firing of a squib in a car's airbag supplemental restraint system (SRS). The less efficient p-channel high-side device is used as a controlled current source while the n-channel is used purely as a switch. The series combination offers redundancy to guarantee an open circuit to prevent false triggering and allow diagnostic checking of the HSS, the LSS and the squib. By paralleling this dual-switch single-squib series circuit, redundancy used to guarantee squib ignition and airbag deployment can also be achieved.

Another aspect of trench power MOSFET technology is its performance improvement at lower breakdown ratings. The second curve in Figure 10 illustrates the measured on-resistance of an SO-8 sized 30-V trench power MOSFET (Si4410). Typical Vgs = 10 V resistances of under 12 mΩ (13.5-mΩ, 10-A spec) can be achieved in a SO-8 package.

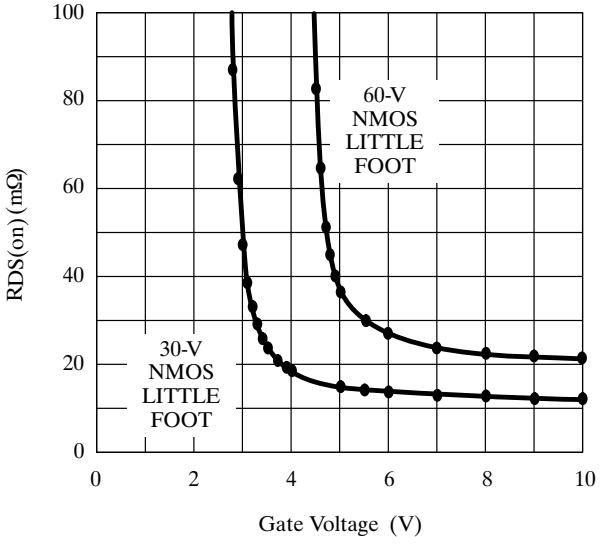

Figure 10. Surface Mount Trench Power MOSFETs

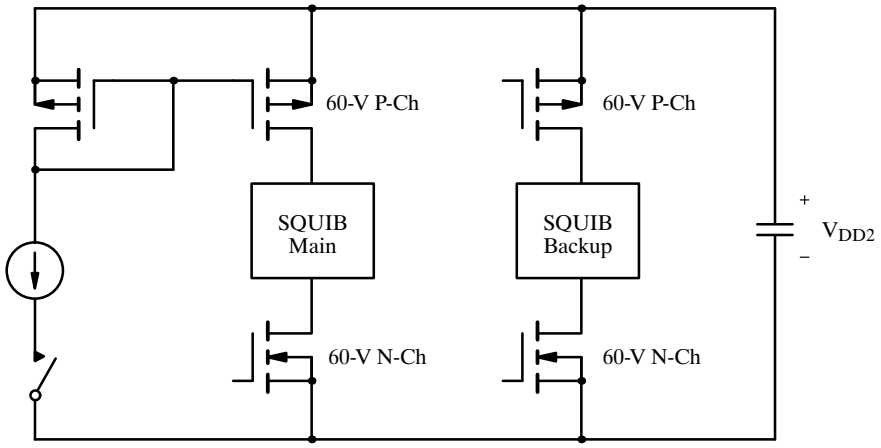

Figure 11. Redundant Complementary Switch Array in Airbag SR

At a 4.5-V gate drive, a resistance of 20 mΩ at 8 A is guaranteed. Like the 60-V SO-8 device, the Si4450, this part has a guaranteed gate bias rating of ±20 V. P-channel 30-V trench power MOSFETs are also under development.

Conclusion. The commercialization of trench power MOSFETs represents a fundamental breakthrough in power MOSFET technology, with beneficial consequences for automotive, computer, and consumer applications. Trench gate MOSFETs developed by Siliconix are capable of improved on-resistance at cell densities never before possible, including 12 million cells per square inch for the 30-V trench process. The difference between trench and typical planar DMOS FETs is dramatic for both n-channel and p-channel devices. Trench products are being introduced in several package styles, including TO-220, TO-263, and small-outline LITTLE FOOT versions, which will be ideal for such applications as controlling the firing of a squib in a car's airbag supplemental restraint system.

Literature Cited

[1] Richard K. Williams and Robert Blattner (1993). "Benefits of DMOS Voltage Scaling on Synchronous Buck Regulator Efficiency," Proceedings of the 5th International Symposium on Power Semiconductor Devices and ICs (ISPSD'93), Monterey, California, pp. 146-51.

[2] Goodenough, F. (1994). "P-DMOSFET and TSSOP Turns On With 2.7 V_{GS}." *Electronic Design*, May 2.