Ordering number:EN2746

N-Channel Junction Silicon FET

2SK1065

High-Frequency General-Purpose Amplifier Applications

Features

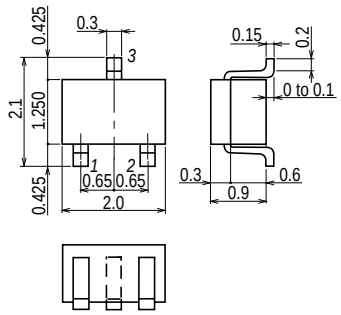
- Ultrasmall-sized package permitting 2SK1065-applied sets to be made smaller and slimmer.
- Small Crss (Crss=0.04pF typ).

Package Dimensions

unit:mm

2057

[2SK1065]



1 : Gate
2 : Drain
3 : Source
SANYO : MCP

Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Gate-to-Drain Voltage	V_{GDO}		–20	V
Gate Current	I_G		10	mA
Drain Current	I_D		20	mA
Allowable Power Dissipation	P_D		150	mW
Junction Temperature	Tj		150	˚C
Storage Temperature	Tstg		–55 to +150	˚C

Electrical Characteristics at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Gate-to-Drain Breakdown Voltage	$V_{(BR)GDO}$	I_G=–10μA	–20			V
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=–0.5V, V_{DS}=0			–10	nA
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=5V, V_{GS}=0	1.2*		12.0*	mA
Cutoff Voltage	$V_{GS(off)}$	V_{DS}=5V, I_D=10μA	–0.4	–1.3	–2.5	V
Forward Transfer Admittance	| yfs |1	V_{DS}=5V, V_{GS}=0, f=1kHz	2.4	6.0		mS
	| yfs |2	V_{DS}=5V, V_{GS}=0, f=100MHz	2.4	6.0		mS

* : The 2SK1065 is classified by I_{DSS} as follows (unit : mA) :

1.2	3	3.0	2.5	4	6.0	5.0	5	12.0

Continued on next page.

(Note) Marking : T
I_{DSS} rank : 3, 4, 5
• For CP package version, use the 2SK242.

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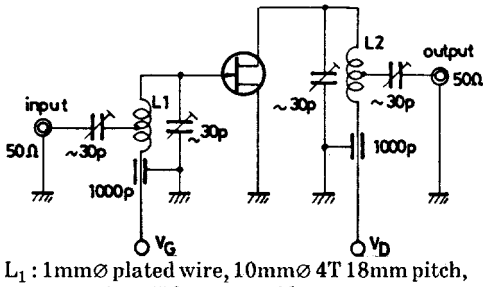
Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			Unit
Input Capacitance	Ciss	V_{DS}=5V, V_{GS}=0, f=1MHz		4.0		pF
Reverse Transfer Capacitance	Crss	V_{DS}=5V, V_{GS}=0, f=1MHz		0.04	0.15	pF
Output Capacitance	Coss	V_{DS}=5V, V_{GS}=0, f=1MHz		4.0		pF
Power Gain	PG	V_{DS}=5V, V_{GS}=0, f=100MHz, See specified Test Circuit		24		dB
Noise Figure	NF	See specified Test Circuit		3.5	6.0	dB

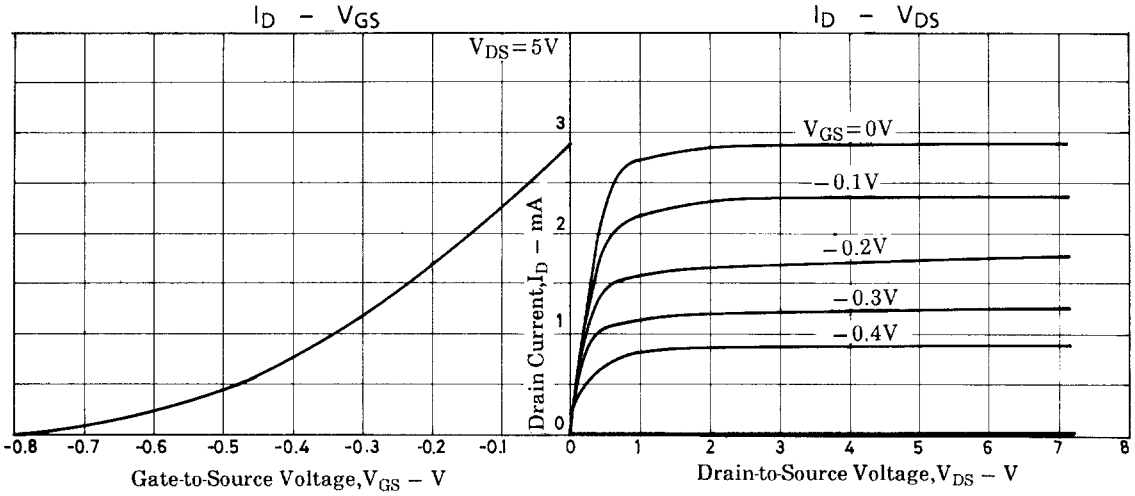
PG, NF Specified Test Circuit

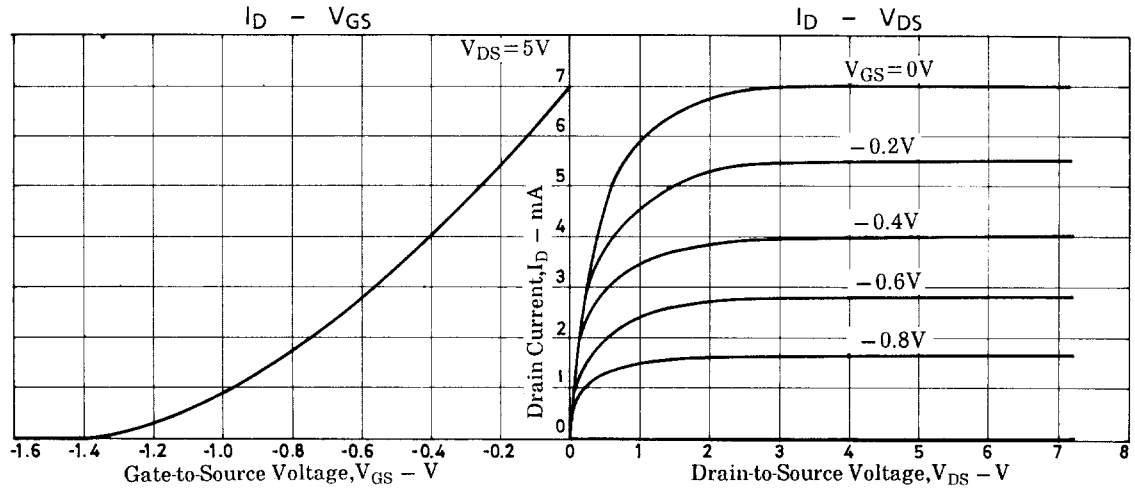
Unit (capacitance : F)



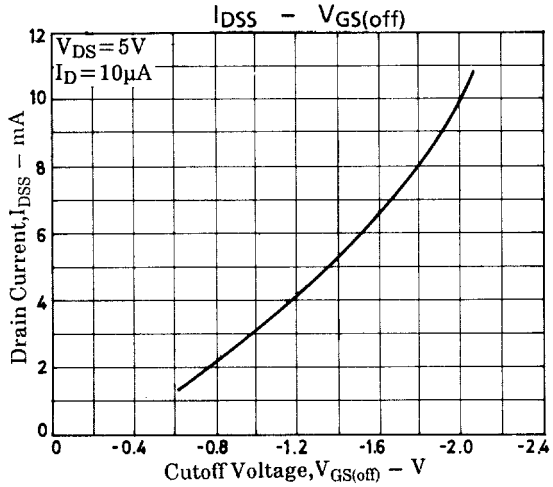
L_1 : 1mmØ plated wire, 10mmØ 4T 18mm pitch, tapped at 1T from gate side

L_2 : 1mmØ plated wire, 10mmØ 6T 10mm pitch, tapped at 1T from drain side

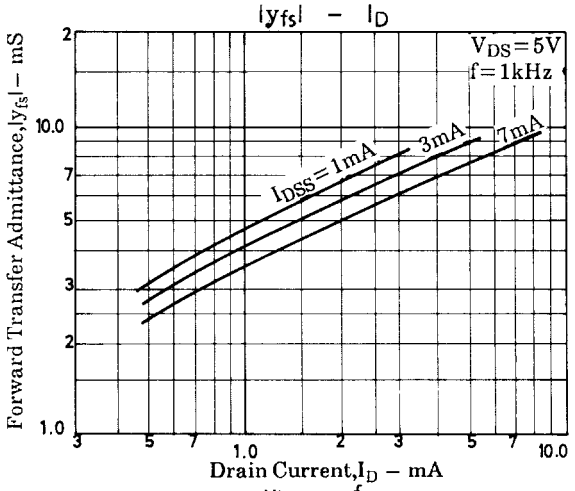




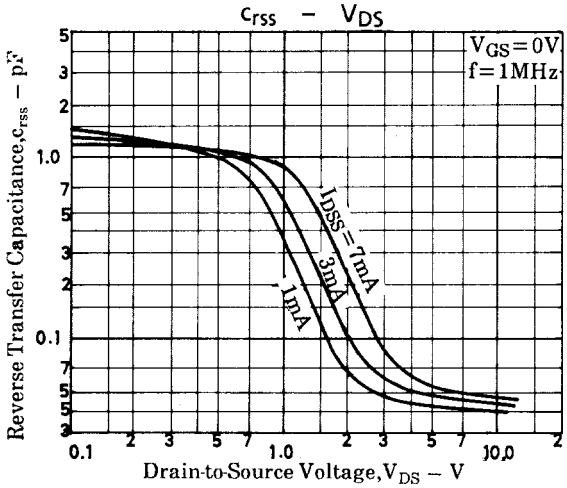
I_{DSS} – $V_{GS(off)}$



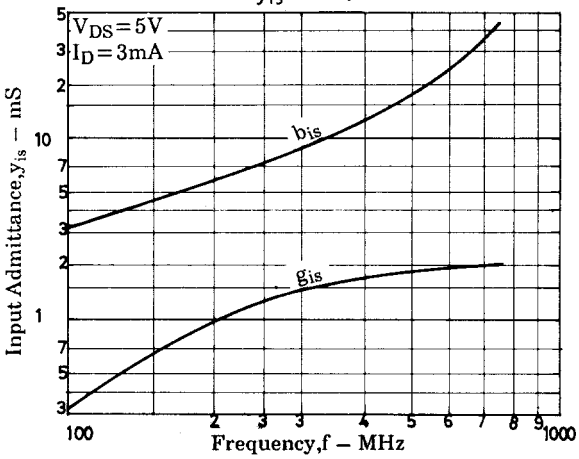
$|y_{fs}|$ – I_D



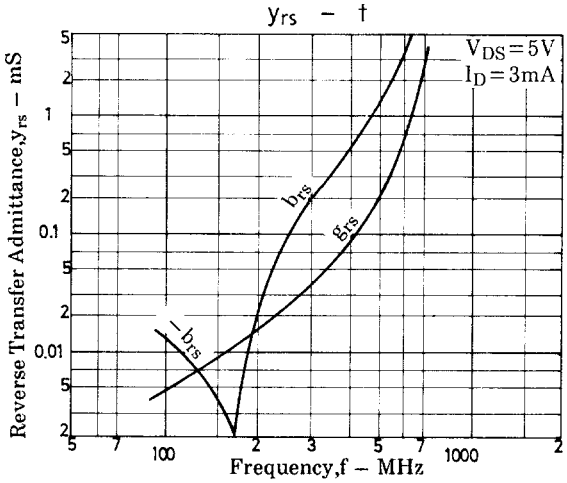
C_{rss} – V_{DS}



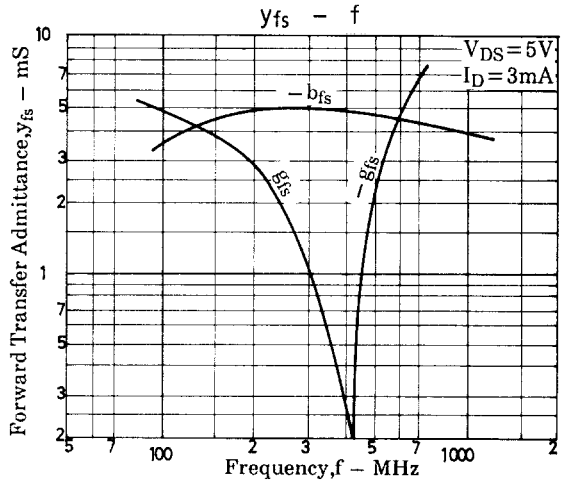
y_{is} – f



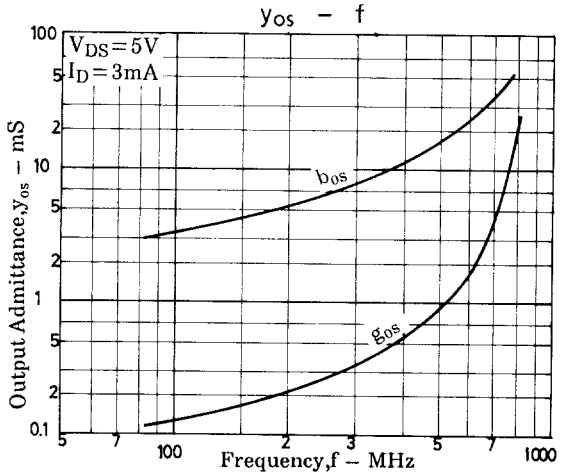
y_{rs} – f



y_{fs} – f



y_{os} – f



y_{is} – I_D