Parallel Operation Of Insulated Gate Transistors

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In the November issue of Powertechnics, the general considerations of paralleling semiconductor switches were presented. Some of the important factors include the characteristics of different types of load reactances and the action of the switching device during its turn-on delay, rise time and turn-off delay times. Different types of switching devices must be handled differently when operated in parallel. Power bipolar transistors, SCRs, MOSFETs and IGTs all have different characteristics which must be taken into consideration. The IGT transistor combines the high input impedance, voltage controlled turn on/turn off capabilities of power MOSFETs and the low on-state conduction losses of bipolar transistors. Like MOSFETs, the output characteristics of IGTs are generated by plotting collector-emitter current, collector-emitter voltage and gate voltage. Unlike the MOSFET, there is an offset voltage generated by the collector-emitter junction of the npn transistor. However, once this offset is overcome, the effective on-resistance in the saturation region is much lower for the IGT than for the MOSFET. A steady state equivalent circuit is shown in Figure 1. Total device current equals MOSFET current (I_{MOS}) plus bipolar current (I_{BIT}) and since the MOSFET current is the base current of the pnp, these current components are related by the gain of the pnp.

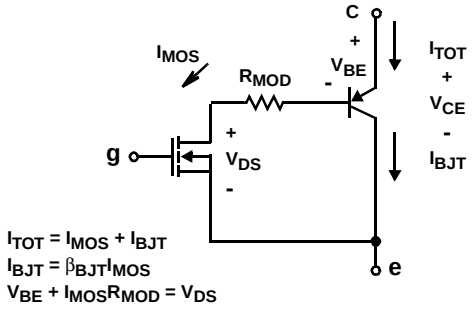


FIGURE 1. N-CHANNEL IGT TRANSISTOR STEADY STATE EQUIVALENT CIRCUIT

To understand the unusual behavior of its temperature coefficient, negative at low current, almost zero at normal current, and positive at high current, we analyzed the IGT by treating the two branch currents comprising the conduction path as two separated devices. The IGT's on-state voltage drop is composed of the MOSFET voltage drop plus the bipolar V_{BE} drop apparently parallel by a pnp-transistor. Note that the only part of the bipolar in parallel to the MOSFET and modulation resistance is the base-collector junction, but the base-emitter junction is common to both branches.

We also know from measurements, the MOSFET's temperature coefficient in the epi-resistance is positive. We know further that as the device temperature increases, the bipolar transistor's gain increases, the V_{BE} drop decreases, which both tend to reduce on-voltage drop. On the other hand, the MOSFET and epi-resistance voltage drop will increase with temperature, tending to increase on-voltage voltage.

These effects cancel and the net result is that the IGT exhibits much less variation of on-voltage voltage with temperature than either bipolars or MOSFETs. The temperature coefficient goes from a bipolar like negative (at low currents) to zero (at rated current) and to a MOSFET-like positive coefficient as current density increases (Figure 2).

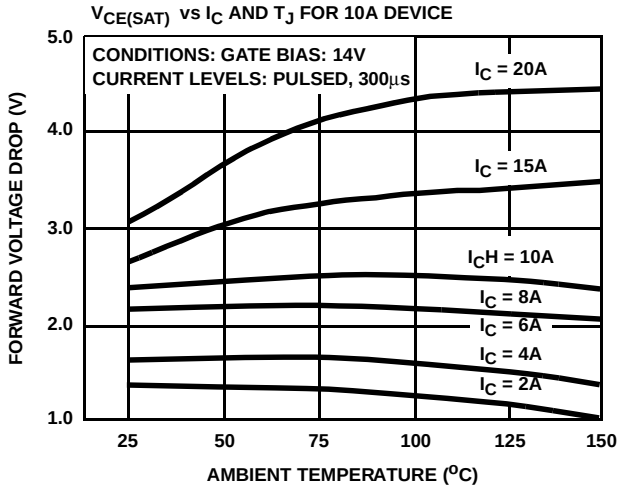


FIGURE 2. V_{CE} vs T_A OF IGT, AT DIFFERENT COLLECTOR CURRENT

Turn-On Switching Performance

Like the MOSFET, the IGT gate presents a capacitive load to the drive circuit. The IGT capacitive elements and their typical variation with voltage is analogous to the MOSFET, hence the IGT turn-on interval can be divided into three distinct regions (refer to Figure 3). In region I, the input capacitance is charged until the gate voltage reaches the value needed to initiate collector current conduction. In region II, turn-on is essentially completed as the collector voltage falls rapidly to the 10% level. The effective capacitance increases dramatically in this region due to the Miller effect. In region III, the collector voltage slowly settles to its saturation level. At the start of Section III, the effective input capacitance remains high because as the collector voltage is driven below the gate voltage, the polarity of the collector gate voltage reverses and C_{GC} increases dramatically. When the collector reaches the saturation voltage level, the gate rises to the gate-emitter supply level (typically 15 volts).

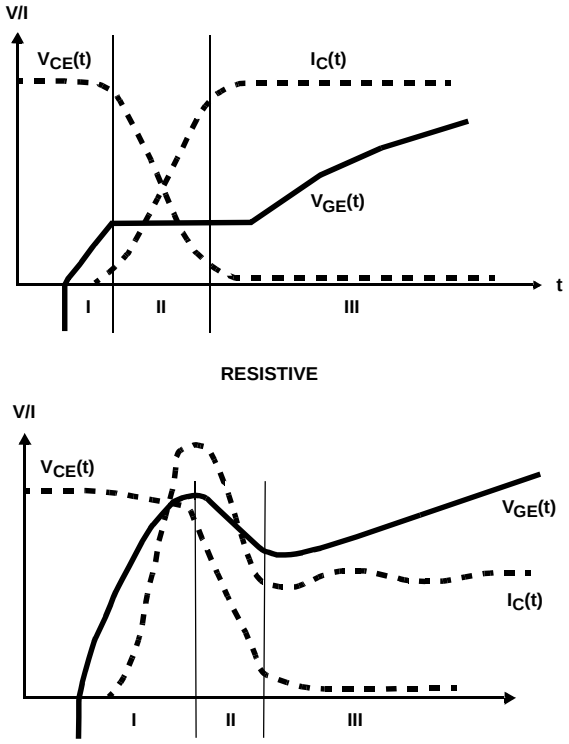


FIGURE 3. IGT TRANSISTOR TURN ON WAVEFORM

Turn-Off Switching Performance

The turn off interval is also composed of three regions as shown in Figure 4 for the case of an inductive load. Region I represents the discharge of the gate to the point where the gate voltage just sustains the collector current.

Region II corresponds to reversing the voltage on C_{GC} whose value is very high at this point. The gate voltage changes very little during this period and the collector-emitter voltage begins to rise slightly. Taken together, regions I and II represent a turn-off delay. Referring back to the equivalent circuit of Figure 1 when the device is fully on, the MOSFET voltage prevents the base-collector junction of the pnp from becoming forward biased. Thus the pnp contributes no significant storage time delay during turn off. In region III, the collector voltage rises rapidly at a rate controlled by the amount of current supplied by the gate drive to reverse charge C_{GC}.

The turn off current fall exhibits two distinct phases: an initial fast drop followed by a slow exponential fall. The initial fast drop is due to the fast cutoff of the MOSFET current. After the MOSFET channel cuts off, the pnp transistor undergoes an open base turn off. The gate drive circuit only controls the initial turn off delay and the slope of the MOSFET current fall by how fast it withdraws gate charge. The pnp exponential turn off tail is a characteristic of the device design.

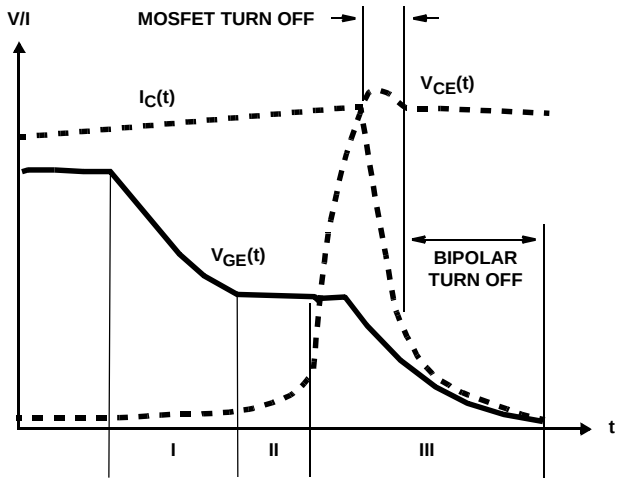


FIGURE 4. IGT TRANSISTOR TURN OFF WAVEFORMS

Device Design To Optimize Turn Off

The bipolar current tail was the cause of the excessive switching times of the first-generation IGT. Turn off of the pnp transistor is a function of the stored base charge and the lifetime of carriers in the base region.

Shortening the pnp turn-off time involves decreasing the bipolar current component and/or reducing the carrier lifetime. The carrier recombination rate can be reduced by localized techniques such as electron or proton irradiation. In addition to a faster decay rate, an irradiated device will have a power pnp gain. By decreasing the bipolar current component, the MOSFET current and the amount of initial drop in the turn-off waveform both increase, resulting in a substantially lower current level for the bipolar decay.

Turn-Off SOA Optimization

The dynamic equivalent circuit of the IGT includes a parasitic pnp thyristor (Figure 5). When the sum of the current gains of the npn and pnp exceeds one, the four layer pnp structure latches on and gate control is lost. The npn is effectively shorted by the emitter metal but there is a finite well resistance, P_{WELL}, below the surface. The npn gain is very low until sufficient current flows through P_{WELL} to exceed its V_{BE} threshold. Thus, $V_{BE(ON)} = (I_{WELL})\ (P_{WELL})$ provides a latching criteria.

The R_{WELL} resistance increases with temperature due to falling carrier mobility in the P_{WELL} region. The I_{WELL} current is the pnp collector current and hence depends upon the pnp gain. I_{WELL} can be increased dramatically by displacement currents from high dv/dt. Increased temperature causes in- creased pnp gain and hence increased I_{WELL}. The $V_{BE(ON)}$ threshold will decrease with increasing temperature.

Clearly, high-temperature, fast turn-off of an inductive load represents a worse case test. Second generation IGT are SOA limited and not latching-current limited. They will fail due to operation outside the power related current at $150^{O}C$

under the fast (R_{GE} = 100Ω), inductive turn off conditions. This performance has been achieved by minimizing P_{WELL} through cell design and the addition of a deep p+ diffusion and by utilizing the buffer layer structure to lower pnp gain.

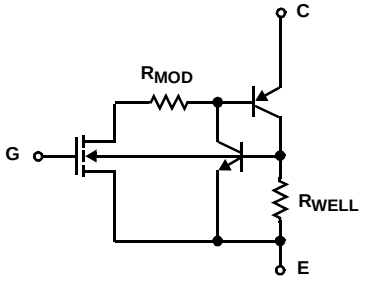


FIGURE 5. DYNAMIC EQUIVALENT CIRCUIT OF THE IGT TRANSISTOR

Results Of Paralleling IGT

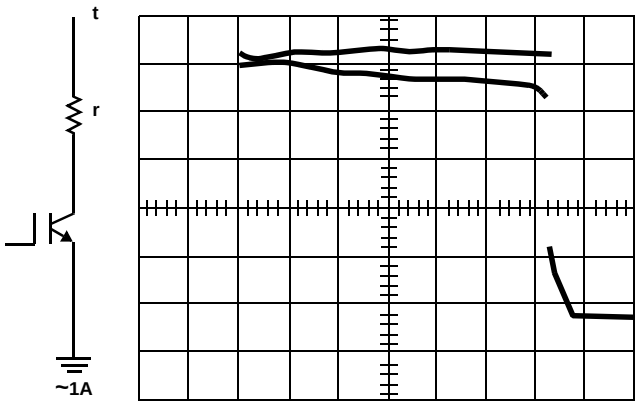
From our experience with paralleling devices like bipolars and MOSFETs, there seemed to be no reason why IGTs should not perform reasonably well.

To perform the measurement, we used the IGT-4E10 and the IGT-4E11 both rated at I_C = 10A at T_C = 100°C and a V_{CE} = 500V. We also used a 20A device the IGT-6E21.

The parameters we considered important for parallel operation, the saturation voltage $V_{CE(SAT)}$ which we measured at different current levels and a gate voltage V_{GE} = 14V. Gate threshold voltage ($V_{G(TH)}$) which we measured at 250µA and 1A (at that level, we can call it an input voltage versus output current) and transconductance (G_{FS}).

TABLE 1.

NO.	$V_{CE(SAT)}$ 10A	$V_{G(TH)}$ 1A	G_{FS}	I	T_{DELAY} ON	T_R	T_{DELAY} OFF	T_F
44	2.35	5.38	4.3	10.5	51	225	250	402
48	2.55	5.50	3.8	9.5	51	236	230	381
Δ%	85%	22%	13%	10%	0%	4.8%	8.6%	5.5%



DEVICE 44/48 (2A/DIV 2µs/DIV)

The circuit we used consisted of HP pulse generators 222 and 214A driving a logic gate (7402N) and the memory driver D50026 connected to the gate through resistors R_1 and R_2 to the gate of the IGT, a Tektronix scope 7854 and current probes 6021 and 6302.

Device 44 and 48 were selected as an average combination and deltas of the different parameters can be seen in Table 1. Parallel operation is good, delta I = 1A at 9.5A and 10.5A in each device. We see clearly the FET and bipolar turn off.

The same devices were used to increase the current to about 40A, checking for latching problems, which did not occur.

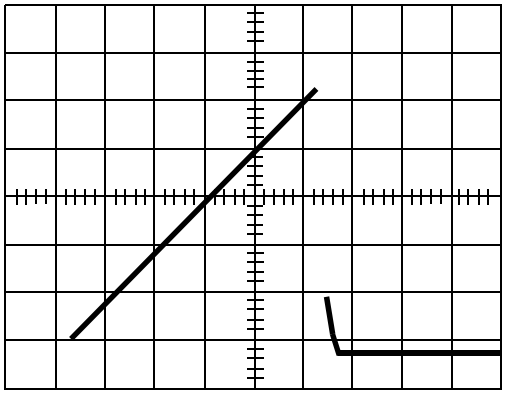
We then changed the gate resistor from 50Ω to 4.7Ω and increased case temperature to the rated 150°C. Still no problems became apparent. Note that the peak current was over four times the rated continuous current.

The same pair was also used to switch on an inductive load (L = 182µH). Excellent parallel operation is achieved with this combination. Even 500ns resolution did not reveal any problems.

The first interesting combination 14 specified T_{FMAX} = 1µs and 15 specified t_{FMAX} = 605µs. The trade-off in switching speed versus $V_{CE(SAT)}$ can be seen in Table 2.

TABLE 2A.

NO.	$V_{CE(SAT)}$ 10A	$V_{G(TH)}$ 1A	G_{FS}	I	T_{DELAY} ON	T_R	T_{DELAY} OFF	T_F
19	2.15	5.55	4.7	10.2	58	244	277	835
20	2.15	4.95	4.3	9.8	46	252	269	871
Δ%	0%	12%	9%	4%			2.9%	4.3%



DEVICE 14/15 60% DIFFERENCE ≈ $V_{CE(SAT)}$ AND LARGE DIFFERENCE IN SWITCHING TIME

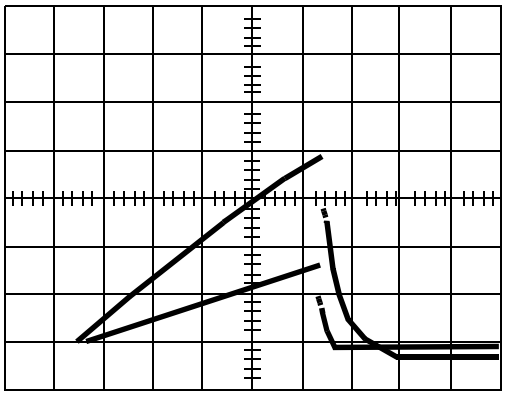
Excellent parallel operation is achieved with this combination, even the 500ns resolution does not reveal any problems.

Device 20 having the lower $V_{CE(SAT)}$ and lower $V_{G(TH)}$ is taking the higher share of current. Both parameters $V_{CE(SAT)}$ and $V_{G(TH)}$ are important in the overall performance. Turn off showing is excellent, but the 500ns time scale shows the result of the difference in the t_{DELAY} off, of

23ns and the difference in device 15 and 16, are the devices having low $V_{CE(SAT)}$ and long turn off times. If paralleled with the proper device (same type), excellent parallel operation is achieved.

TABLE 2B.

NO.	$V_{CE(SAT)}$ 10A	$V_{G(TH)}$ 1A	G_{FS}	I	T_{DELAY} ON	T_R	T_{DELAY} OFF	T_F
14	2.25	5.75	4.3	6.0	53	264	246	750
15	1.40	5.35	5.7	14.8	54	228	436	4317
Δ%	60%	7%	32%	47%	1.8%	16%	102%	575%



CURRENT SHARING OF DEVICE 19/20 (2A/DIV, 5μs/DIV)

Note that 15 paralleled before with the much faster 14 showing extremely poor current sharing.

The 38 and 48 were paralleled to show an inductive load and the recovery current of diode. This is a realistic waveform found in many applications.

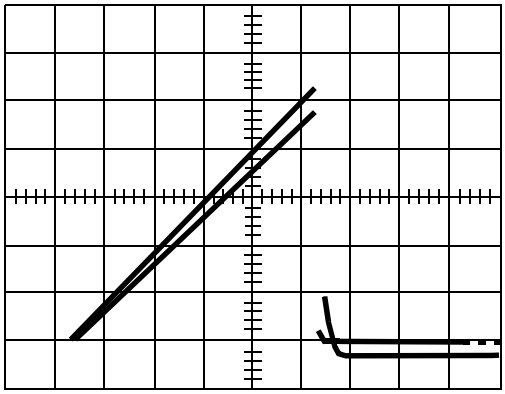
Here we paralleled two 20A IGT transistors. Also excellent current showing which is confirmed at the 500μs/div time scale in.

We paralleled the device 50 and 14 which have a relatively large delta 78% in fall time.

They can be operated in parallel and share much better than we might expect. The large deltas in fall time are the result of the relatively large delta at the current tail in comparison to the rest of the fall time.

TABLE 3.

NO.	$V_{CE(SAT)}$ 10A	$V_{G(TH)}$ 1A	G_{FS}	I	T_{DELAY} ON	T_R	T_{DELAY} OFF	T_F
14	2.25	5.75	4.3	9.2	53	264	246	750
15	2.15	4.95	4.3	10.4	46	252	269	871
Δ%	5%	16%	0%	13%			9.3%	16%



CURRENT SHARING OF DEVICE 14/20 (2A/DIV, 5μs/DIV)

Conclusion

All the conventional wisdom applied in the past to parallel bipolar type devices and MOSFET type devices can be applied to parallel operation of IGT Transistors.

1. $V_{CE(SAT)}$ voltage should be compared at rated current and should not exceed approximately 20% difference.
2. Gate threshold voltage which we measured and compared is important, but could be replaced by V_{GATE} vs I_C at rated current. Maximum differences should not exceed 10-20%.
3. Transconductance g_{FS} differences are not as critical as assumed and may be ignored.
4. $t_{D(ON)}$ and rise time are important for current sharing when switching resistive or inductive loads with reverse recovery currents at turn on, but tolerances are small, seldom posing a problem. Check FBSOA. Note that the fastest device takes most of the current. Emitter inductors can be inserted.
5. $t_{D(OFF)}$ and fall time show also small tolerances, but don't seem to pose a problem. Different device types and different manufacturers should never be paralleled. Note that the slowest device takes most of the current. Removal rate of gate voltage may become a factor. Emitter inductors less than 100μH show excellent results [3].
6. Circuit layout should be mechanically and electrically symmetrical. All lead length and differences in lead length become a factor (12-15nH/inch). Separate the gate circuit from the collector circuit (to avoid magnetic coupling).
7. Always use separate gate resistor to avoid oscillation. We did not see a problem of rated current but we have not made sufficient measurements to insure no problems.
8. Close thermal coupling is recommended (common heatsink) resulting in only small differences in junction temperature.

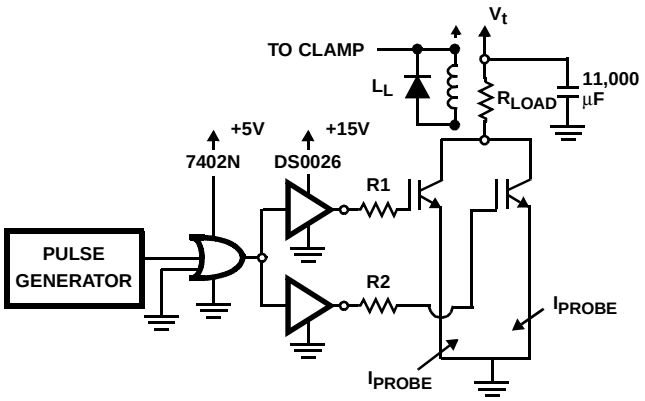


FIGURE 6. TEST CIRCUIT TO EVALUATE PARALLEL OPERATION OF IGT TRANSISTOR

The IGT's key parameters show relatively close distribution making it difficult to establish exact limits for parallel operation but following the above recommendations will give very good results. Additional measurements were made and in no instances did I exceed 2.5A.

IGT Transistors can be paralleled with a relatively small amount of difficulty. Some current derating may be advisable, which tends to improve current sharing. (We can see on the inductive switching waveform up to 6A sharing is almost perfect.)

In the future, switching modules rated at 100A and 200A or higher having blocking voltages of 500V or 1200V are realistic possibilities.

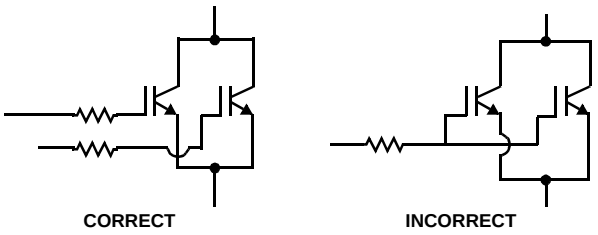


FIGURE 7. PROBLEM GATE CONNECTION

References

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[2] Use Equations to Parallel Transistors. Otto R. Buhler, IBM, Boulder, Colorado, Electronics Design 4, February 15,1977.

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[4] Paralleling Switching Bipolar Power Transistors, J. T. Hutchinson, PCIM, September 1985.

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[8] A Chopper for Motor Speed Control Using Parallel Connected Power HEXFET's, by S. Clemente, B. Pelly, IR.

[9] MOS Power Applications Handbook, Siliconix, Inc., Chapter 5.3, Parallel Operation of Power MOSFET's (TA84-5).

[10] Motor Control Applications of Second Generation IGT Power Transistors, by Donald J. MacIntyre, Jr., Application Note 200.95.

[11] Non-destructive Forward Biased Second Breakdown Testing, No. 78-3, by Sebald Korn, Internal General Electric Report.

TABLE 4. RESULTS OF PARALLELING IGT TRANSISTORS

DEVICE NUMBER	$V_{CE(SAT)}$ AT V_{GE} = 14V			GATE THRESHOLD		TRANS-CONDUC-TANCE G_{FS}	RESISTIVE		INDUCTIVE	
	2A	5A	10A	250μA	1A		T_{DELAY} ON	T_R	T_{DELAY} OFF	T_F
TO-3 LOT 14353										
37	1.42V	1.82V	2.30	3.60V	5.50	4.3	51ns	230ns	23ns	390
38	1.54	2.05	2.70	3.70	5.75	4.2	53	253	230	427
42	1.4	1.78	2.25	3.75	5.60	5.4	45	223	226	421
44	1.42	1.82	2.35	3.50	5.38	4.3	51	225	250	402
47	1.50	1.98	2.60	3.75	5.75	4.2	58	238	226	422
48	1.49	1.94	2.55	3.50	5.50	3.8	51	236	230	381
50	1.45	1.87	2.40	3.62	5.60	4.4	58	232	240	389
Δ MAX			0.45		0.25	1.6				

DEVICE NUMBER	$V_{CE(SAT)}$ AT V_{GE} = 14V			GATE THRESHOLD		TRANS-CONDUC-TANCE G_{FS}	RESISTIVE		INDUCTIVE	
	2A	6A	10A	250μA	1A		T_{DELAY} ON	T_R	T_{DELAY} OFF	T_F
TO-3 LOT 14933.1 — IGT 6E11										
13	1.34	1.79	2.13	3.70	5.90	4.7	55	261	277	808
14	1.37	1.85	2.25	3.94	5.75	4.4	53	264	246	750
19	1.32	1.78	2.15	3.75	5.55	4.7	58	244	277	835
20	1.30	1.78	2.15	3.10	4.95	4.3	46	252	269	871
Δ			0.18		0.8	0.4				
TO-3 LOT (X) — IGT 6E10										
15	0.95	1.20	1.40	4.00	5.35	5.7	54	228	496	4317
16	0.96	1.21	1.42	3.95	5.30	5.7	58	227	515	4190

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