National Semiconductor

Application Note OA-19

Wideband Op Amp Capable of µPower Operation

January 1993

The CLC505 is a current-feedback operational amplifier with an externally-adjustable supply current whose AC performance can be tuned to meet the precise requirements of many high-speed applications. The CLC505 provides a small-signal bandwidth of 150MHz (A_v = +6) while drawing 9mA supply current from ±5V power supplies. Reducing the supply current to 1mA decreases the bandwidth by only a third; 50MHz (A_v = +6). Please refer to the CLC505 data sheet for a full performance description over the 1mA to 9mA supply current range. The following application note is intended to supplement the CLC505 data sheet describing its operation with quiescent supply currents at or below 1mA.

Frequency Response Dependence on Supply Current

Application note OA-13 describes the internal topology of a current-feedback amplifier and the dependence of its loop gain (and hence bandwidth) on the inverting-input impedance. For an ideal current-feedback amplifier, this impedance is zero and the amplifier's frequency response is completely independent of the signal gain. As the supply current of the CLC505 is reduced below the 1mA region, the inverting-input impedance increases to such a degree that its effect on the loop-gain begins to dominate. To understand the impact of this impedance, as well as a similar increase in the output impedance (R_o) at low supply currents, the amplifier's internal block diagram, figure 1, and resulting transfer function are shown. This analysis considers only the non-inverting op amp configuration but a similar result is obtained for the inverting configuration.

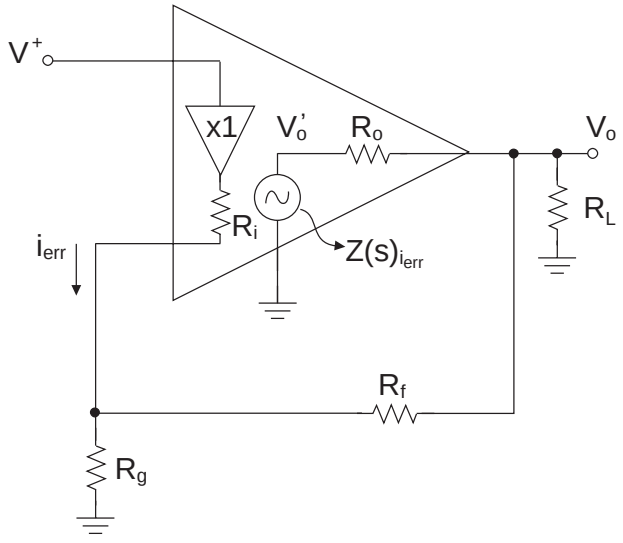

Figure 1: Low current CLC505 analysis topology

An understanding of the transfer function given in Equation 1 is the central point of this discussion. The supply current's dependence enters into this equation through the three internal terms, R_i, R_o, and Z(s). R_i represents the output impedance of the unity-gain buffer found between the amplifier's inputs, while R_o represents the output impedance of the output voltage buffer. Z(s) is the frequency-dependent transimpedance gain which converts the error current (i_{err}), flowing through the inverting input, to a voltage which is buffered to the output.

Both the inverting input and the output pins are voltage-output structures consisting of symmetric (PNP and NPN)

$$\frac{V_o}{V^+} = \left(1+\frac{R_f}{R_g}\right)\left(\frac{1+\dfrac{R_o}{\left(1+\frac{R_f}{R_g}\right)z(s)}}{1+\dfrac{\left(R_f+R_i\left(1+\frac{R_f}{R_g}\right)\right)\left(1+\frac{R_o}{R_L}\right)+R_o\left(1+\frac{R_i}{R_g}\right)}{z(s)}}\right) \quad \textbf{Eq. 1}$$

where:

$1+\frac{R_f}{R_g} \rightarrow$ desired noninverting signal gain

$\frac{R_o}{\left(1+\frac{R_f}{R_g}\right)z(s)} \rightarrow$ will set a limit to the high frequency attenuation as the forward transimpedance gain, Z(s), become very small.

$$\frac{\left(R_f+R_i\left(1+\frac{R_f}{R_g}\right)\right)\left(1+\frac{R_o}{R_L}\right)+R_o\left(1+\frac{R_i}{R_g}\right)}{z(s)} = \frac{1}{\text{Loop Gain}}$$

emitter followers (ref. 1), very similar to a Class AB power buffer (ref. 2, p 293). Emitter-follower outputs show an output impedance that is directly proportional to the operating temperature (K) and inversely proportional to the transistor's quiescent current ($R_e = V_t/I_c$, $V_t = kT/q$, ref. 2, p 398). As the supply current decreases, the portion of the supply current allocated to these stages also decreases causing an increase in both the inverting input impedance, R_i, and the output impedance, R_o. Decreasing the supply current will also increase the DC open-loop gain, Z_{OL}, while decreasing the dominant pole frequency, w_o. However, the product of Z_{OL}*w_o remains relatively constant over supply current and temperature.

From the transfer function shown in Equation 1
Rewriting Equation 1 in these terms
Manipulating this into standard form

Let $1+\frac{R_f}{R_g} = A_v^+$ desired signal gain

$z(s) = \frac{z_{OL}\omega_o}{s+\omega_o}$ single pole, forward transimpedance gain

$$z_t = \left(R_f + R_i\left(1+\frac{R_f}{R_g}\right)\right)\left(1+\frac{R_o}{R_L}\right) + R_o\left(1+\frac{R_i}{R_g}\right) \quad \textbf{Eq. 2}$$

feedback transimpedance; this is the inverting error current, i_{err} resulting from V_o'

$$\text{Loop gain} \equiv \frac{z(s)}{z_t}$$

$$\frac{V_o}{V^+} = A_v^+\left(\frac{1+\frac{R_o}{A_v^+}\left(\frac{s+\omega_o}{z_{OL}\omega_o}\right)}{1+\frac{z_t(s+\omega_o)}{z_{OL}\omega_o}}\right)$$

$$\frac{V_o}{V^+} = \frac{R_o}{z_t}\left(\frac{s+\omega_o\left(\frac{A_v^+ z_{OL}}{R_o}+1\right)}{s+\omega_o\left(\frac{z_{OL}}{z_t}+1\right)}\right) \quad \text{Let} \quad \frac{A_v^+ z_{OL}}{R_o} >> 1, \quad \frac{z_{OL}}{z_t} >> 1$$

then

$$\frac{V_o}{V^+} = \frac{R_o}{z_t}\left(\frac{s+\left(\frac{A_v^+}{R_o}\right)z_{OL}\omega_o}{s+\frac{z_{OL}\omega_o}{z_t}}\right) \quad \textbf{Eq. 3}$$

as $s \to 0$, DC gain, $\frac{V_o}{V^+} = A_v^+$

as $s \to \infty$, high frequency gain, $\frac{V_o}{V^+} = \frac{R_o}{z_t} \equiv A_{min}$

Note that the zero frequency shown in Equation 3 is at a significantly higher frequency than the pole frequency. Once the operating frequency approaches this zero frequency, Equation 3 predicts a minimum gain, A_{min}. This is generally not observed in practice, since the zero frequency of Equation 3 is typically much higher than the frequencies at which R_i and R_o start to show a normal emitter-follower inductive characteristic. To simplify this analysis, the inductive characteristics of R_i and R_o have been neglected. It should be noted that the inductive characteristics will continue to roll off the closed-loop response with attenuations much greater than that predicted by A_{min} at high frequencies. The zero shown in the transfer function of Equation 3 will be neglected with the rest of this discussion focused on the closed-loop pole frequency.

Looking at equation 3 again, the closed-loop response pole will be set by $(Z_{OL}*w_o)/Z_t$. As the supply current is changed, the $Z_{OL}*w_o$ product remains relatively constant. Figure 2 shows the typical open-loop forward transimpedance gain, $(20*\log(|Z(s)|))$, plotted over frequency as the supply current is varied. Figure 3 shows this same forward open-loop gain at 1mA supply current plotted over the full military temperature range. As long as these forward gain responses fall on the same line in the 20dB/decade roll-off region, the $Z_{OL}*w_o$ product remains constant.

With a constant $Z_{OL}*w_o$ term, the only element setting the bandwidth in the transfer function of equation 3 is the Z_t expression, equation 2. In general, it is advantageous to make Z_t as small as possible which will increase the loop gain and as a result improve harmonic distortion and extend the bandwidth. The limit to the reduction of Z_t comes when higher order poles of Z(s) degrade the phase margin at the unity-gain crossover of the loop gain. For a given supply current and desired gain, decreasing R_f and increasing R_L will decrease Z_t. An important limitation on decreasing R_f is the available output current drive. For the non-inverting configuration, R_f+R_g appears as an additional load in parallel with R_L, while for the inverting configuration, only R_f appears as an additional load in parallel with R_L.

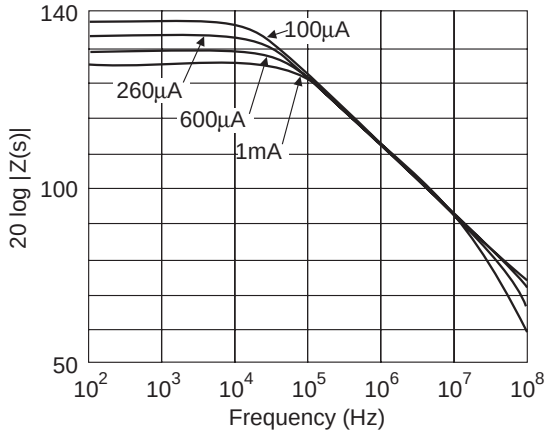

Figure 2: 20log|Z(s)| at different supply currents

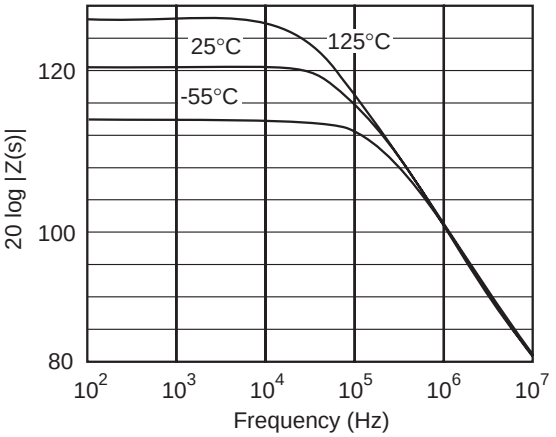

Figure 3: 20log|Z(s)| at 1mA = I_{cc} over temperature

Letting $1+\frac{R_f}{R_g}=A_v^+$, and $R_g=\frac{R_f}{A_v^+-1}$

Z_t can be rewritten as

$$z_t = A_V^+ R_i\left(1+\frac{R_o}{R_L \| R_f}\right)+R_f+R_o\left(1+\frac{R_f}{R_L}-\frac{R_i}{R_f}\right) \quad \textbf{Eq. 4}$$

Equation 4 emphasizes the gain dependence of Z_t. At low supply currents, R_i becomes so large (500Ω at 1mA) as to cause the first term of Equation 4 to dominate. This part of the feedback transimpedance expression is directly related to the desired signal gain, A_v^+. As the gain is increased, Z_t increases, decreasing the bandwidth. This bandwidth dependence on gain is analogous to that observed with voltage-feedback amplifiers. As such, for configurations which set the first term of equation 4 to be the dominant contributor to Z_t, a gain-bandwidth (GBW) product characteristic will be observed. Figure 4 shows a test circuit used to measure the GBW as the supply current is decreased from 1mA to 100µA over gains of +5, +10, and +20. At very low supply currents, slight DC-output currents due to offsets can change the AC performance. For this reason, the output DC-blocking capacitor was used to limit output DC currents.

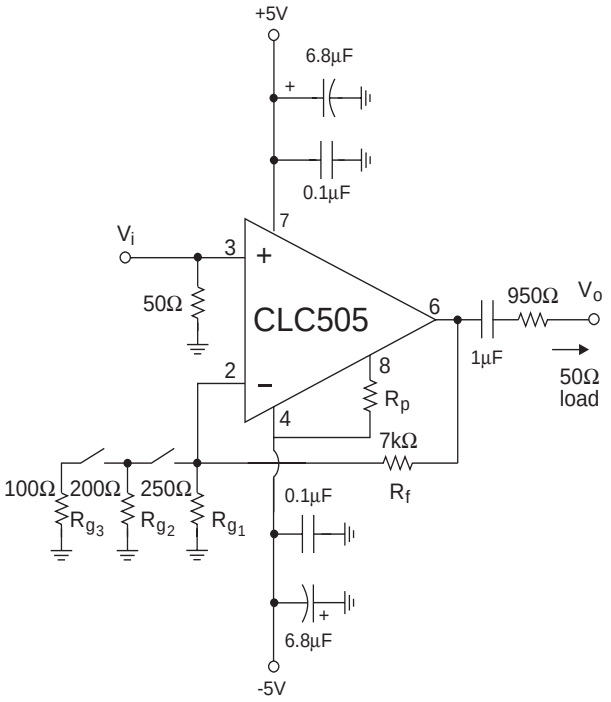

Figure 4: Test circuit for Gain Bandwidth product measurement

For the 1mA case, Equations 2 and 3 were used to predict the small-signal -3dB bandwidth at the three gains of +5,+10, & +20. With R_p = 300kΩ, I_{cc} ≈ 1mA, R_i ≈ 500Ω, R_o ≈ 50Ω and approximate Z_{OL}*w_o product = 2π120E9. Compute Z_t from Equation 2 and expected -3dB bandwidth from Equation 3. The computed and measured results are shown in Table 1. Figure 5 shows the small-signal frequency responses for each of these gains normalized to enter the graph at the same point on the y-axis.

Table 1.

Gain	Computed Z_t	Expected -3dB BW	Measured -3dB BW	Measured GBW
A_v^+=5	3.78kΩ	32MHz	57MHz	285MHz
A_v^+=10	6.50kΩ	18.5MHz	26MHz	260MHz
A_v^+=20	11.9kΩ	10MHz	11.5MHz	230MHz

The test results are in good agreement with the simplified analysis of Figure 5 at the highest gain tested, A_v = +20. At lower gains, several effects combine to extend the bandwidth beyond that predicted by this simplified analysis. Specifically, all of the additional higher frequency poles of the open loop response can come into play at lower gains. These include both the inductive characteristics of the two output impedances and higher order poles for Z(s). This has the effect of decreasing the phase margin from the theoretical 90° assumed by the single pole analysis. Phase margins less than 90° but greater than 60° will extend the closed-loop bandwidth without peaking.

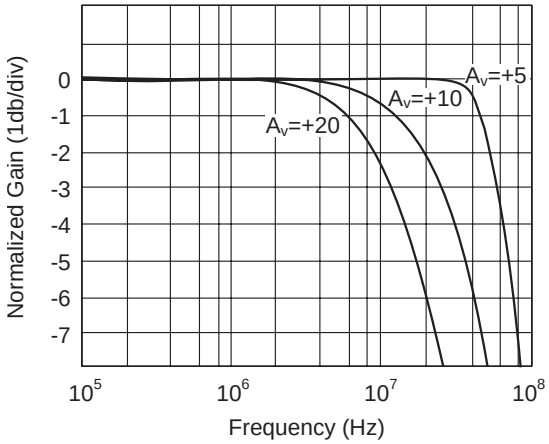

Figure 5: Small signal frequency response vs. gain (I_{cc} = 1mA)

An additional effect serves to increase the measured bandwidth as the desired signal level is increased. As the frequency of operation increases (or as fast rise time signals are applied), an increase in the steady-state inverting-stage current is observed due to the increased I_{err} required when operating at these higher frequencies with reduced loop gain. This increasing error current, as the input is swept over higher frequencies, decreases the inverting input impedance. This frequency and signal level dependence of R_i will decrease the value for Z_t, increasing

the loop gain and extending the bandwidth. This effect is particularly pronounced when the R_i*A_v term becomes a large part of the total Z_t expression, at relatively high non-inverting or inverting gains. Under these conditions, the bandwidth actually increases as the signal level is increased. Figure 6 shows this effect for the A_v = +20 case of Figure 4 with I_{cc} = 1mA.

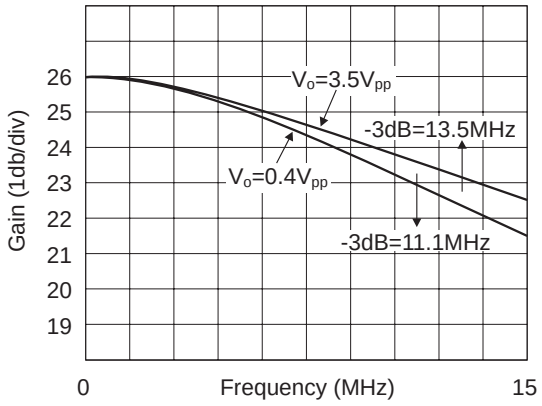

Figure 6: Frequency response vs. signal level

For a given desired supply current, load impedance and signal gain, a close inspection of the feedback transimpedance expression of Equation 4 shows that an optimum R_f can be found that will minimize Z_t, maximizing the bandwidth and loop gain. This is a relatively shallow minimum with the resulting -3dB bandwidth not significantly different than for a fixed 1kΩ = R_f. Nevertheless, solving for this optimum R_f yields the following.

Table 2 on page 6 shows the required information to predict a gain-bandwidth product vs. supply current. At each supply current, the internal parameters (R_i, R_o, and Z_{OL}*w_o) are shown. From this, an optimum R_f can be calculated using Equation 5. The measured small-signal bandwidth and GBW are then recorded. The measured -3dB bandwidths shown in table 2 agree very closely with those predicted from Z_{OL}*w_o/Z_t (evaluating this expression from the data given in this table and Equation 2 for Z_t).

$$\text{Optimum } R_f = \sqrt{\frac{R_i R_o\left(A_v^+ - 1\right)}{1+\frac{R_o}{R_L}}} \qquad \textbf{Eq. 5}$$

This estimate of GBW vs. supply current represents a very conservative estimate. As the signal gain is decreased from A_v = +20V/V, the GBW will increase as shown in Table 1. In addition, the measured bandwidth would increase as signal level is increased, as discussed earlier, up to the point that output-stage drive current and slew limits come into consideration. The supply current and resulting GBW of Table 2 are plotted in Figure 7. This GBW should be taken as a minimum achievable value and a good starting point for estimating the bandwidth capability of the CLC505 at very low supply currents. A PSPICE simulation macromodel available from National can be used to test the performance under different operating conditions. This macromodel reasonably simulates most of the effects discussed earlier. Transient simulation will even show the improved rise times at higher gains as the signal swing is increased.

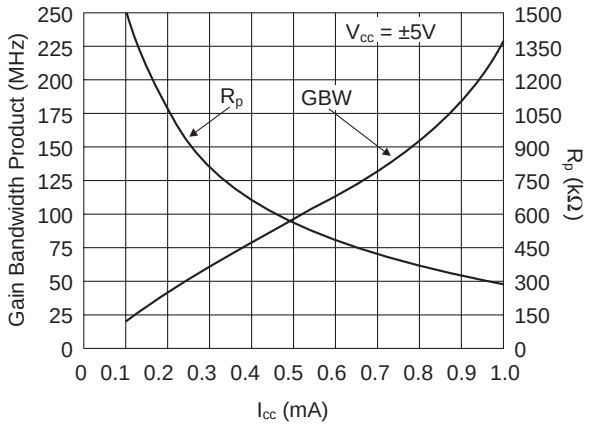

Figure 7: Gain bandwidth product and current set resistor vs. I_{cc}

A common way to illustrate the wideband capability of low-power amplifiers is through a MHz-per-mA figure of merit. Figure 8 shows the same data as Figure 7 with boundary regions for decades of MHz/mA shown. Two low-power Maxim op amps are also shown that claim superior MHz/mA performance. Although certainly capable parts, the Maxim amplifiers are about a decade lower in performance than the CLC505. The CLC505, along with several other National wideband current-feedback amplifiers (such as the CLC406), push strongly above the 100MHz/mA barrier. The discussion thus far has assumed ±5 volt supplies. As will be discussed later, single supply operation is also possible.

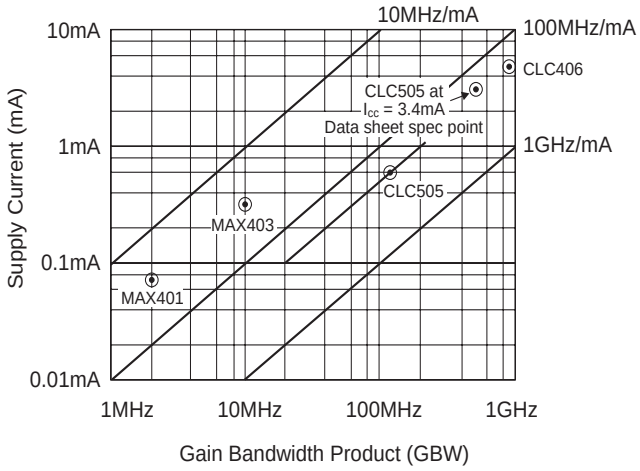

Figure 8: GBW vs. supply current

Table 2: Performance vs. Supply Current (V_{cc} = ±5V, T_A = 25°C, R_L = 1kΩ)

R_p	I_{cc}	R_i	R_o	Z_{OL}	W_o	$Z_{OL}W_o$	A_v=+20 Optimum R_f	A_v=+20 -3dB BW	GBW
300kΩ	1mA	500Ω	47Ω	1.93MΩ	2π62kHz	2π120E9	653Ω	11.4MHz	228MHz
400kΩ	800µA	620Ω	64Ω	2.46MΩ	2π49kHz	2π121E9	842Ω	7.9MHz	158MHz
500kΩ	600µA	920Ω	81Ω	2.92MΩ	2π42kHz	2π123E9	1.14kΩ	6.0MHz	120MHz
600kΩ	480µA	1.16kΩ	100Ω	3.35MΩ	2π38kHz	2π127E9	1.42kΩ	4.6MHz	92MHz
900kΩ	260µA	1.97kΩ	139Ω	4.73MΩ	2π26kHz	2π123E9	2.14kΩ	2.7MHz	54MHz
1MΩ	230µA	2.27kΩ	185Ω	5.13MΩ	2π25kHz	2π128E9	2.60kΩ	2.3MHz	46MHz
1.3MΩ	160µA	3.27kΩ	258Ω	6.80MΩ	2π20kHz	2π136E9	3.57kΩ	1.6MHz	32MHz
1.6MΩ	100µA	4.30kΩ	333Ω	7.50MΩ	2π17.5kHz	2π131E9	4.52kΩ	1.1MHz	22MHz

Secondary Effects of Low Supply Current Operation

Besides having a profound effect on the small signal AC performance, low supply current operation of the CLC505 will also modify most other performance characteristics. The most drastic effect is on the available output current. At 1mA supply current, the CLC505 data sheet guarantees ±5mA at 25°C. This specification should be scaled down proportionately for operation below 1mA. The non-inverting slew rate is retained with very low power levels due to a slew enhancement circuitry in the input buffer stage (e.g. at 1mA supply current, SR = 500V/µs for the particularly demanding condition of A_v = +2). Both of the input bias currents will decrease with supply current but the input offset voltage and temperature drift will become more pronounced. Recall that, for a current-feedback topology, the two input bias current terms are unrelated in both magnitude and polarity. Bias current cancellation to an offset-current specification is therefore ineffective. Please refer to the CLC505 data sheet for more information on these DC error terms at 1mA.

The most subtle effect is perhaps found with the noise performance. As I_{cc} is reduced, all of the amplifier's input referred noise terms show an increase in their 1/f noise corner frequencies. Also, an additional gain term for the inverting noise current becomes appreciable. Specifically, the inverting input impedance acts as an additional impedance gain for the inverting bias current noise. The noise model discussed in application note OA-12 (Noise Analysis for National's Current-Feedback Amplifier's) does not consider this effect and would therefore understate the total output noise. The simulation macromodel will, however, show the correct output noise including this effect.

Taking Advantage of Voltage Feedback Characteristics

Most of the design techniques developed for voltage-feedback amplifiers are applicable to the CLC505 operating at or below 1mA supply current. One of the standard applications for a voltage-feedback amplifier, that is not directly possible with a current-feedback part, is a simple integrator with direct capacitive feedback. Changing the feedback resistor to a capacitor and moving to the inverting integrator configuration will result in the following circuit, Figure 9, and transfer function.

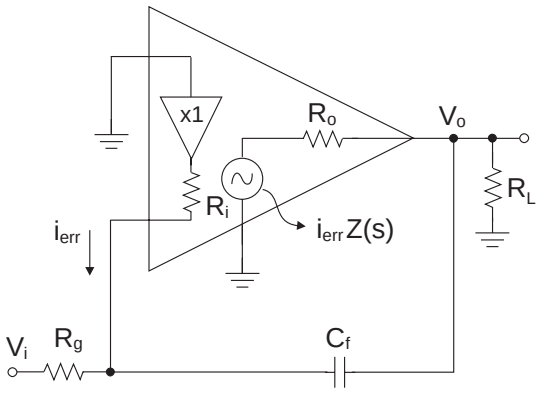

Figure 9: Analysis circuit for inverting integrator

Neglecting the high frequency zero due to R_o. Should set feedback transimpedance zero < higher order poles of Z(s).

Also, high frequency feedback impedance should be > 1kΩ Figure 10 shows a test circuit to demonstrate this integrator operation, while Figure 11 shows the resulting integration of a square wave (100kHz) input to an output triangle wave.

Again the simulation macromodel for the CLC505 is very effective for analyzing the performance of these types of circuits.

$$\frac{V_o}{V_i} = \frac{-1}{sR_gC_f}\left(\frac{1}{1+\frac{1}{z(s)}\left(R_i\left(\frac{R_o}{R_L \| R_g}+1\right)+R_o\right)\left(\frac{s+\frac{1}{C_f\left(R_i \| R_g + R_o \| R_L\right)}}{s}\right)}\right)$$

$$\frac{1}{C_f\left(R_i \| R_g + R_o \| R_L\right)} < 2\pi(10 \rightarrow 20\text{MHz}) \text{ for } I_{cc} \le 1\text{mA}$$

$$R_i\left(\frac{R_o}{R_L \| R_g}+1\right)+R_o > 1\text{k}\Omega$$

Figure 12 shows the simulated gain and phase for the integrator shown in Figure 10. Note that the DC gain of 66dB is comparable to other high-speed voltage-feedback amplifiers (such as the CLC420) while the supply current for this integrator is a very low 500µA.

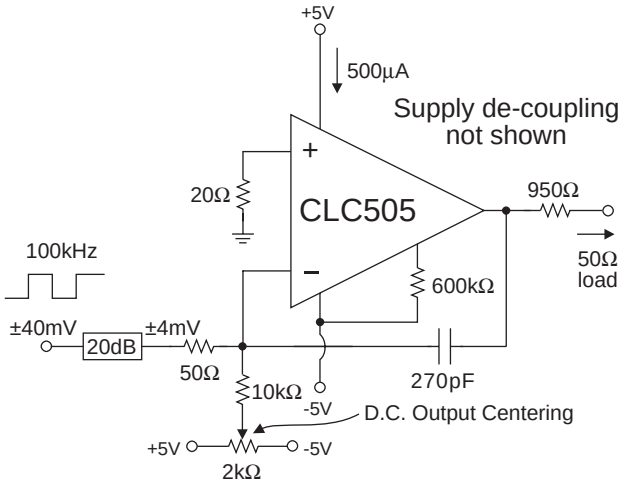

Figure 10: Low power integrator test circuit

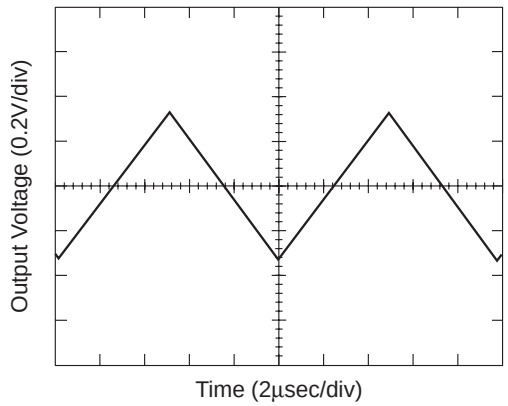

Figure 11: Integrator output to square wave input

µPower Active Filters

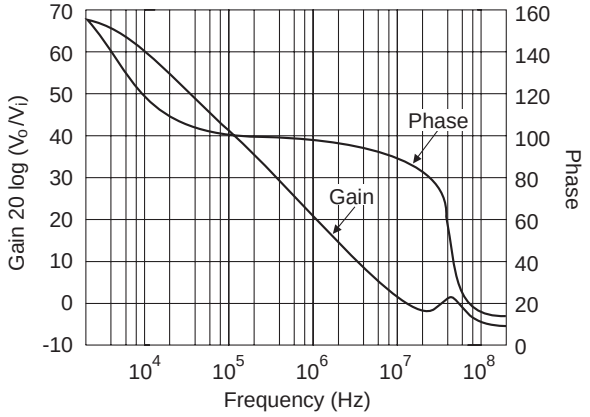

Figure 12: Integrator frequency response

To implement the Sallen-Key type of active filters, it is generally desirable to have an amplifier bandwidth at least twenty times the desired cutoff frequency. It is also desirable to operate the amplifier at relatively low gains. Figure 13 shows a test circuit used to demonstrate the CLC505's capability of implementing very low-power single-supply high-frequency active filters.

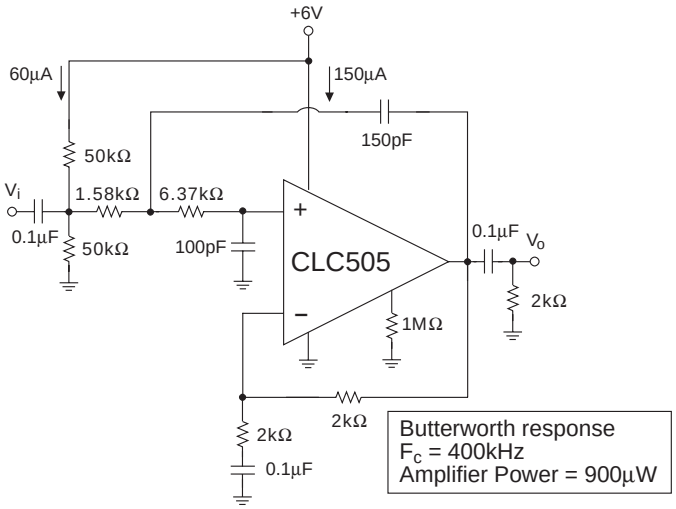

Figure 13: Single supply µpower active filter

For low-power single-supply operation, all of the signal nodes need to be AC coupled. The three 0.1µF capacitors provide this function. This allows the non-inverting input pin to be biased at a midpoint between the supply pins, +3V in this case. The capacitors also prevent any DC currents from flowing in the output pin and reduce the DC amplifier gain to 1, which will hold the output pin DC operating point equal to the non-inverting input (centered between the supply pins.)

At least 6 volts across the part's supply pins is required to give some signal swing capability at the input stage from common-mode input range considerations. The amplifier's AC gain has been set for +2 and the filter components have been adjusted to allow for the amplifier's bandwidth (ref. 3).

Figure 14 shows the frequency response for just the amplifier. At this very low power and gain some peaking due to a loss of phase margin is observed. This will not effect the filter performance however. The 9MHz bandwidth is more than adequate to implement the desired 400kHz Butterworth low-pass filter. Figure 15 shows the measured filter frequency response. The desired cutoff was achieved precisely. The loss in rolloff at higher frequencies arises from a direct signal coupling to the output through the filter components after the amplifier has stopped controlling the output voltage.

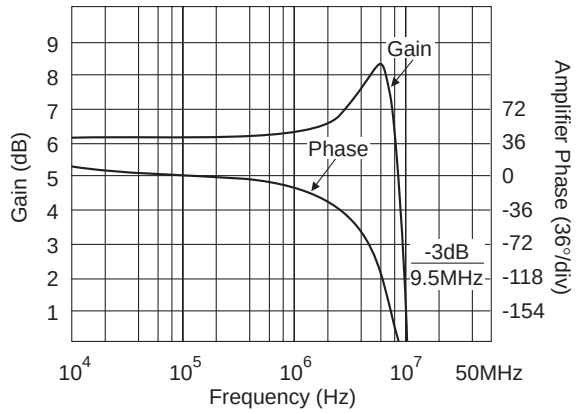

Figure 14: Very low power, single supply, amplifier frequency response

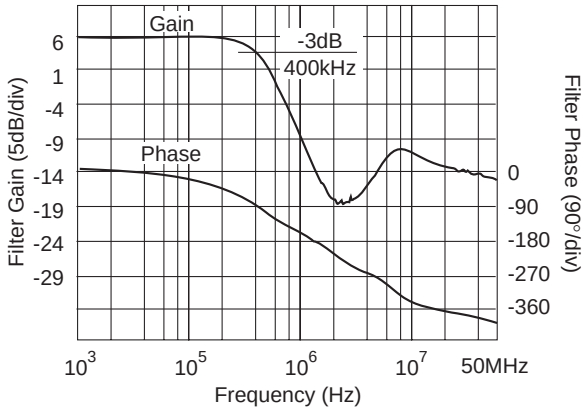

Figure 15: Very low power, single supply, active filter frequency response

Conclusions and Caveats

The CLC505 adjustable supply current op amp offers one of the highest MHz-per-mA performance levels available in a monolithic amplifier. A simplified analysis can do a good job of predicting the gain-bandwidth product under a variety of supply current, gain, feedback resistor, and loading conditions. A PSPICE simulation model available from

National does an even better job of predicting performance over a wide variety of conditions. Although the internal topology of the CLC505 uses a current-feedback approach, at very low supply currents this part may be treated more like a voltage-feedback amplifier having a gain-bandwidth product. Very high-speed integrators and active filters may be implemented at exceptionally low supply currents.

Due to leakage effects, the part-to-part tolerance on supply current for a fixed R_p becomes greater as the desired nominal supply current is decreased. At R_p = 300kΩ, National guarantees a maximum 1.3mA supply current at 25°C from a nominal 1mA value. If a closer tolerance at this, or lower, supply currents is required, please contact National for further information.

References:

Ref. 1 "Current Feedback Amplifiers", National Application Note AN

Ref. 2 “Analysis and Design of Analog Integrated Circuits”, Gray & Meyer, Wiley 1977.

Ref. 3 "Simplified Component Value Pre-Distortion for High Speed Active Filters", National Application Note OA-21

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, a) are intended for surgical implant into the body, or b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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