SEU and Latchup Tolerant Advanced CMOS Technology

National Semiconductor
Application Note 932
R. Koga, K.B. Crawford, S.J. Hansel,
B.M. Johnson, D.D. Lau, S.H. Penzin,
and S.D. Pinkerton, Space Sciences Laboratory
Aerospace Corporation, El Segundo, CA 90245
M.C. Maher
National Semiconductor, S. Portland, ME 04106
March 1994

ABSTRACT

Selected microcircuits constructed in National Semiconductor's FACT™ technology were tested for heavy ion induced Single Event Upset (SEU) and latchup. The devices showed no signs of heavy ion induced latchup for LET values up to 120 MeV/(mg/cm^2). SEU LET thresholds varied within a rather narrow range of 40 MeV/(mg/cm^2) to 60 MeV/(mg/cm^2). The test results suggest that FACT devices will exhibit higher tolerances to the cosmic ray environment than functionally similar microcircuits fabricated in HC/HCT, ALS, or LS technologies.

INTRODUCTION

A new series of microcircuits, belonging to National Semiconductor's FACT (Fairchild Advanced CMOS Technology) family of logic devices has been developed for use in systems that require high speed and low power dissipation. The FACT family consists of devices in two classes, designated by AC and ACT. AC devices have CMOS input switching levels, while ACT devices incorporate a TTL-to-CMOS input buffer stage. Both AC and ACT devices have buffered outputs which are designed to drive CMOS or TTL devices with no additional interface circuitry. Detailed device specifications for this family can be found in commercially available specification sheets.

As shown in Table I, FACT devices are faster and dissipate less power than those fabricated in other technologies such as HC/HCT (High-speed CMOS), ALS (Advanced Low-power Schottky), and LS (Low-power Schottky).

Note: This table is based on data obtained from manufacturer's specification sheets.

FACT microcircuits therefore appear to be good candidates for replacing members of high-power or low-speed logic families in space applications. To determine the suitability of these devices for use in the cosmic ray environment, we have systematically measured the SEU and latchup susceptibilities of selected FACT device types.

TABLE I. Comparison of Several Technologies

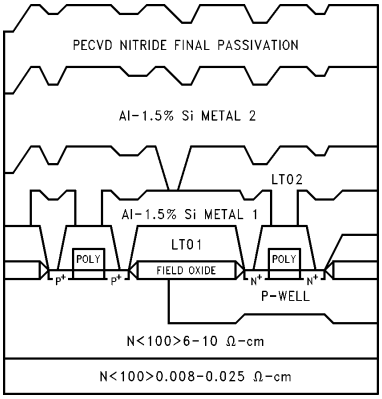
	Power Consumption at 1 MHz Clock Freq.	Propagation Delay (t_{PLH}/t_{PHL})	Internal Gate Delay
FACT	0.1 mW/gate	5.0 ns	1.0 ns
HC/HCT	0.1 mW/gate	8.0 ns	6.5 ns
ALS	1.2 mW/gate	5.0 ns	3.5 ns
LS	2.0 mW/gate	10.0 ns	6.5 ns

The following sections describe the devices tested, the test procedure, and the results obtained for these devices. The test results are compared with those obtained for microcircuits constructed in other technologies, such as HC/HCT, ALS, and LS. Total dose and dose rate susceptibilities are also included to complete the space-radiation assessment of the FACT logic family.

TEST DEVICES

FACT devices utilize a ''2.0 μm CMOS process'' on a thin epitaxial layer, as shown in *Figure 1.* The substrate material is $N^+<100>$, which has a resistivity of 0.008 Ω-cm–0.025 Ω-cm; the 7.5 μm–8.0 μm thick epitaxial layer consists of $N<100>$ material with a resistivity of 6 Ω-cm–10 Ω-cm. Other transistor characteristics of this family of logic devices are listed below:

1. The n-channel MOSFETs are located in p-wells.
2. The effective gate length of this (single polysilicon, self-aligned) process is 1.3 μm for both p-channel and n-channel transistors.
3. No special hardening process is incorporated during the formation of the field oxide, whose thickness is about 5,000Å.
4. After the gate oxidation is performed, low temperature (900°C) processing is employed.
5. The first layer of dielectric material (LTO1), which is deposited in a low temperature environment, has a thickness of 5,000Å; the second dielectric (LTO2) has a thickness of 9,000Å.
6. The dual-layer metalization process uses AlSi metal.
7. The passivation layer is PECVD (Plasma Enhanced Chemical Vapor Deposition) silicon nitride.



TL/F/11663–1

FIGURE 1. FACT Inverter Cross Section

FACT™ is a trademark of National Semiconductor Corporation.

The FACT test devices are enclosed in ceramic, dual-in-line packages with topside rather than backside contacts to the substrate. As shown in *Figure 1,* there are no guard bands around the p-well; a p-channel stop formed under the field oxide isolates the p-well. Design rules governing the n^+ to p-well edge, p^+ to p-well edge, and n^+ to p^+ spacings, have been established by National Semiconductor to help prevent latchup caused by the application of electrically improper signals. However, no special techniques are employed to eliminate possible single event latchup.

A two-transistor equivalent circuit (a combination of the lateral pnp and the vertical npn transistors) is commonly accepted as the latchup circuit for the inverter in *Figure 1* [1]. The collector of the pnp transistor ''sources'' the base current of the npn transistor, while the collector of the npn transistor ''sinks'' the base current of the pnp transistor. This combined transistor configuration is equivalent to a Silicon Controlled Rectifier (SCR). The resistance between the emitter and the base of the pnp transistor is controlled by the substrate material, while the resistance between the emitter and the base of the npn transistor is controlled by the p-well material. The epi-layer decreases the value of the emitter-base resistance of the pnp transistor, making it difficult for the transistor to remain in the ''turned-on'' condition.

A number of FACT devices were selected for SEU and latchup testing, as shown in Table II. We have also tested several earlier versions of Fairchild AC/ACT devices (listed in Table III), which do not have the epitaxial layer. These devices were produced during the initial development phase of the FACT family, and have date codes (DC's) smaller than 8820—all FACT devices with date codes larger than 8820 have the epitaxial layer.

TEST PROCEDURE

SEU and latchup tests were conducted at the Lawrence Berkeley Laboratory 88-inch cyclotron facility using Xe (603 MeV), Kr (380 MeV), Cu (290 MeV), Ar (180 MeV), Ne (90 MeV), and N (67 MeV) ion beams. Ranges for the ion beams spanned from 45 μm for Kr to 130 μm for N. The test devices were oriented at various angles to the incident beams, in order to obtain ''effective LET'' values (the effective LET is found by dividing the actual LET by the cosine of the exposure angle). Care was taken to ensure close agreement among cross-section values obtained from different particle beams having the same effective LET. The beam monitor, and the mechanism for rotating and positioning the test devices were located within a vacuum chamber at the end of the beam pipe.

TABLE II. FACT Test Devices with Epitaxial Structure
(Listed in order of test date)

Device	Function	DC	Measurements	Test Dates
54AC138	1-of-8 Decoder	8840	Latchup	Nov. 1988
54AC245	Octal Bidirectional Transceiver	8840	Latchup	Nov. 1988
54AC374	Octal D Flip-Flop	8840	Latch and SEU	Nov. 1988
54ACT174	Hex D Flip-Flop	8920	Latch and SEU	Aug. 1989
54AC163	4-Bit Binary Counter	8909	Latch and SEU	Dec. 1989
54AC174	Hex D Flip-Flop	8922	Latch and SEU	Dec. 1989
54AC245	Octal Bidirectional Transceiver	8902	Latch	Dec. 1989
54AC299	Octal Shift/Storage Register	8922	Latch and SEU	Dec. 1989
54ACT373	Octal Transparent Latch	8948	Latch and SEU	Dec. 1989
54ACT253	Dual 4-to-1 Multiplexer	8922	Latch	May 1990

TABLE III. Fairchild AC/ACT Test Devices without Epitaxial Structure
(Listed in order of test date)

Device	Function	DC	Measurements	Test Dates
54AC138	1-of-8 Decoder	8627	Latchup	Nov. 1988
54AC245	Octal Bidirectional Transceiver	8747	Latchup	Nov. 1988
54AC374	Octal D Flip-Flop	8638	Latchup and SEU	Nov. 1988
54AC163	4-Bit Binary Counter	8718	Latchup	Feb. 1990
54AC245	Octal Bidirectional Transceiver	8751	Latchup	Feb. 1990
54AC299	Octal Shift/Storage Register	8741	Latchup and SEU	Feb. 1990
54ACT374	Octal D Flip-Flop	8745	Latchup and SEU	Feb. 1990

SEU measurements were obtained using a newly constructed (at Aerospace) tester called the Bus Access Storage and Comparison System (BASACS). BASACS is a logic analyzer, operated via a Macintosh II computer, which can record the correct output signature of a test device while the device is not in the beam line. Later, during exposure to a particle beam, BASACS compares the device outputs with the recorded signature (all devices were biased at 5.0V, and operated at room temperature). This technique is called the ''virtual golden chip'' method, by analogy with the ''golden chip'' method utilized previously [2].

The SEU test procedure is as follows:

1. At the start of the test, the correct signature of the device under test (DUT) is transferred from the Macintosh computer to BASACS.
2. The DUT is held static for 10 ms while the beam shutter opens.
3. The DUT is then run through one complete cycle (several clocks cycles). This is done to ensure that the circuit was initialized properly. If an error occurs in this test cycle, it is flagged as a synchronization error and is not counted as an upset. The DUT is then reset and the test cycle is restarted. (Synchronization errors may occur as a result of setup times not being met, because the reset input is asynchronous to the clock.)
4. After a successful comparison of the first cycle, the DUT is cycled continually while the outputs are monitored by BASACS.
5. When BASACS finds an error (an output does not match the prerecorded pattern), the states of all outputs, position in the cycle, and other necessary information are transmitted to, and stored in the Macintosh computer. The DUT is then reset for 10 ms, and the test starts again after running one test cycle to make sure the device has completely recovered from the upset.

While running the test, the upset rate is kept between 1 and 3 per second. This makes the dead time caused by resetting the test device negligible compared to the total test time. Also, because the device cycles thousands of times between upsets, no part of the device is checked more often than another.

After a sufficient number of errors have been stored, the test is stopped and the total fluence of particles, F, and total number of errors, N, are recorded. The device error probability or cross-section, σ, is then calculated from the expression,

$$\sigma = (N/F) \sec \theta$$

where θ is the incident angle of the beam measured with respect to the chip-surface normal.

Latchup is detected by monitoring the device power supply for an abrupt increase in current. This is done automatically, using a computer controlled programmable power supply (HP6624A).

TEST RESULTS

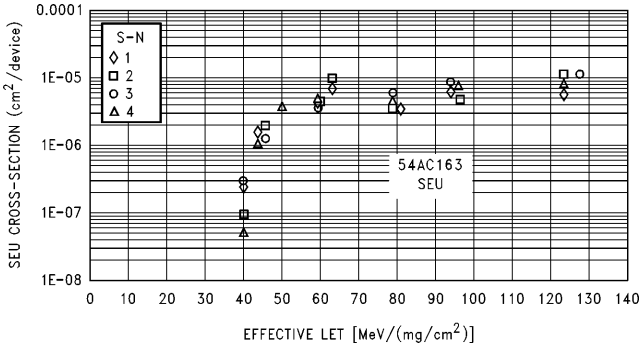
No latchup was detected in any of the FACT device types (listed in Table II) for linear energy transfer (LET) extending from 40 MeV/(mg/cm^2) to 120 MeV/(mg/cm^2). We therefore place the upper limit of latchup cross-section at about 10^{-9} cm^2/device for LET near 120 MeV/(mg/cm^2).

Figure 2 through *Figure 5* show the SEU susceptibilities (cross-section curves) for 54AC163, 54AC174, 54AC299, and 54ACT373 FACT devices, respectively. Test results for 54ACT174 and 54AC374 are provided in the Discussion section, in comparison with other devices. A summary of the susceptibilities of FACT devices to SEU is given in Table IV.

TABLE IV. SEU Susceptibilities of FACT Test Devices

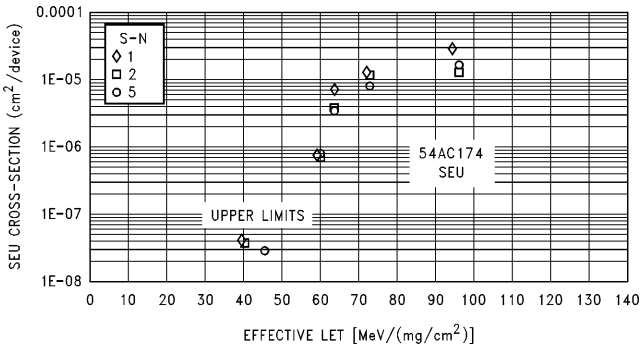
Device Type	DC	LET Threshold MeV/(mg/cm^2)	Saturation X-Section cm^2/device
54AC163	8909	40	$2 * 10^{-5}$
54AC174	8922	55	$3 * 10^{-5}$
54ACT174	8920	60	$9 * 10^{-5}$
54AC299	8922	48	$3 * 10^{-5}$
54ACT373	8948	40	$2 * 10^{-4}$
54AC374	8840	50	$2 * 10^{-6}$

Device types without the epitaxial layer (those listed in Table III) experienced latchup during testing. However, the latchup cross-section curves for these devices are not very similar. An example of a very gradual threshold is shown in *Figure 6* (for 54AC163), whereas an abrupt threshold is shown in *Figure 7* (for 54AC299). The gradual rise in cross-section for the device in *Figure 6* is indicative of latch-up sites of varying sensitivities; the more abrupt threshold ex-



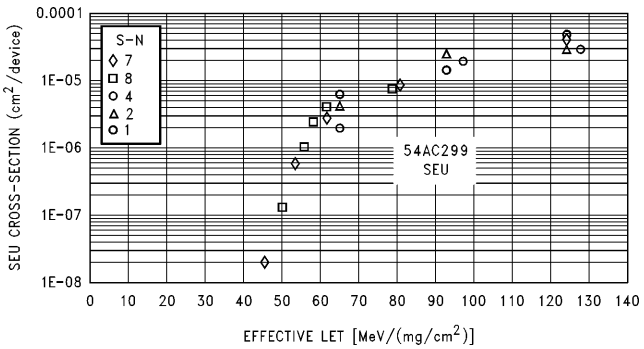
TL/F/11663–2

FIGURE 2. SEU Test Results for 54AC163



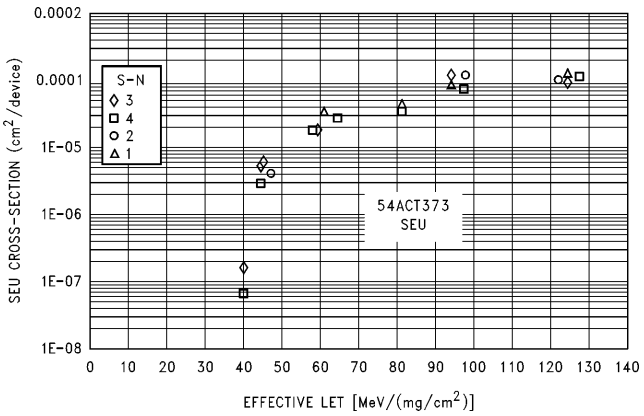
TL/F/11663–3

FIGURE 3. SEU Test Results for 54AC174



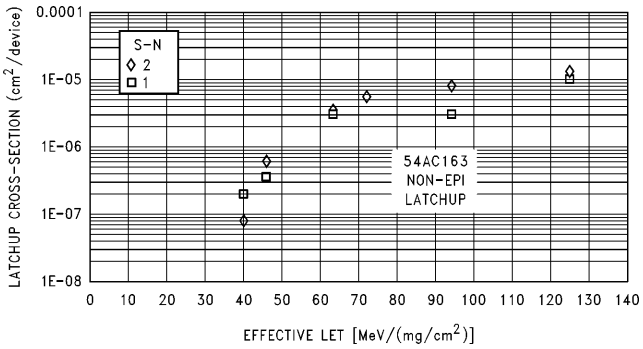
TL/F/11663–4

FIGURE 4. SEU Test Results for 54AC299



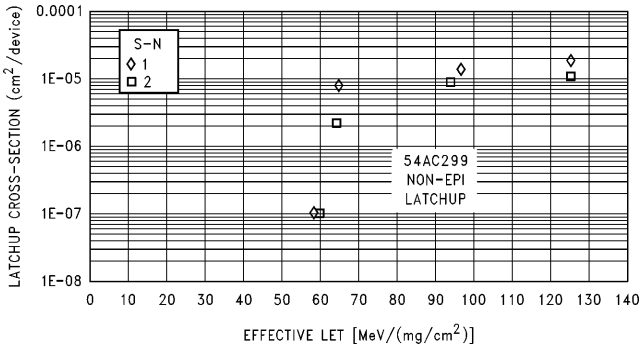
TL/F/11663–5

FIGURE 5. SEU Test Results for 54ACT373



TL/F/11663–6

FIGURE 6. Latchup Test Results for 54AC163 (non-epi)



TL/F/11663–7

FIGURE 7. Latchup Test Results for 54AC299 (non-epi)

hibited in *Figure 7* strongly suggests that the latch-up sites for this device are of a single kind. In both cases the latchup current was about 700 mA at 5V. The sensitivity of these devices to latchup is summarized below in Table V.

TABLE V. Latchup Susceptibilities of AC/ACT Test Devices

Device Type	DC	LET Threshold MeV/(mg/cm^2)	Saturation X-Section cm^2/device
54AC138	8627	~70	$\sim 2 * 10^{-6}$
54AC245	8747	~70	$\sim 2 * 10^{-6}$
54AC374	8638	~70	$\sim 2 * 10^{-6}$
54AC163	8718	40	$1 * 10^{-5}$
54AC245	8751	60	$1 * 10^{-6}$
54AC299	8741	60	$2 * 10^{-5}$
54ACT374	8745	50	$5 * 10^{-6}$

SEU measurements of the devices listed in Table III were not straightforward, since the SEU and latchup LET thresholds were very close to each other. Even though the saturation cross-sections for SEU are higher than those for latchup, the differences are within a factor of 5. Therefore, exact SEU cross-sections for these devices were not calculated.

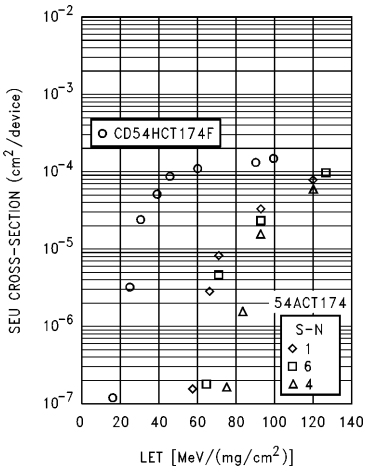
DISCUSSION

A major problem with CMOS is its sensitivity to latchup, as evidenced by the devices listed in Table V. In contrast, no sign of heavy ion induced latchup was detected in any of the new FACT device types tested. These devices (with a date code larger than 8820), incorporate an 8 μm thick epitaxial layer, which aided the suppression of latchup conditions during testing. It should be noted that the inclusion of an epitaxial layer does not, in itself, guarantee latchup immunity in CMOS devices (see, for example, the article by Chapuis and Constant, this issue [6]). However, in conjunction with low resistance p-wells and substrate contacts, and appropriate design rule spacings, the incorporation of an epitaxial layer may be quite effective in suppressing latchup.

The most striking feature of the SEU test results is that the SEU LET threshold values of the FACT devices are quite large and lie within a rather narrow range of 40 MeV/(mg/cm^2) to 60 MeV/(mg/cm^2). In contrast, the SEU LET thresholds of HC/HCT devices vary between 20 MeV/(mg/cm^2) and 60 MeV/(mg/cm^2) [3]. Since the FACT process uses a thin epitaxial layer with a heavily-doped substrate, it has a low susceptibility to SEU. That is, the combined result of a suitable choice of material (heavily-doped substrate) and proper design (thin epitaxial structure) greatly reduces the funnel effect by decreasing the charge-collection region. This effectively diverts the excess charge away from the sensitive node.

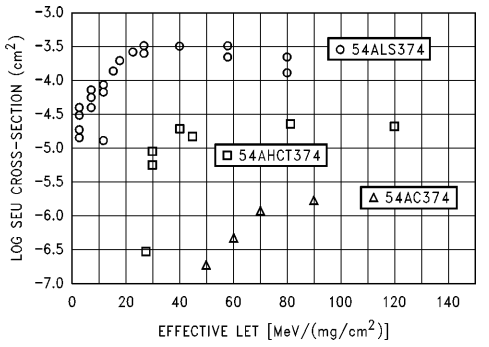
Previous results indicate that HC/HCT devices have much higher SEU LET thresholds than either ALS or LS devices [3]. It appears that FACT devices have even higher threshold values than those of HC/HCT devices, and by implication, than those of either ALS or LS devices.

Figure 8 compares SEU test results for FACT 54ACT174 with those of RCA's functionally equivalent CD54HCT174. The cross-section curve for CD54HCT174 was obtained as an average of several samples tested previously by the authors. Similarly, *Figure 9* compares test results for FACT 54AC374 with those of 54AHCT374 and 54ALS374 (54AHCT374 is an advanced CMOS, TTL-compatible device). Since the SEU test data for 54AHCT374 and 54ALS374 had already been plotted in [3], the test results for 54AC374 were simply overlayed on this plot.



TL/F/11663–8

FIGURE 8. SEU Test Results for 54ACT174 and CD54HCT174



TL/F/11663–9

FIGURE 9. SEU Test Results for 54AC374, 54AHCT374 and 54ALS374

The size of the sensitive region can be inferred from the measured saturation cross-section. The inferred sensitive region of one memory location in a FACT device ranges from 400 μm^2 to 2500 μm^2, which is consistent with the geometrical area.

Total dose and dose rate (transient) tests have been conducted by National Semiconductor Corporation. Since the test results have been published previously [4, 5], only the salient points are summarized here. The total dose resistance at high dose rates is as follows: The parametric failure (mainly an increase in the standby current) level is greater than 100 krad(Si) at 3 Vdc, while the functional failure level is greater than 300 krad(Si) at 3 Vdc. The dose rate test results indicate that the products are latchup immune and that the minimum soft error upset level is about 10^9 rad(Si)/sec, at temperatures up to 117°C (for details, see [5]).

CONCLUSION

SEU and latchup test results were obtained for selected device types from National Semiconductor's FACT family of microcircuits. The tested devices showed no signs of heavy ion induced latchup for LET values up to 120 MeV/(mg/cm^2). SEU LET thresholds varied within a rather narrow range of 40 MeV/(mg/cm^2) to 60 MeV/(mg/cm^2).

Comparing the test results for FACT devices with those in [3], we can tentatively conclude that the FACT devices will have higher tolerances in the cosmic ray environment than functionally similar microcircuits fabricated in HC/HCT, ALS, or LS technologies. However, it should be noted that the tests reported here were conducted at room temperature, and as such, may not accurately reflect the behavior of the tested devices at elevated temperatures.

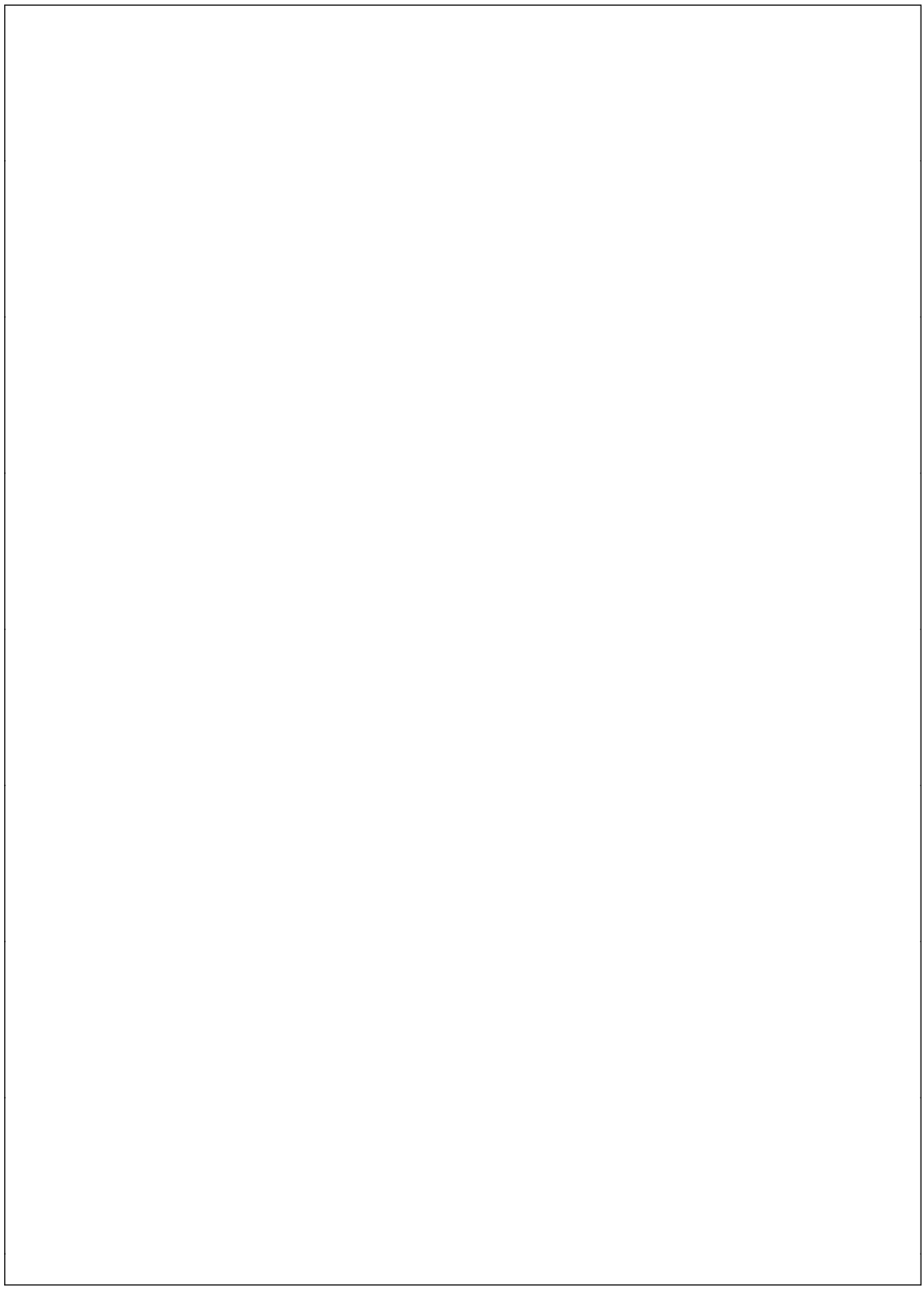
Since FACT logic devices are designed and processed differently from AC/ACT logic devices produced by other manufacturers, the preliminary results given here do not necessarily apply to all AC/ACT devices. We are currently in the process of increasing the data base for AC/ACT devices from other manufacturers, as well as continuing our testing program of National's FACT devices.

ACKNOWLEDGEMENTS

The authors would like to thank R.L. Walter, V.T. Tran, D.T. Katsuda, and W.J. Wong for providing technical assistance during preparation of the experiment. Thanks are also extended to the staff of the LBL 88″ cyclotron facility for their skillful beam delivery and control.

REFERENCES

1. K. Saliman and D.K. Nichols, *"Latchup in CMOS Devices from Heavy Ions",* IEEE Trans. Nucl. Sci., NS-30, pp. 4514–4519, 1983.
2. R. Koga, W.A. Kolasinski, M.T. Marra, and W.A. Hanna, *"Techniques of Microprocessor Testing and SEU-Rate Prediction",* IEEE Trans. Nucl. Sci., NS-32, pp. 4219–4224, 1985.
3. J.H. Sokol, W.A. Kolasinski, M. Wong, R. Koga, R.V. Suhrke, and T.H. Frey, *"Advantage of Advanced CMOS over Advanced TTL in a Cosmic Ray Environment",* IEEE Trans. Nucl. Sci., NS-34, pp. 1338–1340, 1987.
4. J. Fry, **FACT Radiation Test Results,** National Semiconductor Corporation, Maine, 1987.
5. M.C. Maher, *"Dose Rate Response of Advanced CMOS Products",* GOMAC DIGEST, pp. 143–145, 1989.
6. T. Chapuis and H. Constant, *"Latchup On CMOS/EPI Devices",* IEEE Trans. Nucl. Sci., this issue.



National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408