

Introducing the MF10: A Versatile Monolithic Active Filter Building Block

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Introducing the MF10: A Versatile Monolithic Active Filter Building Block

A unique alternative for active filter designs is now available with the introduction of the MF10. This new CMOS device can be used to implement precise, high-order filtering functions with no reactive components required.

Filter design takes one of two approaches: passive or active. Passive designs combine resistors, capacitors and inductors to perform specific frequency filtering in applications where precision is less important than mass producibility. For very high frequency applications, a passive approach is quite often the only way to go. Active filters combine op amps and discrete transistors, primarily with resistors and capacitors, to provide impedance buffering and filter parameter tunability. In precision filters, it is most desirable to have an independent "handle" for each of three basic filter parameters: resonant frequency (f_o), Q or quality factor, and the passband gain (H_o). As a general rule, the degree of tunability increases with the number of amplifiers used. The three op amp, state variable active filter, *Figure 1*, is most popular for 2nd order designs.

A major shortcoming of this type of filter is that resonant frequency accuracy is only as good as the capacitors used. In high volume production, to minimize filter tuning procedures, costly, low-tolerance, low-drift capacitors are required. Furthermore, these filters use a fair number of components; 3 op amps, 7 resistors and 2 capacitors for each 2nd order section. Even the best single amplifier 2nd order filter realizations require 3 to 5 resistors and 2 capacitors.

To offer designers an attractive alternative to these types of active filters, a device would have to:

- 1) eliminate critical capacitors entirely
- 2) minimize overall parts count
- 3) provide easy tunability of filter parameters
- 4) allow for the design of all five filter responses and,
- 5) simplify design equations.

These are the design objectives behind the development of the MF10. Recent advances in sample-data techniques permit the construction of an op amp integrator on a monolithic substrate without the need for any external capacitors (see page 11 "The Switched Capacitor Integrator—How it Works"). The integrator is a key factor in filter designs for establishing the overall filter time constant and, therefore, its resonant frequency. The MF10 contains, in one 20-pin DIP package, all of the necessary active and reactive components to construct two complete 2nd order state variable type active filters, *Figure 2*. The only external requirements are for resistors to establish the desired filter parameters.

BASIC CIRCUIT DESCRIPTION

To keep the device as universal as possible, the outputs of each section of each filter are brought out. This allows designs for all five filtering functions: lowpass, bandpass, highpass, allpass and bandreject or notch filters. With two independent 2nd order sections in one package, cascading to achieve 4th order responses can easily be accomplished. Additionally, any of the classical filter response types such as Butterworth, Chebyshev, Bessel and Cauer can be implemented.

Between the output of the summing op amp and the input of the first integrator there is a unique 3-input summing stage where two of the inputs are subtracted from the third. One of the (–) inputs is brought out to serve as the signal input for some filter configurations. The other (–) input is connected through an internal switch to either the lowpass output or analog ground depending upon the desired filter implementation. The direction of this input connection is common to both halves of the MF10 and is controlled by the voltage level on the $S_{A/B}$ input terminal.

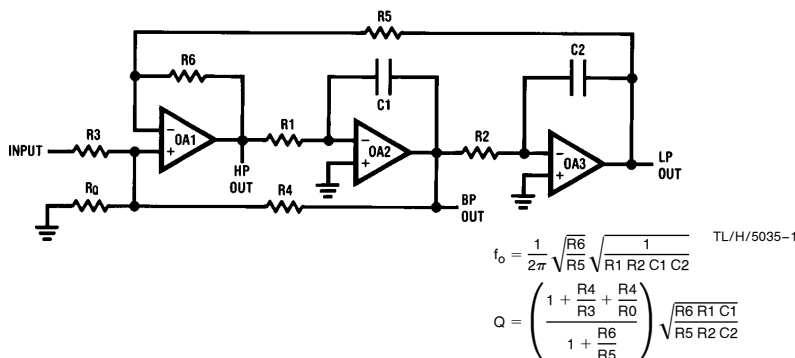


FIGURE 1. The Universal State Variable 2nd Order Active Filter
(note the complexity of design equations and the number of critical external components)

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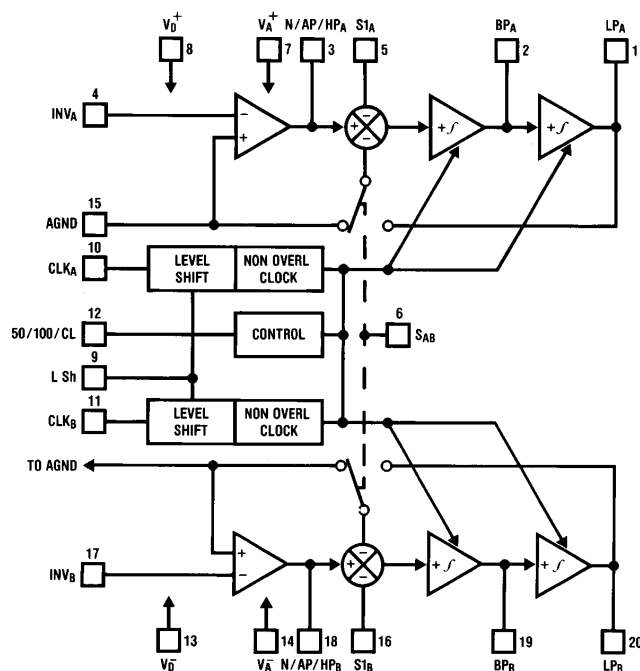


FIGURE 2. Block Diagram of the MF10

When tied to V_D^+ [the (+) supply], the switch connects the lowpass output, and when tied to V_D^- [the (-) supply], the connection to ground is made. In some applications one half of the MF10 may require that both of the (-) inputs to this summer be connected to ground, while the other side requires one to be connected to the lowpass output and the other to ground. For this, the $S_{A/B}$ control should be tied to the (-) supply and the connection to the lowpass output should be made externally to the $S1_A$ ($S1_B$) pin.

A clock with close to 50% duty cycle is required to control the resonant frequency of the filter. Either TTL or CMOS logic compatible clocks can be accommodated, whether the MF10 is powered from split supplies or a single supply, by simply grounding the level shift (L Sh) control pin.

The resonant frequency of each filter is directly controlled by its clock. A tri-level control pin sets the ratio of the clock frequency to the center frequency (the 50/100/CL pin) for both halves. When this pin is tied to V^+ the center frequency will be 1/50 of the clock frequency. When tied to mid-supply potential (i.e., ground, when biased from split supplies) provides 100 to 1 clock to center frequency operation. When this pin is tied to V^- a power saving supply current limiter shuts down operation and rolls back the supply current by 70%.

Filter center frequency accuracy and stability are only as good as the clock provided. Standard crystal oscillators, combined with digital counters, can provide very stable clocks for specific filter frequencies. A relatively new device from National's COPS family of microcontrollers and peripherals, the COP452 programmable frequency generator/counter, finds a unique use with the MF10, Figure 3. This low cost device can generate two independent 50% duty cycle clock frequencies. Each clock output is programmed

via a 16-bit serial data word (N). This allows over 64,000 different clock frequencies for the MF10 from a single crystal.

The MF10 is intended for use with center frequencies up to 20 kHz, and is guaranteed to operate with clocks up to 1 MHz. This means that for center frequencies greater than 10 kHz, the 50 to 1 clock control should be used. The effect of using 100 to 1 or 50 to 1 clock to center frequency ratio manifests itself in the number of "stair-steps" apparent in the output waveform. The MF10 closely approximates the time and frequency domain response of continuous filters (RC active filters, for example) but does so using sampling techniques. The clock to center frequency control determines the number of samples taken (1 per clock cycle) in one cycle of the center frequency. Therefore, as shown in the photo of Figure 4, 100 to 1 clocking provides a smoother looking output as it has twice as many samples per cycle. For most audio applications, the audible effects of these step edges and the clock frequency component in the output are negligible as they are beyond 20 kHz. To obtain a cleaner output waveform, a simple passive RC lowpass can be added to the output to serve as a smoothing filter without affecting the MF10 filtering action.

Several of the modes of operation (discussed in a later section) allow altering of the clock to center frequency ratio by an external resistor ratio. This can be used to obtain center frequencies of values other than 1/50 or 1/100 of the clock frequency. In multiple stage, staggered tuned filters, the center frequency of each stage can be set independently with resistors to allow the overall filter to be controlled by just one clock frequency.

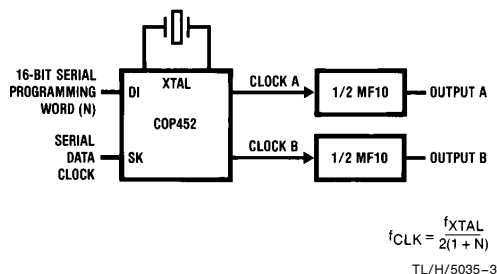


FIGURE 3. A Programmable Dual Clock Generator

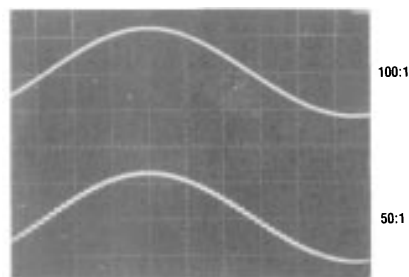
All of the rules of sampling theory apply when using the MF10. The sampling rate, or clock frequency, should be at least twice the maximum input frequency to produce the best equivalent to a continuous time filter. High frequency components in the input signal that approach the clock frequency will generate aliasing signals which appear at the output of the lower frequency filter and are indistinguishable from valid passband signals. Bandlimiting the input signal to attenuate these potential aliasing frequencies is the best preventative measure. In most applications, aliasing will not be a problem as the clock frequency is much higher than the passband of interest. In the event that a much higher clock frequency is required, the modes of operation which utilize external resistor ratios to increase the clock to center frequency ratio can extend the clock frequency to greater than 100 times the center frequency. By using a higher clock frequency, the aliasing frequencies are correspondingly higher. The limiting factor, with regard to increasing the clock to center frequency ratio, has to do with increased DC offsets at the various outputs.

THE BASIC FILTER CONFIGURATIONS

There are six basic configurations (or modes of operation) for the 2nd order sections in the MF10 to realize a wide variety of filter responses. In all cases, no external capacitors are required. Design is a simple matter of establishing a few resistor ratios to set the desired passband gain and Q and generating a clock for the proper resonant frequency. Each 2nd order section can be treated in a modular fashion, with regard to individual center frequency, Q and gain, when cascading either the two sections within a package or several packages for very high order filters. This individuality of sections is important in implementing the various response characteristics such as Butterworth, Chebyshev, etc.

The following is a general summary of design hints common to all modes of operation.

- 1) The maximum supply voltage for the MF10 is $\pm 7V$ or just $+ 14V$ for single supply operation. The minimum supply to properly bias the part is $8V$.



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FIGURE 4. The Sampled-Data Output Waveform

- 2) The maximum swing at any of the outputs is typically within 1V of either supply rail.
- 3) The internal op amps can source 3 mA and sink 1.5 mA. This is an important criterion when selecting a minimum resistor value.
- 4) The maximum clock frequency is typically 1.5 MHz.
- 5) To insure the proper filter response, the $f_o \times Q$ product of each stage must be realizable by the MF10. For center frequencies less than 5 kHz, the $f_o \times Q$ product can be as high as 300 kHz (Q must be less than or equal to 150). A 3 kHz bandpass filter, for example, could have a Q as high as 100 with just one section. For center frequencies less than 20 kHz, the allowable $f_o \times Q$ product is limited to 200 kHz. A 10 kHz bandpass design using a single section should have a Q no larger than 20.
- 6) Center frequency matching from part to part for a given clock frequency is typically $\pm 0.2\%$. Center frequency drift with temperature (excluding any clock frequency drift) is typically ± 10 ppm/ $^{\circ}C$ with 50:1 switching and ± 100 ppm/ $^{\circ}C$ for 100:1.
- 7) Q accuracy from part to part is typically $\pm 2\%$ with a temperature coefficient of ± 500 ppm/ $^{\circ}C$.
- 8) The expressions for circuit dynamics given with each of the modes are important. They determine the voltage swing at each output as a function of the circuit Q. A high Q bandpass design can generate a significant peak in the response at the lowpass output at the center frequency.
- 9) Both sides of the MF10 are independent, except for supply voltages, analog ground, clock to center frequency ratio setting and internal switch setting for the three input summing stage.

In the following descriptions of the filter configurations, f_o is the filter center frequency, H_o is the passband gain and Q is the quality factor of the complex pole pair and is equal to f_o / BW where BW is the -3 dB bandwidth measured at the bandpass output.

MODE 1A: Non-Inverting Bandpass, Inverting Bandpass, Lowpass

This is a minimum external component configuration (only 2 resistors) useful for low Q lowpass and bandpass applications. The non-inverting bandpass output is necessary for minimum phase filter designs.

Design Equations

$$f_o = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$Q = \frac{R3}{R2}$$

$$H_{OLP} = -1$$

$$H_{OBP1} = -\frac{R3}{R2}$$

$$H_{OBP2} = 1 \text{ (non-inverting)}$$

Circuit Dynamics

$H_{OBP1} = -Q$ (this is the reason for the low Q recommendation)

$$H_{OLP \text{ (peak)}} = Q \times H_{OLP}$$

MODE 1: Notch, Bandpass and Lowpass

With the addition of just one more external resistor, the output dynamics are improved over Mode 1A to allow bandpass designs with a much higher Q. The notch output features equal gain above and below the notch frequency.

Design Equations

$$f_o = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$f_{notch} = f_o$$

$$Q = \frac{R3}{R2}$$

$$H_{OLP} = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

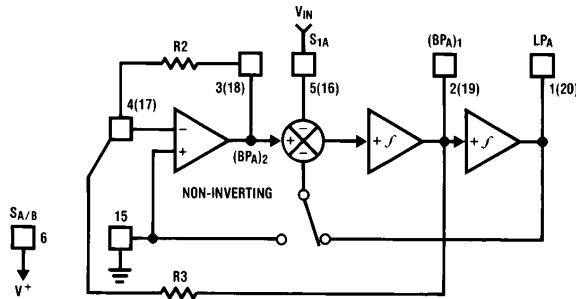
$$H_{ON} = -\frac{R2}{R1} \text{ as } f \rightarrow 0 \text{ and as } f \rightarrow \frac{f_{CLK}}{2}$$

Circuit Dynamics

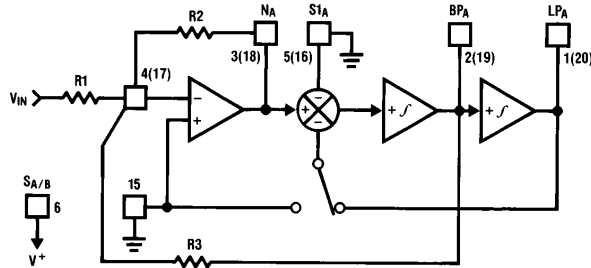
$$H_{OBP} = H_{OLP} \times Q = H_{ON} \times Q$$

$H_{OLP \text{ (peak)}} = Q \times H_{OLP}$ (if the DC gain of the LP output is too high, a high Q value could cause clipping at the lowpass output resulting in gain non-linearity and distortion at the bandpass output).

MODE 1A



MODE 1



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MODE 2: Notch (with $f_n \leq f_o$), Bandpass and Lowpass

This configuration allows tuning of the clock to center frequency ratio to values greater than 100 to 1 or 50 to 1. The notch output is useful for designing elliptic highpass filters because the frequency of the required complex zeros (f_{notch}) is less than the frequency of the complex poles (f_o).

Design Equations

$$f_o = \frac{f_{\text{CLK}}}{100} \sqrt{1 + \frac{R_2}{R_4}} \text{ or } \frac{f_{\text{CLK}}}{50} \sqrt{1 + \frac{R_2}{R_4}}$$

$$f_n = \frac{f_{\text{CLK}}}{100} \text{ or } \frac{f_{\text{CLK}}}{50}$$

$$Q = \frac{\sqrt{R_2/R_4 + 1}}{R_2/R_3}$$

$$H_{\text{OLP}} = \frac{-\frac{R_2}{R_1}}{1 + \frac{R_2}{R_4}}$$

$$H_{\text{OBP}} = -\frac{R_3}{R_1}$$

$$H_{\text{ON}_1} \left(\text{as } f \rightarrow 0 \right) = \frac{-\frac{R_2}{R_1}}{1 + \frac{R_2}{R_4}}$$

$$H_{\text{ON}_2} \left(\text{as } f \rightarrow \frac{f_{\text{CLK}}}{2} \right) = -\frac{R_2}{R_1}$$

Circuit Dynamics

$$H_{\text{OBP}} = Q \sqrt{H_{\text{OLP}} \times H_{\text{ON}_2}} = Q \sqrt{H_{\text{ON}_1} \times H_{\text{ON}_2}}$$

MODE 3: Highpass, Bandpass and Lowpass

This configuration is the classical state variable filter (the circuit of Figure 1) implemented with only 4 external resistors. This is the most versatile mode of operation, since the clock to center frequency ratio can be externally tuned either above or below the 100 to 1 or 50 to 1 values. The circuit is suitable for multiple stage Chebyshev filters controlled by a single clock.

Design Equations

$$f_o = \frac{f_{\text{CLK}}}{100} \sqrt{\frac{R_2}{R_4}} \text{ or } \frac{f_{\text{CLK}}}{50} \sqrt{\frac{R_2}{R_4}}$$

$$Q = \sqrt{\frac{R_2}{R_4}} \times \frac{R_3}{R_2}$$

$$H_{\text{OHP}} = -\frac{R_2}{R_1}$$

$$H_{\text{OBP}} = -\frac{R_3}{R_1}$$

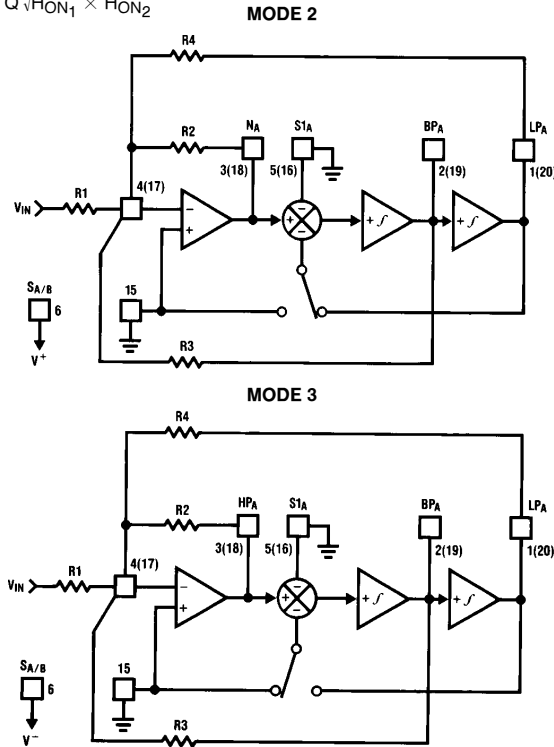
$$H_{\text{OLP}} = -\frac{R_4}{R_1}$$

Circuit Dynamics

$$H_{\text{OHP}} = H_{\text{OLP}} \left(\frac{R_2}{R_4} \right)$$

$$H_{\text{OBP}} = Q \sqrt{H_{\text{OHP}} \times H_{\text{OLP}}}$$

$$H_{\text{OHP}} (\text{peak}) = Q \times H_{\text{OHP}}$$



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MODE 3A: Highpass, Bandpass, Lowpass and Notch

A notch output is created from the circuit of Mode 3 by summing the highpass and lowpass outputs through an external op amp. The ratio of the summing resistors R_h and R_l adjusts the notch frequency independent of the center frequency. For elliptic filter designs, each stage combines a complex pole pair (at f_o) with a complex zero pair (at f_{notch}) and this configuration provides easy tuning of each of these frequencies for any response type. When cascading several stages of the MF10 the external op amp is needed only at the final output stage. The summing junction for the intermediate stages can be the inverting input of the MF10 internal op amp.

Design Equations

$$f_o = \frac{f_{CLK}}{100} \sqrt{\frac{R_2}{R_4}} \text{ or } \frac{f_{CLK}}{50} \sqrt{\frac{R_2}{R_4}}$$

$$Q = \sqrt{\frac{R_2}{R_4}} \times \frac{R_3}{R_2}$$

$$f_{notch} = \frac{f_{CLK}}{100} \sqrt{\frac{R_h}{R_l}} \text{ or } \frac{f_{CLK}}{50} \sqrt{\frac{R_h}{R_l}}$$

$$H_{OHP} = -\frac{R_2}{R_1}$$

$$H_{OLP} = -\frac{R_4}{R_1}$$

$$H_{OBP} = -\frac{R_3}{R_1}$$

$$H_{ON} \text{ (at } f = f_o) = \left| Q \left(\frac{R_g}{R_l} H_{OLP} - \frac{R_g}{R_h} H_{OHP} \right) \right|$$

$$H_{ONl} \text{ (as } f \rightarrow 0) = \frac{R_g}{R_l} \times H_{OLP}$$

$$H_{ONh} \left(\text{as } f \rightarrow \frac{f_{CLK}}{2} \right) = \frac{R_g}{R_h} \times H_{OHP}$$

MODE 4: Allpass, Bandpass and Lowpass

Utilizing the $S1_A$ ($S1_B$) terminal as a signal input, an allpass function can be obtained. An allpass can provide a linear phase change with frequency which results in a constant time delay. This configuration restricts the gain at the allpass output to be unity.

Design Equations

$$f_o = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$f_z \text{ (frequency of complex zero pair)} = f_o$$

$$Q = \frac{R_3}{R_2}$$

$$Q_z \text{ (Q of complex zero pair)} = \frac{R_3}{R_1}$$

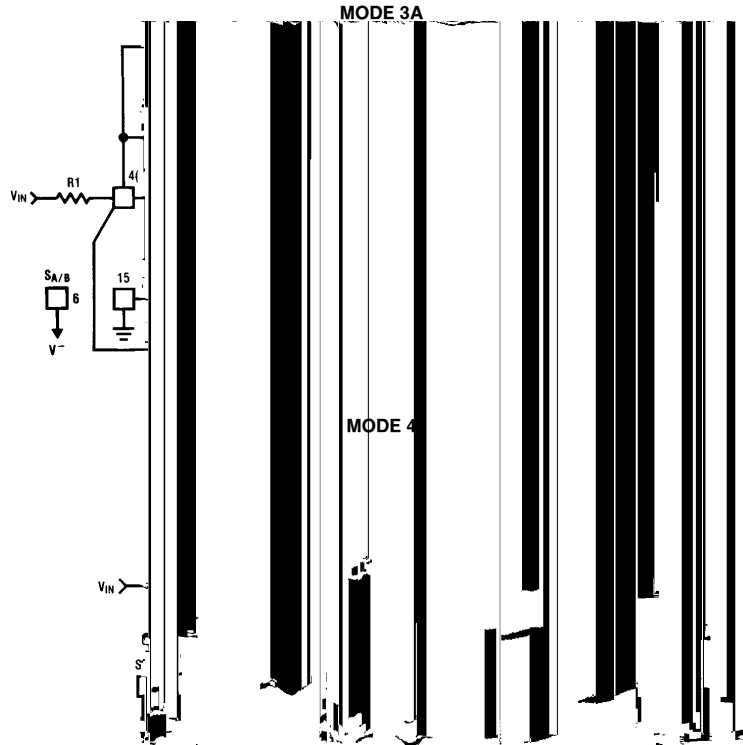
$$H_{OAP} = -\frac{R_2}{R_1} = -1$$

$$H_{OLP} = -\left(\frac{R_2}{R_1} + 1 \right) = -2$$

$$H_{OBP} = -\left(1 + \frac{R_2}{R_1} \right) \frac{R_3}{R_2} = -2 \frac{R_3}{R_2}$$

Circuit Dynamics

$$H_{OBP} = H_{OLP} \times Q = (H_{OAP} + 1)Q$$



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MODE 5: Complex Zeros (C.z), Bandpass and Lowpass

This mode features an improved allpass design over that of Mode 4, in that it maintains a more constant amplitude with frequency at the complex zeros (C.z) output. The frequencies of the pole pair and zero pair are resistor tunable.

Design Equations

$$f_o = \frac{f_{CLK}}{100} \sqrt{1 + \frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \sqrt{1 + \frac{R2}{R4}}$$

$$f_z = \frac{f_{CLK}}{100} \sqrt{1 - \frac{R1}{R4}} \text{ or } \frac{f_{CLK}}{50} \sqrt{1 - \frac{R1}{R4}}$$

$$Q = \frac{R3}{R2} \sqrt{1 + \frac{R2}{R4}}$$

$$Q_z = \frac{R3}{R1} \sqrt{1 - \frac{R1}{R4}}$$

$$H_{O(C.z)} \text{ as } f \rightarrow 0 = \frac{R2(R4 - R1)}{R1(R2 + R4)}$$

$$H_{O(C.z)} \text{ as } f \rightarrow \frac{f_{CLK}}{2} = \frac{R2}{R1}$$

$$H_{OBP} = \frac{R3}{R2} \left(1 + \frac{R2}{R1} \right)$$

$$H_{OLP} = \frac{R4}{R1} \left(\frac{R2 + R1}{R2 + R4} \right)$$

MODE 6A: Single Pole, Highpass and Lowpass

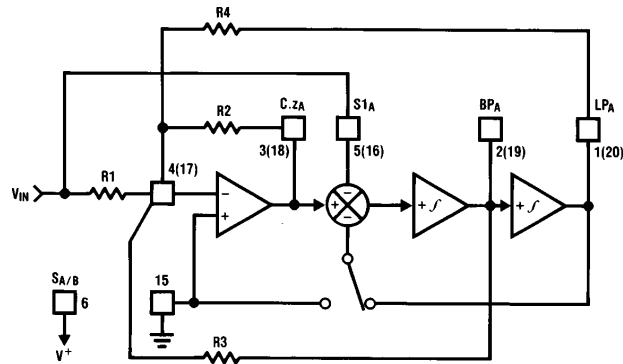
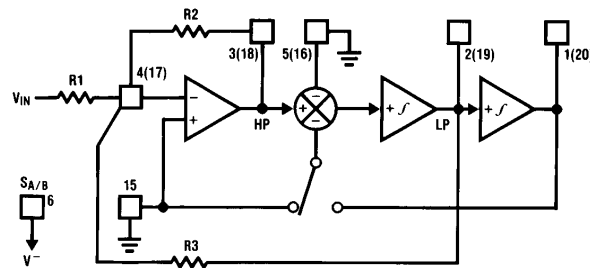
By using only one of the internal integrators, this mode is useful for creating odd-ordered cascaded filter responses by providing a real pole that is clock tunable to track the resonant frequency of other 2nd order MF10 sections. The corner frequency is resistor tunable.

Design Equations

$$f_c \text{ (cut-off frequency)} = \frac{f_{CLK}}{100} \left(\frac{R2}{R3} \right) \text{ or } \frac{f_{CLK}}{50} \left(\frac{R2}{R3} \right)$$

$$H_{OLP} = -\frac{R3}{R1}$$

$$H_{OHP} = -\frac{R2}{R1}$$

MODE 5**MODE 6A**

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MODE 6B: Single Pole Lowpass (Inverting and Non-Inverting)

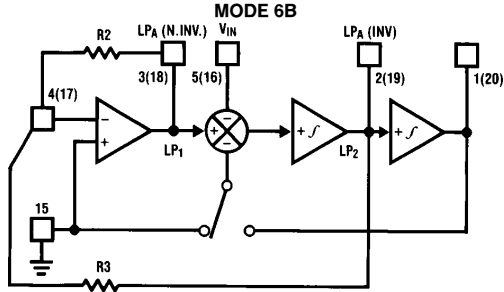
This mode utilizes only one of the integrators for a single pole lowpass, and the input op amp as an inverting amplifier, to provide non-inverting lowpass output. Again, this mode is useful for designing odd-ordered lowpass filters.

Design Equations

$$f_c \text{ (cut-off frequency)} = \frac{f_{CLK}}{100} \left(\frac{R_2}{R_3} \right) \text{ or } \frac{f_{CLK}}{50} \left(\frac{R_2}{R_3} \right)$$

$$H_{OLP} \text{ (inverting output)} = -\frac{R_3}{R_2}$$

$$H_{OLP} \text{ (non-inverting output)} = +1$$



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SOME SPECIFIC APPLICATION EXAMPLES

For single-supply operation, it is important for several terminals to be biased to half supply. A single-supply design for a 4th order 1 kHz Butterworth lowpass (24 dB/octave or 80 dB/decade rolloff) is shown using Mode 1 in Figure 5. Note that the analog ground terminal (pin 15), the summer inputs S1A and S1B (pins 5 and 16) and the clock switching control pin (pin 12) are all biased to $V_{CC}/2$. For symmetrical

split supply operation these pins would be grounded. An input coupling capacitor is optional, as it is needed only if the input signal is not also biased to $V_{CC}/2$. For a two-stage Butterworth response, both stages have the same corner frequency, hence the common clock for both sides. The resistor values shown are the nearest 5% tolerance values used to set the overall gain of the filter to unity and to set the required Q of the first stage (side A) to 0.504 and the second stage (side B) Q to 1.306 for a flat passband response.

A unique advantage of the switched capacitor design of the MF10 is illustrated in Figure 6. Here the MF10 serves double duty in a data acquisition system as an input filter for simple bandlimiting or anti-aliasing and, as a sample and hold to allow larger amplitude, higher frequency input signals. By gating OFF the applied clock, the switched capacitor integrators will hold the last sampled voltage value. The droop rate of the output voltage during the hold time is approximately 0.1 mV per ms.

A useful non-filtering application of the MF10 is shown in Figure 7. In this circuit, the MF10, together with an LM311 comparator, are used as a resonator to generate stable amplitude sine and cosine outputs without using AGC circuitry. The MF10 operates as a Q of 10 bandpass filter which will ring at its resonant frequency in response to a step input change. This ringing signal is fed to the LM311 which creates a square wave input signal to the bandpass to regenerate the oscillation. The bandpass output is the filtered fundamental frequency of a 50% duty cycle square wave. A 90° phase shifted signal of the same amplitude is available at the lowpass output through the second integrator in the MF10. The frequency of oscillation is set by the center frequency of the filter as controlled by the clock and the 50:1/100:1 control pin. The output amplitude is set by the peak to peak swing of the square wave input, which in this circuit is defined by the back to back diode clamps at the LM311 output.

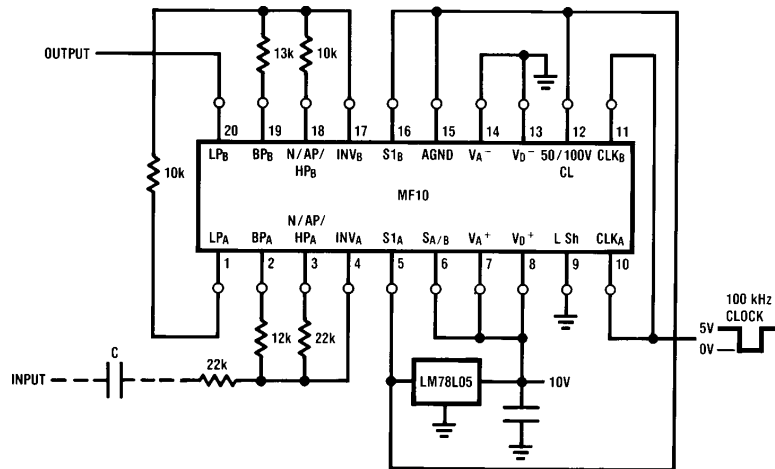


FIGURE 5. Only 6 resistors required for this 4th order, 1 kHz Butterworth lowpass filter. This example also illustrates single-supply biasing.

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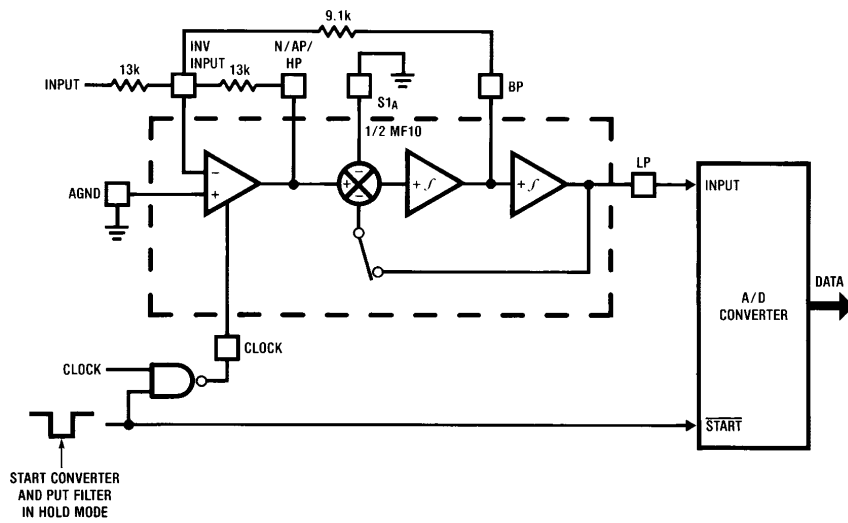


FIGURE 6. An MF10 as an Input Filter and Sample/Hold

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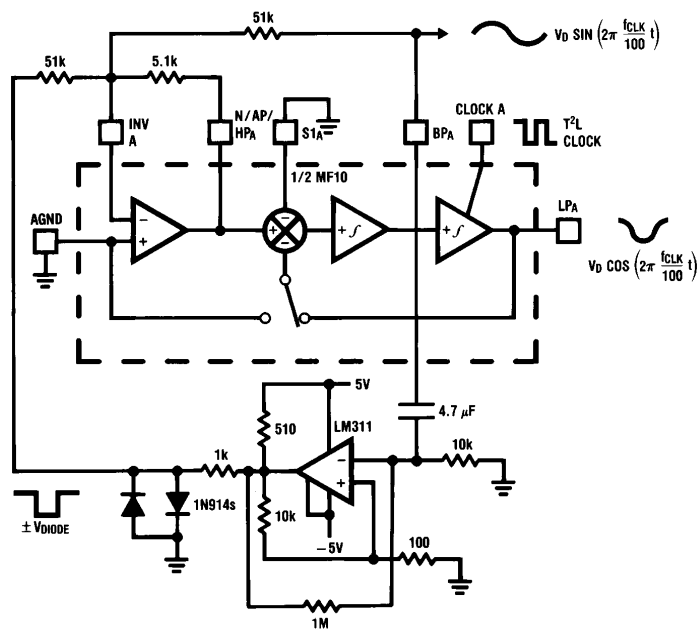


FIGURE 7. Generating Quadrature Sine Waves from a T2L Clock

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Finally, as a graphic illustration of the simplicity of filter implementation using the MF10, *Figure 8* is a complete 300 baud, full-duplex modem filter. The filter is an 8th order, 1 dB ripple Chebyshev bandpass which functions as both an 1170 Hz originate filter and a 2125 Hz answer filter. Control of answer or originate operation is set by the logic level at the 50/100/CL input so that only one clock frequency is required. The overall filter gain is 22 dB.

Construction of this filter on a printed circuit board would obviously be more compact than an RC active filter approach and much more cost effective for the level of precision required. An even more attractive implementation from a space savings point of view would be a hybrid circuit approach. A film resistor array connecting to two MF10 die could produce the entire filter in one package requiring only 7 external connections for input, output, supplies, etc.

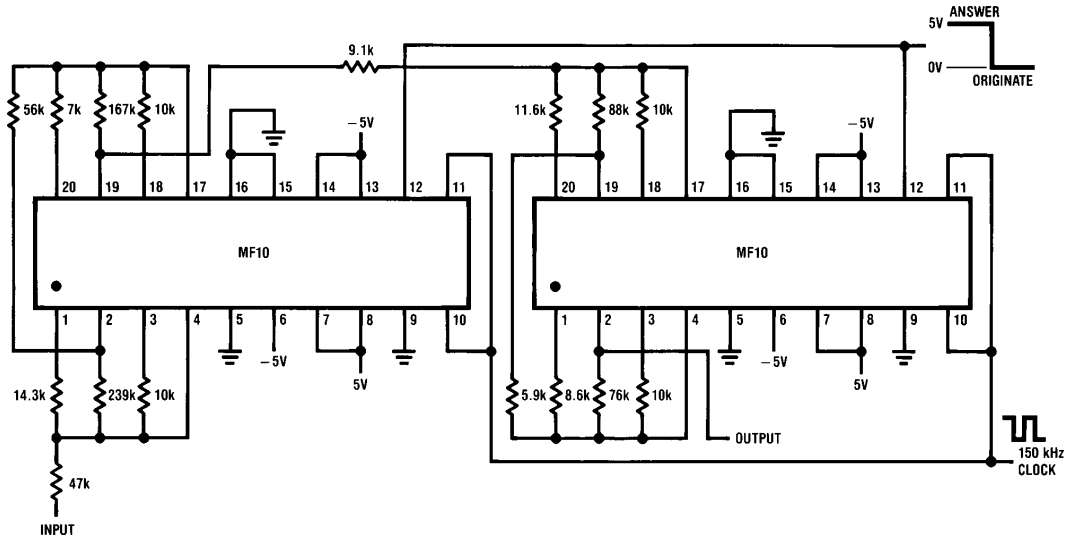


FIGURE 8. A Complete Full-Duplex 300 Baud Modem Filter

TL/H/5035-12

THE SWITCHED CAPACITOR INTEGRATOR—HOW IT WORKS

The most important feature of the MF10 is that it requires no external capacitors, yet can implement filters over a wide range of frequencies. A clock is used to control the time constant of two non-inverting integrators. To feel comfortable with the operation of the MF10, it is important to understand how this control is accomplished.

It is easiest to discuss an inverting integrator (*Figure A*) and how its input resistor can be replaced by 2 switches and a capacitor (*Figure B*). In *Figure A* the current which flows through feedback capacitor C is equal to V_{IN}/R and the circuit time constant is RC . This time constant accuracy depends on the absolute accuracy of two completely different discrete components. In *Figure B*, switches $S1$ and $S2$ are alternately closed by the clock. When switch $S1$ is closed ($S2$ is opened), capacitor $C1$ charges up to V_{IN} . At the end of half a clock period, the charge on $C1$ ($QC1$) is equal to $V_{IN} \times C1$. When the clock changes state, $S1$ opens and $S2$ closes. During this half of the clock period all of the charge on $C1$ gets transferred to the feedback capacitor $C2$.

The amount of charge transferred from the input, V_{IN} , to the summing junction [the $(-)$ input] of the op amp during one complete clock period is $V_{IN}C1$. Recall that electrical current is defined as the amount of charge that passes through a conduction path during a specific time interval (1 ampere = 1 coulomb per second). For this circuit, the current which flows through $C2$ to the output is:

$$I = \frac{\Delta Q}{\Delta t} = \frac{V_{IN}C1}{T} = V_{IN}C1 f_{CLK}$$

where T is equal to the clock period.

The effective resistance from V_{IN} to the $(-)$ input is therefore:

$$R = \frac{V_{IN}}{I} = \frac{1}{C1 f_{CLK}}$$

This means that $S1$, $S2$ and $C1$, when clocked in *Figure B*, act the same as the resistor in *Figure A* to yield a clock tunable time constant of:

$$\tau = \frac{C2}{C1 f_{CLK}}$$

Note that the time constant of the switched capacitor integrator is dependent on a *ratio* of two capacitor values, which, when fabricated on the same die, is very easy to control. This can provide precise filter resonant frequency control both from part to part and with changes in temperature.

The actual integrators used in the MF10 are non-inverting, requiring a slightly more elegant switching scheme, as shown in *Figure C*. In this circuit, $S1_A$ and $S1_B$ are closed together to charge $C1$ to V_{IN} . Then $S2_A$ and $S2_B$ are closed to connect $C1$ to the summing junction with the capacitor plates reversed, to provide the non-inverting operation. If V_{IN} is positive, V_{OUT} will move positive as $C2$ acquires the charge from $C1$.

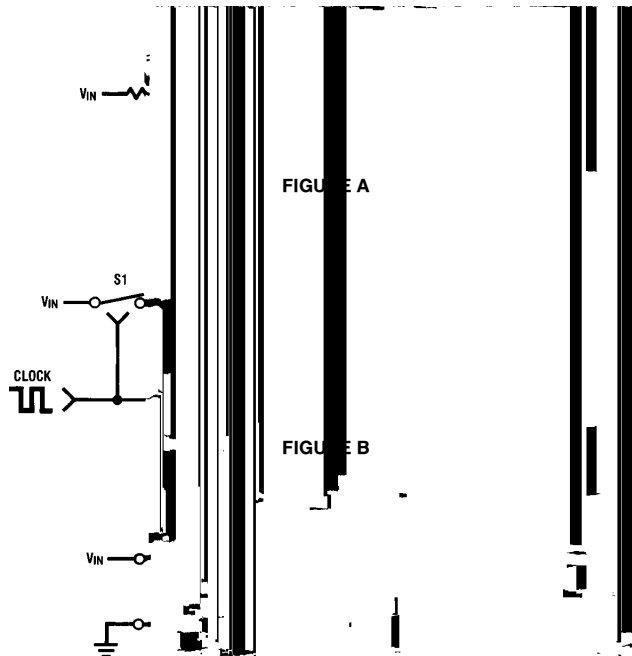


FIGURE C. The Non-Inverting Integrator Used in the MF10

TL/H/5035-13

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