

Applications of Wide-Band Buffer Amplifiers

National Semiconductor
Application Note 227
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INTRODUCTION

The LH0002, LH0033 and LH0063 are wide-band, high current, unity gain buffer amplifiers. They are intended for use alone or in closed-loop combination with op amps to drive co-axial cables and capacitive or other high-current loads. Features and characteristics of these buffers are summarized in Table I. All are active trimmed for low unadjusted output offset voltage and uniform performance. Good thermal coupling between dice is achieved by hybrid thick-film construction on ceramic substrates.

Part I analyzes the AC and DC equivalent circuits.

Part II is a comprehensive guide to applications techniques and shows how to get optimum performance under a variety of circumstances.

Finally, Part III illustrates these techniques in some specific applications including drivers, sample-and-hold amplifiers and active filters.

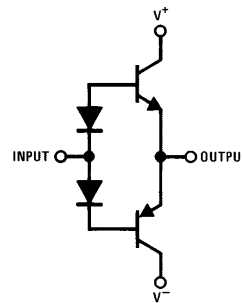
I. CIRCUIT DESCRIPTIONS

General

The three buffer amplifiers share a similar class AB emitter-follower output stage as shown in *Figure 1*. The symmetrical class AB amplifier output provides current sourcing or sinking and relatively constant low impedance to the load during positive and negative output swing. The input stage of the LH0002 consists of a complementary bipolar emitter-follower. The LH0033 and LH0063 employ junction FETs configured as source-followers, thereby achieving several orders of magnitude improvement in DC input resistance over the LH0002. In each case, the output stage collectors are uncommitted to allow the use of current limiting resistors in series with either or both output collectors.

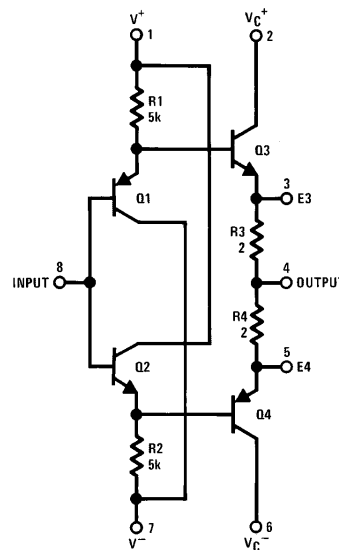
LH0002 Low Frequency Operation

The LH0002 circuit shown in *Figure 2* is a compound emitter-follower with small-signal current gain of approximately 40,000 (product of first and second stage betas).



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FIGURE 1. LH0002 Simplified Output Stage



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FIGURE 2. LH0002 Schematic Diagram

TABLE I. Buffer Amplifier Typical Characteristics

Parameter	Conditions	LH0002	LH0033	LH0063	Units
DC Output Current Continuous		±100	±100	±250	mA
Peak Output Current		±200	±250	±500	mA
Slew Rate	$R_L = 1 \text{ k}\Omega$, $R_S = 50 \Omega$	200	1500	6000	V/ μ s
Bandwidth, 3 dB		50	100	180	MHz
Voltage Gain	$V_{IN} = 1 \text{ V @ } 1 \text{ kHz}$, $R_L = 1 \text{ k}$	0.97	0.98	0.98	V/V
Output Offset Voltage	$T_C = 25^\circ\text{C}$, $R_S = 100 \text{ k}\Omega$ ($R_S = 300 \Omega$ for LH0002)	±10	±5	±10	mV
Input Bias Current	$T_C = 25^\circ\text{C}$	6 μ A	50 pA	100 pA	
Output Resistance		6	6	1	Ω

Operation is symmetrical, and the circuit may be analyzed by considering only the upper or the lower half of the circuit as redrawn in *Figure 3*. Input stage operating current is determined by R1 in conjunction with supply and input voltages. For $V_{IN} = 0$ and $V_S = \pm 15V$, first stage quiescent current is typically:

$$I_C = \frac{V_S - V_{BE} - V_{IN}}{R1} = \frac{15 - 0.63 - 0}{5000\Omega} = 2.88 \text{ mA} \quad (1)$$

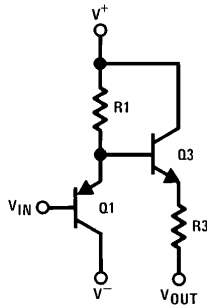
The normal production variation of I_C is $\pm 5\%$.

The emitter-base junction of the first and second stages appear in series between input and output terminals, therefore the output offset voltage for $V_{IN} = 0$ is the difference in base-emitter junction voltages of a PNP and an NPN transistor. This is true for both upper and lower halves of the circuit, so there is no conflict between the two circuit halves. Output stage quiescent current will equal that of the input stage if the transistors are matched and at equal temperatures. This establishes a class AB bias in the output stage so there is no class B crossover distortion in the output. Resistors R3 and R4 inserted in the output emitter circuits minimize the effect of unmatched upper and lower circuit halves and limit the potential for thermal runaway due to input and output stage temperature differences. There is no thermal runaway if operation is confined within data sheet limits.

Maximum output current is dependent on the supply voltage, R1, Q3 current gain, and the output voltage. Maximum current is available when V_{IN} rises sufficiently above V_{OUT} that Q1 is cut off. Under this condition, the 5k resistor supplies base current to Q3, and the maximum output current is:

$$\begin{aligned} I_{O(MAX)} &= \frac{V_S - V_{BE3} - I_O R3 - V_O}{R1/\beta_3} \\ &= \frac{V_S - V_{BE3}}{R1/\beta_3 + R3 + R_L} \approx \frac{V_S - 0.7}{30 + R_L} \end{aligned} \quad (2)$$

where $\beta_3 \approx 200$.



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FIGURE 3. LH0002 Half Circuit

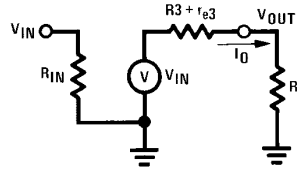
If $V_S = \pm 15V$, the LH0002 can theoretically deliver about 500 mA peak into a shorted load (in practice, only 400 mA peak can be realized, for the current density in the output transistors limits the beta to about 150) or 180 mA peak into 50Ω . Current limiting may be employed for short circuit protection (see section on Current Limiting).

The voltage gain of the LH0002 is slightly less than unity and is a function of load as with any emitter-follower. It is dominated by the finite output resistance of the output stage. Hence, the gain analysis for all three buffers can utilize the hybrid π model as shown in *Figure 4*. Note that r_{e3} is the emitter dynamic resistance of Q3 and is load-current dependent. The gain expression written as a function of load resistance and input voltage is:

$$\begin{aligned} A_v &\approx \frac{R_L}{R_L + R3 + r_{e3}} = \frac{R_L}{R3 + R_L \left(1 + \frac{0.026}{V_O + 0.003R_L} \right)} \\ &= \frac{R_L}{R3 + R_L \left(1 + \frac{0.026}{V_{IN}} \right)} \Bigg|_{V_{IN} > 0.1V} \end{aligned} \quad (3)$$

Voltage gain could range from 0.996 for $R_L = 1 \text{ k}\Omega$ to 0.978 for $R_L = 100\Omega$ at 10V input. In contrast, the same loads would yield gains of 0.973 to 0.956, respectively, for an input of 1V because r_{e3} would be somewhat larger.

Because of the inherent current-mode feedback, initial offset error is typically 10 mV with a finite (300Ω) series input resistance. Even with unsymmetrical supplies, V_{OS} increases only an additional 3 mV per volt of supply differential. Usually this error component may be ignored as it is relatively small compared to the large-signal error predicted by equation (3) when driving heavy loads.



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Where: $r_{e3} = 0.026/I_O$

FIGURE 4. Equivalent Model of LH0002

LH0002 High Frequency Operation

The high frequency response is limited primarily by internal circuit capacitances; most significant are the junction capacitances shown in *Figure 5*.

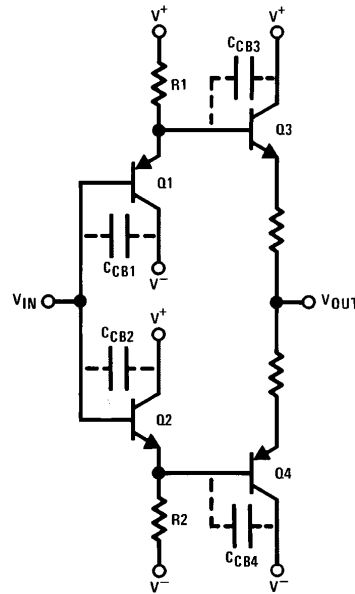
Since the base-emitter junction capacitances of emitter-followers see little effective junction voltage change, they may be neglected in the following first-order analysis. For the transistors used we may also assume that the transistor delay and transit time effects are over-shadowed by the RC effect. We can then simplify the half-circuit to that of *Figure 6*: a single transistor emitter-follower plus an equivalent load reflected from the output stage.

Evaluation of the transfer function of equation (4) as derived from *Figure 6b* indicates that the input pole dominates for finite source resistance.

$$\frac{e_o(s)}{e_{in}(s)} = \frac{\left(\frac{R_2}{R_2 + R_s} \right) \left(\frac{\beta_3 R_L}{\beta_3 R_L + r_{out}} \right)}{[1 + s(R_2 \parallel R_s) C'_{CB1}] [1 + s(r_{out} \parallel \beta_3 R_L) C_{CB3}]} \quad (4)$$

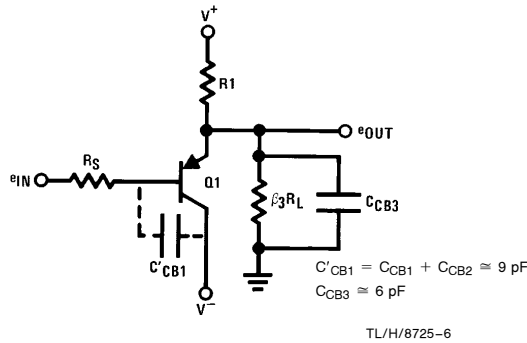
$$\cong \frac{A_V \text{ (low frequency)}}{(1 + s R_s C_{CB1}) (1 + s r_{e1} C_{CB3})}$$

To illustrate, for $R_s = 300\Omega$, the primary pole is predicted to occur at about 60 MHz, a close correlation to the real value, while the output pole is well beyond 1 GHz. The implication of this analysis is quite significant—the fundamental bandwidth of the LH0002 is a function of the input source resistance within a reasonable range of 50Ω to 300Ω . For the case of $R_s = 50\Omega$, the resulting bandwidth is well above 100 MHz.



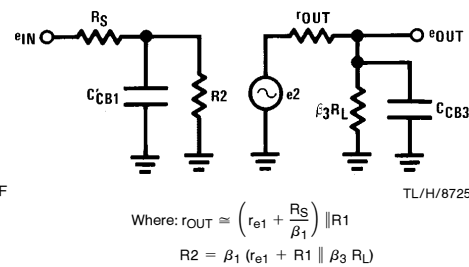
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FIGURE 5. LH0002 High Frequency Circuit



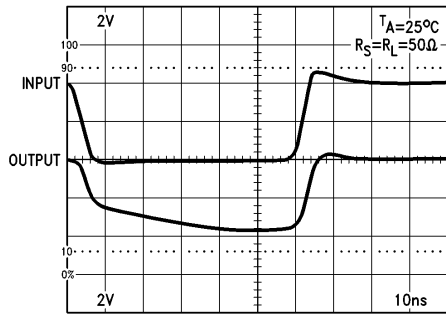
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FIGURE 6a. LH0002 Simplified Mirror-Half Input Stage



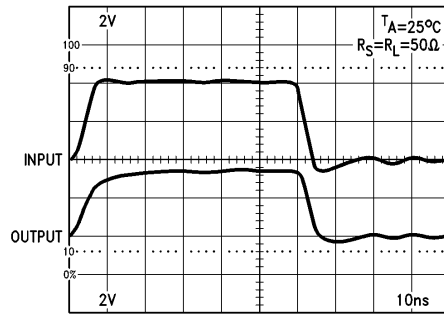
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FIGURE 6b. Hybrid π Model



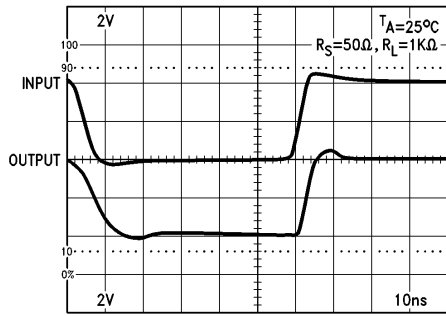
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a. Negative Pulse Response



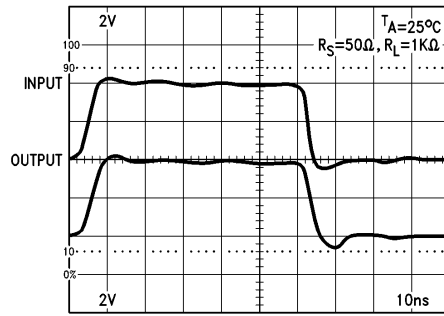
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b. Positive Pulse Response



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c. Negative Pulse Response



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d. Positive Pulse Response

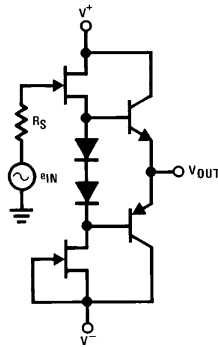
FIGURE 7. LH0002 Pulse Response

LH0002 Large Signal Pulse Response

Figure 7 shows the typical large signal pulse response of the LH0002.

LH0033 Low Frequency Operation

The LH0033 circuit can be described in simplified form, Figure 8, as a source-follower plus a balanced emitter-follower. The complete circuit is shown in Figure 9.

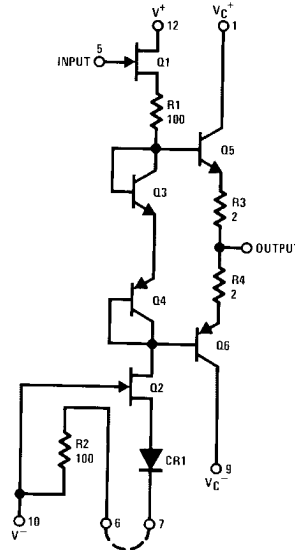


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FIGURE 8. LH0033 Simplified Circuit

When Q1 and Q2 are well matched, offset voltage and drift will be low because the gate-source voltage of Q2, V_{GS2} , is set $\approx 2 V_{BE}$, thus forcing $V_{GS1} = V_{GS2}$ due to the matching when operating at equal currents. However, as load current

is drawn from the output, Q1 and Q2 will drift at slightly different rates as I_{D1} will no longer equal I_{D2} by the difference in output stage base current. Resistor R2 is trimmed to establish the drain current of current-source transistor Q2 at 10 mA, and R1 is trimmed for zero offset.



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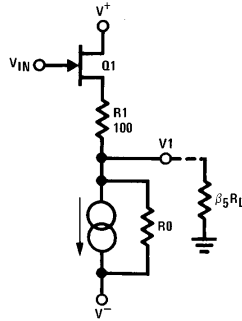
FIGURE 9. Complete LH0033 Schematic Diagram

The same current flowing through Q2 also flows through Q1 and R1, causing a gate-source voltage of approximately 1.6V. The 10 mA flowing through R1 plus Q3's V_{BE} of 0.6V causes $V_{OUT} = 0$ for $V_{IN} = 0$. The output stage current is established to be approximately equal to that of the input stage by Q3 and Q4.

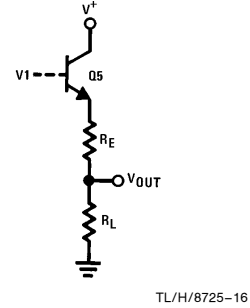
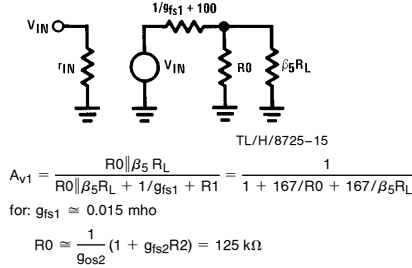
Voltage gain of the LH0033 is the product of the 1st and 2nd stage gains taken independently. The analysis of each is shown in Figure 10. We can write the total amplifier gain expression as:

$$A_V = \frac{1}{1 + 2/R_L + 167/\beta_5 R_L + 0.26/V_{IN}} \quad (5)$$

where $\beta_5 \approx 200$.



a. Hybrid π Model of FET Source-Follower Including Effect of Output Load



$$A_{V2} = \frac{R_L}{R_L + R_E + r_{e5}} = \frac{1}{1 + R_E/R_L + 0.026/V_1}$$

b. Output Stage Gain with the Effect of Emitter Dynamic Resistance

FIGURE 10. Voltage Gain Analysis of the LH0033

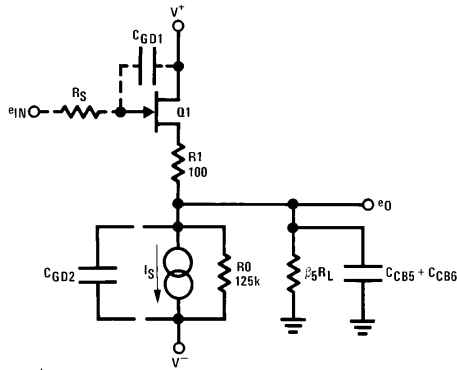
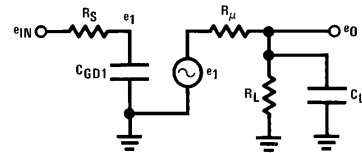


FIGURE 11. LH0033 Simplified Circuit



Where: $R_\mu = R_1 + 1/g_{fs1}$
 $R_L = R_0 \parallel \beta_5 R_L$
 $C_L = G_{GD2} + C_{CB5} + C_{CB6}$

FIGURE 12. LH0033 High Frequency Circuit Model

Capacitors C_{CB5} and C_{CB6} are collector-base junction capacitances of Q5 and Q6, typically 3 pF each. C_{GD1} and C_{GD2} are the gate-drain capacitances of the FETs, typically 3.5 pF each. The frequency-dependent transfer function of the circuit is:

$$\frac{e_o(s)}{e_{in}(s)} = \frac{R_L / (R_L \parallel R_1)}{[1 + s R_S C_{GD1}] [1 + s (R_\mu \parallel R_L) C_L]} \quad (6)$$

Notice that unlike the LH0002, the output pole ($s = 1/R_\mu C_L$) dominates the primary frequency response roll-off occurring at about 100 MHz with an input source resistance $R_S \approx 50\Omega$. The user is cautioned that as R_S increases, the secondary (input) pole will begin to take effect. To illustrate, for $R_S = 300\Omega$, the secondary pole will have moved from 900 MHz at $R_S = 50\Omega$ to about 150 MHz.

LH0033 Slew Rate

The slew rate of the buffer is predicted by equation (7),

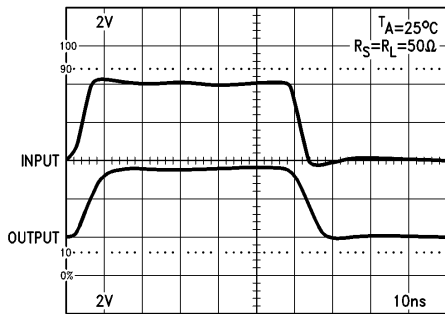
$$\frac{dv}{dt} \approx \frac{I}{C_L} \quad (7)$$

where I is the input stage current available to charge the circuit capacitance C_L .

With the LH0033, the positive slew is 2–3 times greater than the negative slew. The pulse response in *Figure 13* illustrates this. The reason is that during positive slew, the peak charging current is limited by the value of R_1 plus R_S when the FET gate-source junction is forward biased. This could be 30 mA–40 mA peak, allowing a typical slew rate of 3,000 V/ μ s.

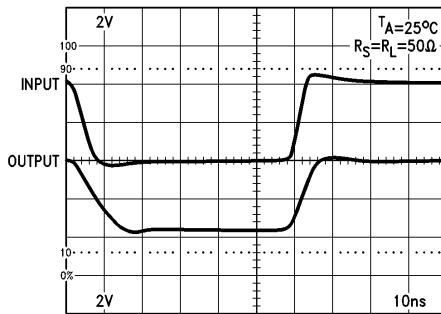
The LH0033 negative-going slew is limited by its input stage quiescent current of 10 mA established by the FET current source. As the input transistor tends to shut off, the circuit capacitance discharges into the current source (sink) at a rate of 10 mA. Therefore, the slew rate is computed to be:

$$\frac{dv}{dt} = \frac{10 \text{ mA}}{9.5 \text{ pF}} = 1,050 \text{ V}/\mu\text{s}$$



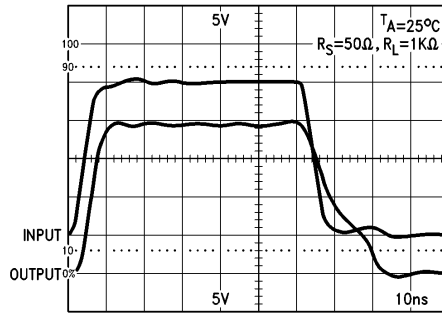
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a. Positive Pulse Response



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b. Negative Pulse Response



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c. ± 10 V Pulse Response

FIGURE 13. LH0033 Large Signal Pulse Response

LH0063 Low Frequency Operation

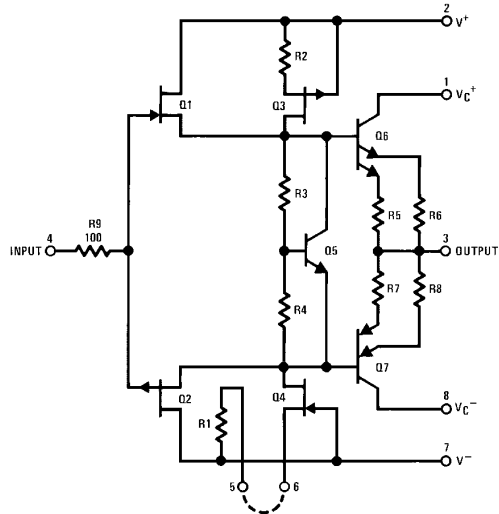
The LH0063 exhibits several times the slew rate and bandwidth of the LH0033 due to a higher input stage operating current. The push-pull design of the first stage also allows the input FETs to be forward biased for either positive or negative-going input signals. The schematic diagram of *Figure 14* shows a pair of complementary FETs at the input stage. Transistor Q1 is biased by the current source Q4. Resistor R1 is trimmed for a 30 mA input stage operating current. Similarly, Q2 is biased to 30 mA by the current source Q3 and R2. Transistor Q5 and resistors R3 and R4 establish a $2V_{BE}$ forward diode equivalent between the Q6 and Q7 bases. These resistors are trimmed such that the output stage operates at a quiescent current of about 1 mA. Each FET gate-source voltage cancels each output transistor V_{BE} drop. Hence, the output of the buffer sits at 0V for an input 0V. The zero-offset voltage-follower action holds for any input voltage within the buffer operating voltage range.

Because of the high current drive capability, multiple output transistors are employed to limit output transistor current density. Four output degeneration resistors of 1Ω each help to prevent thermal runaway.

The DC voltage gain equation is similar to that of the LH0033. Equation (5) may be used without introducing significant error. It needs modification only because of the multiple transistor output stage. Therefore, the LH0063 voltage gain equation is approximately:

$$A_v \approx \frac{1}{1 + 0.5/R_L + 1g_{fs1}\beta_6R_L + 0.026/2V_{IN}} \quad (8)$$

where: $\beta_6 \approx 200$, $g_{fs1}\beta_6 \approx 0.010$ mho.



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FIGURE 14. Complete LH0063 Schematic Diagram

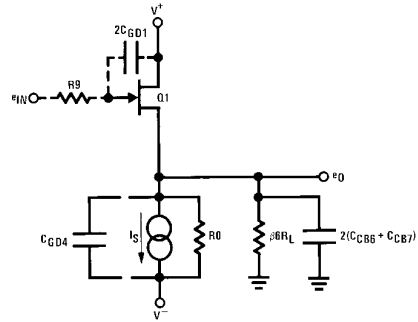
LH0063 High Frequency Operation

The high frequency equivalent circuit may omit the output stage, including only its load effect. The two mirrored half-circuits, consisting of a pair of complementary junction FETs and their respective current sources, can be reduced to a single half-circuit with the combined effect of both as shown in *Figure 15*.

The frequency-dependent transfer function of the LH0063 as derived from *Figure 15b* is:

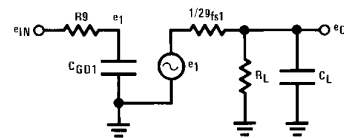
$$\begin{aligned} \frac{e_o(s)}{e_{IN}(s)} &= \frac{R_L / (R_L + 1/2g_{fs1})}{[1 + s2R_9 C_{GD1}] [1 + s \left(\frac{2}{2g_{fs1}} \parallel R_L \right) C_L]} \\ &= \frac{A_v (\text{low freq.})}{[1 + s2R_9 C_{GD1}] [1 + s \left(\frac{1}{2g_{fs1}} \right) C_L]} \end{aligned} \quad (9)$$

Similar to the LH0033, equation (9) indicates that the device output pole ($s = -2g_{fs1}/C_L$) dominates for small value input source resistance ($R_9 = 100\Omega$). Using the parameter values given in *Figure 15b*, equation (9) predicts the primary pole to occur at about 190 MHz, and the secondary (input) pole at beyond 300 MHz.



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a. Lumping the Combined Effects of Two Complementary Input Stages



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$$g_{fs1} \approx 0.010 \text{ mho}, R_L = R_0 \parallel \beta_6 R_L$$

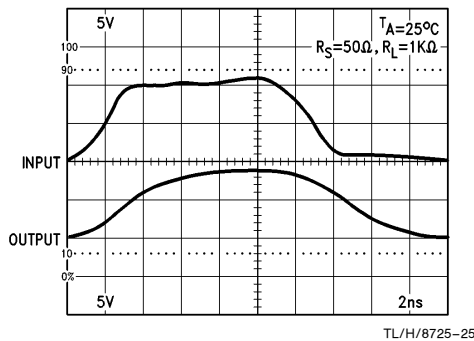
$$C_L = 2(C_{CB6} + C_{CB7}) + C_{GD4}$$

$$C_{CB6} \approx C_{CB7} = 3 \text{ pF}$$

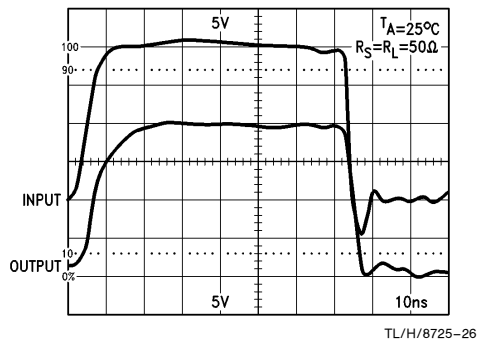
$$C_{GD1} \approx C_{GD4} = 3.5 \text{ pF}$$

b. Hybrid π Model of the Source Follower Substituted in the Composite Model

FIGURE 15. LH0063 Simplified High Frequency Circuit Model



a. Positive Pulse Response



b. ±10V Pulse Response

FIGURE 16. LH0063 Large Signal Pulse Response

LH0063 Large Signal Pulse Response

Figure 16 demonstrates the large signal pulse response capability of the LH0063 under different load conditions. Note the higher positive as well as negative-going slew rate achieved with the complementary FET input stage operating at higher current, a response superior to that of the LH0033.

II. APPLICATIONS INFORMATION

Circuit Layout Considerations

Circuit layout is one of the most important areas of high frequency circuit design. A sound design may yield only marginal performance when insufficient attention is given to circuit layout. This will be particularly important when the buffers are used with an op amp in a closed loop or when using very high frequency devices. The full performance capability of this family of buffers may be realized by following a few basic rules on circuit layout.

Good high frequency layout practice requires use of a ground plane wherever possible. A ground plane provides shielding (isolation) as well as a low-resistance, low-inductance circuit path to reduce undesirable high frequency coupling. In some cases, signal paths should be shielded by a surrounding ground plane to minimize stray signal pick-up; however, this shielding can cause increased stray capacitance which may be harmful at high impedance points in the circuit. Some care and judgement must be exercised in the amount and spacing of shielding ground plane areas. IC sockets should be avoided if possible because the increased inter-lead capacitance may degrade bandwidth or increase feedback capacitance in gain stages. Input and output connections should be kept short for compact physical layout and minimum coupling. When used with an op amp, layout should minimize capacitance from output to

feedback point and from feedback summing junction to ground. Supply and output signal traces should be as wide as practical for these high-current devices.

Power Supply Decoupling

The positive and negative power supply terminals of the devices must be bypassed to ground with one or two 0.1 μ F monolithic ceramic capacitors. They should be placed no more than 1/4 to 1/2 inch from the device pins. In difficult cases with the LH0033 and in all cases with the LH0063, a 4.7 μ F solid tantalum bypass should also be added at both the plus and minus supplies. The circuit board trace between capacitor ground points should be short and of low inductance.

Compensation

The three buffer amplifiers are inherently stable in applications with resistive loads and adequate supply bypassing. However, oscillation may occur in cases where a capacitive load of 100 pF or more is present. A series input resistance of 50 Ω –300 Ω will prevent this oscillation by compensating the negative input-resistance seen as a result of the reflected capacitive load. All source, cathode, or emitter-followers are subject to this phenomenon which is a result of transit time through the active region of the devices.

When these buffer amplifiers are placed within the feedback loop of a high-gain op amp, the phase margin of the operational amplifier is reduced by an additional amount equal to the phase lag of the buffer. Readjustment of circuit compensation may be required to insure stability. For additional information see the section on Closed-Loop Feedback Applications.

Power Dissipation and Device Rating

Each data sheet specifies the conditions for safe operating power dissipation. These limits must be observed for both continuous and pulsed conditions. *Figure 17* shows the power dissipation limits versus temperature for each device, both with and without heat sinks. To compute total power dissipation, the standby power must be added to the load-related power.

The standby power drain is computed from the device DC operating current and its operating voltage:

$$P_{\text{standby}} = (V_S^+ - V_S^-)I_S \quad (10)$$

The load-related power is the average power dissipated in the output stage. It may be estimated as the product of average current delivered to the load and the average voltage across the output stage. Because of the high-current capability of the buffers, it is essential to observe the device dissipation limits. Safe operating areas for each buffer are presented in *Figure 18*. A note of caution: these plots are valid only for 25°C ambient. Additional power derating based on the power derating curves of *Figure 17* is mandatory for operation at higher ambient temperature.

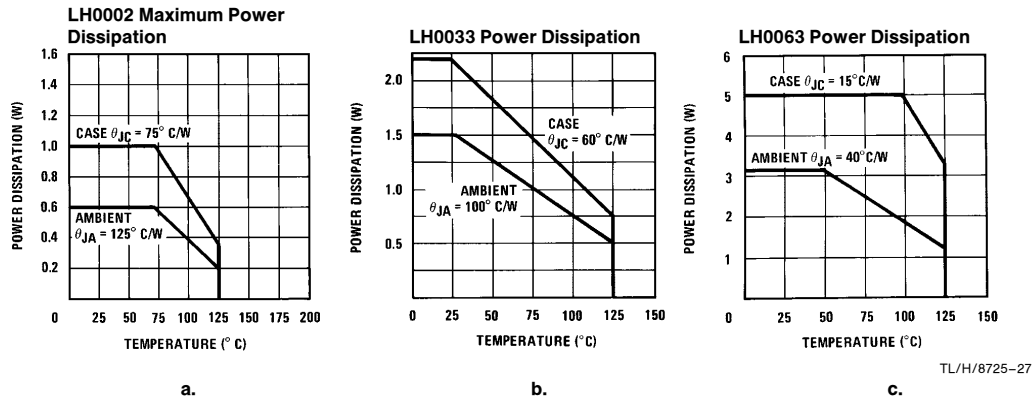


FIGURE 17. Device Power Dissipation

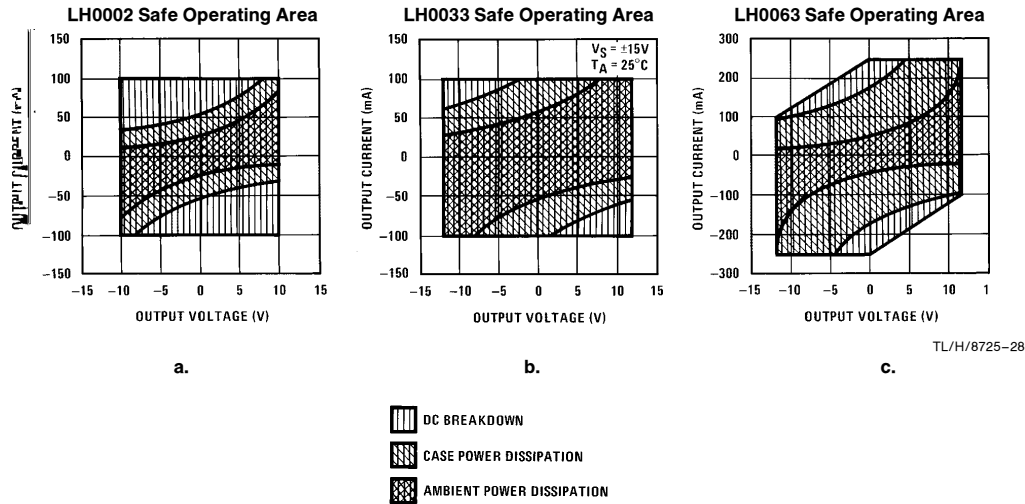


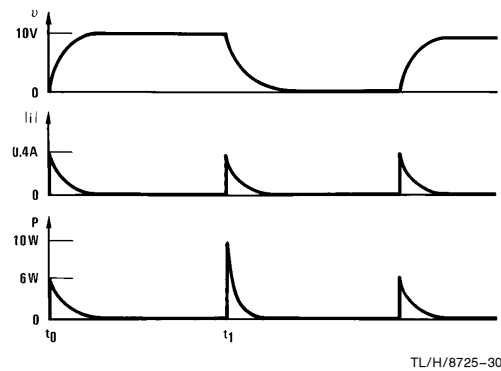
FIGURE 18. Safe Operating Areas at 25°C and $V_S = \pm 15\text{V}$

Peak Power Dissipation

An often overlooked power dissipation factor exists when driving a reactive load. Consider the LH0002 with a possible 400 mA peak current drive capability when driving 10V square pulses into 1000 pF. At the rising edge, the upper device transistor charges the capacitor at its limiting current. The charging waveform is not linear, in fact it approaches a logarithmic curve because the resistor $R1/\beta3$ appears as the principal value of charging resistance [see equation (2)]. The instantaneous power dissipation is simply the product of V^+ and $I_{O(MAX)}$, or 6W, with occurrences at the positive and negative leading edges. Once the load capacitor is charged, the negative leading edge instantaneous peak power is somewhat greater because the power dissipated in the lower output transistor is $(V_O - V^-) I_O = 25I_O$. The PNP pull-down transistor has slightly lower β , limiting peak current to less than 400 mA, therefore the peak negative edge power is just under 10W in this instance.

Figure 19 indicates the output voltage and current relationships as well as the power dissipation versus time for the pulse waveform into a capacitive load.

Obviously, the average power dissipation under peak current drive conditions is dependent upon the pulse repetition frequency, and becomes increasingly dominant as the PRF increases.



PEAK POWER

$$P_{t0} = (15V - 0V) (0.4A)$$

$$= 6 W_{PEAK}$$

$$P_{t1} = [10V - (-15V)] (0.4A)$$

$$= 10 W_{PEAK}$$

FIGURE 19. Peak Power Dissipation Into Pure Capacitive Load

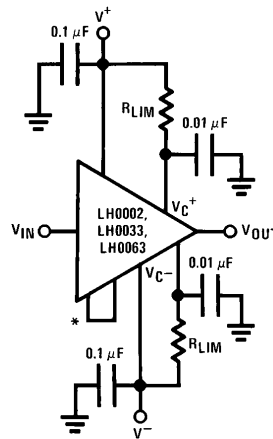
Because each of the buffer amplifiers may be operated on dissimilar supply voltages for input and output stages, device power dissipation is reduced by lowering the output stage supply voltages while retaining the input stage supplies at a higher level for best current driving capability. The limiting factor is, of course, a reduced output voltage swing.

Current Limiting

Current limiting may be provided in either of two ways: by adding series resistors at the collectors of the output stage, or by a single series resistor at the buffer output. The first method (Figure 20) is preferred as there is little effect on output resistance and peak current drive. However, the output voltage swing is reduced by the voltage drop across these resistors. Their value is determined as follows:

$$R_{LIM} = \frac{V^+}{I_{SC}^+}, \frac{V^-}{I_{SC}^-} \quad (11)$$

where $I_{SC} = 100$ mA for LH0002 and LH0033, and 250 mA for LH0063.



*LH0033 and LH0063 only

FIGURE 20. Current Limiting using Collector Resistors

Capacitive Loads

All three devices are capable of driving relatively high capacitive loads. Because capacitive loads on emitter-followers are reflected to the input as negative resistances, it is necessary to add some series compensating positive real resistance; 50Ω – 300Ω is usually sufficient. An alternative is to insert the current limiting resistor at the output as shown in *Figure 22*. This will isolate the capacitive load from the buffer.

Any of the buffers can drive twisted pair, shielded or coaxial cables, or other reactive loads. For all practical purposes, an unterminated coaxial cable presents a capacitive load to the driver. On the other hand, terminated coaxial cables appear as resistive loads, and therefore may not require the compensation for capacitive loads. Don't forget consideration of peak power dissipation when driving cable loads, since they may represent capacitive loads (see section on Peak Power Dissipation).

Offset Voltage and Adjustment

Offset voltage is measured with $V_{IN} = 0$. As V_{IN} and I_L are increased, the apparent offset voltage will change. This is due primarily to a gain which is less than unity (inherent in an emitter-follower). The effect of this is discussed in detail in the section on Circuit Description. Both the LH0033 and LH0063 have provisions for offset voltage adjustment. When not required, the OFFSET ADJUST pins of these two devices should be shorted. When adjustment is desired, they should be open-circuited, and the external adjustment

is accomplished with a 200Ω variable resistor inserted between V^- and pin 7 of the LH0033 or pin 6 of the LH0063. It is good practice to insert a 20Ω resistor in series with the variable resistor to limit excessive power dissipation at the input stage when the pot is at minimum value. The offset adjustment range is typically ± 400 mV.

When a buffer amplifier is used as a current booster in conjunction with an operational amplifier, as in *Figure 22*, there is usually no need for output offset adjustment, since the offset is reduced by the open-loop to closed-loop gain ratio. The total offset of the closed-loop circuit is:

$$V_{OS(TOTAL)} = V_{IOS} \pm V_{OOS} \frac{A_{CL}}{A_{OL}} \quad (12)$$

where: V_{IOS} = input offset voltage.

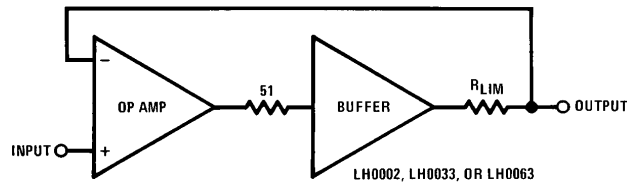
V_{OOS} = buffer offset voltage.

Slew Rate

Slew rate is the rate of change of output voltage for large-signal step input changes. For resistive load, slew rate is limited by internal circuit capacitance and operating current. *Figure 23* shows the slew capabilities of the buffers under large-signal input conditions.

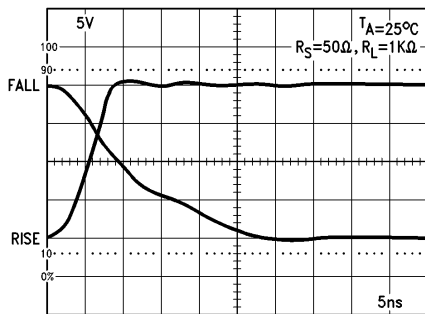
However, when driving capacitive load, the slew rate may be limited by available peak output current according to the following expression.

$$dv/dt = I_{pk}/C_L \quad (13)$$



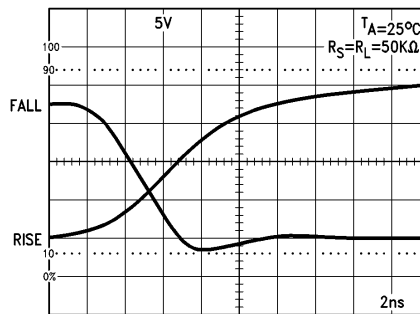
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FIGURE 22. Current Limiting Inside an Amplifier/Buffer Loop



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a. LH0033 Slew Response



TL/H/8725-36

b. LH0063 Slew Response

FIGURE 23. Positive and Negative Slew of Each Buffer

Note that the peak current available to the load decreases as C_L changes [see equation (2)]. Figure 24 illustrates the effect of the load capacitance on slew rate for the three buffers. Slew rate tests are specified for resistance and/or very small capacitance load, otherwise the slew rate test would be a measure of the available output current. For highest slew rate, it is obvious that stray load capacitance should be minimized.

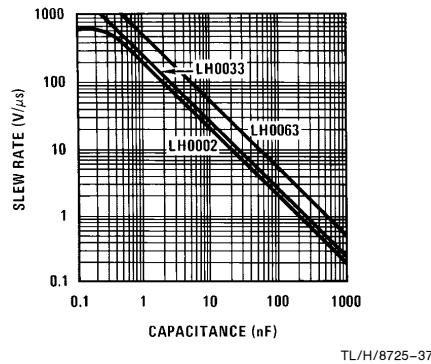
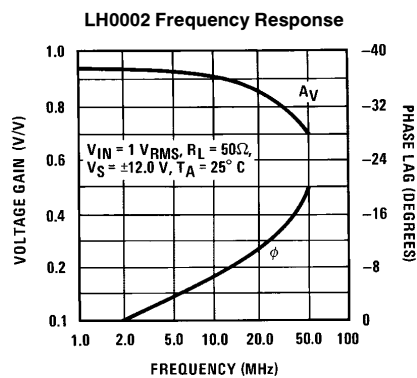


FIGURE 24. Slew Rate vs Load Capacitance

Distortion

The output stage of the three buffer amplifiers are biased at 1 mA to 10 mA to remove any possibility of crossover

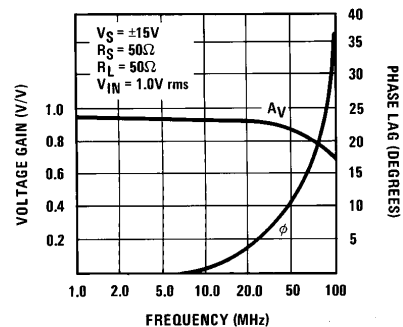


distortion. The LH0063 may exhibit a small amount of crossover distortion in some circumstances due to the relatively low 1 mA output stage bias. The heavy local feedback inherent in emitter-follower or source-follower operation provides a very low distortion output. The remaining distortion (<0.1%) is primarily due to the modulation effect of non-constant V_{CE} as the output voltage changes.

Closed-Loop Feedback Operation

Any of the buffer amplifiers may be used inside an op amp feedback loop. When this is done, the additional phase lag introduced by the buffer must be included in loop stability consideration. With most op amps, the bandwidth of these buffers is so great that the op amp totally controls the loop stability. However, when using very wide-band op amps such as the LH0024, LH0032, and LH0062, the small additional phase lag of the buffers should be taken into consideration. Figure 25 presents the Bode plots of gain and phase for the three buffers. The phase margin and open loop frequency response is altered by the additional pole(s) contributed by the buffer. The buffer phase shift is algebraically summed with the op amp phase shift, and may cause a stable op amp loop to become marginally stable depending upon the relative positions of the op amp and buffer poles. In general, the buffer bandwidth should significantly exceed that of the op amp, so that the loop performance will be determined solely by the op amp.

LH0033 Frequency Response



LH0063 Frequency Response

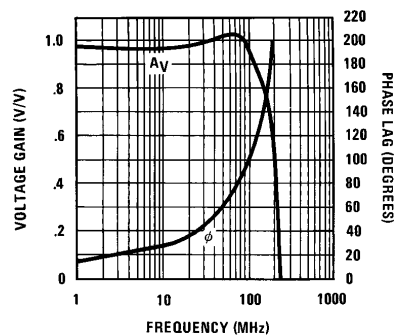


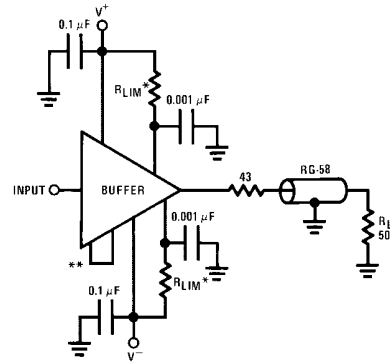
FIGURE 25. Phase-Gain Relationships of Buffers

III. APPLICATIONS CIRCUITS

Because of their high current drive capability, the LH0002, LH0033 and LH0063 buffer amplifiers are suitable for driving terminated or unterminated coaxial cables, and high current or reactive loads. Current limiting resistors should be used to protect the device from excessive peak load currents or accidental short circuit. There is no current limiting built into the devices other than that imposed by the limited beta of the output transistors. Figure 26 shows a coaxial cable drive circuit. The 43Ω resistor matches the driving source to the cable; however, its inclusion will rarely result in visible improvement in pulse response into a terminated cable. If the 43Ω resistor is included, the output voltage to the

load is about half what it would be without the near end termination.

The LH0033 and LH0063 are useful in high speed sample-and-hold or peak detector circuits because of their very high speed and low-bias-current FET input stages. The high speed peak detector circuit shown in Figure 27 could be changed to a sample-and-hold circuit simply by removing the detector diode and the reset circuitry. For best accuracy, the circuit offset may be trimmed with the 10 kΩ offset adjustment pot shown. The circuit has a typical acquisition time of 900 ns, to 0.1% of final value for 10V input step signal, and a droop rate of 100 μV/ms. Even faster acquisition time can be achieved by reducing the hold capacitor value.



*For: LH0002, $R_{LIM} = 100\Omega$, 1W
LH0033, $R_{LIM} = 100\Omega$, 1W
LH0063, $R_{LIM} = 60\Omega$, 5W
**Jumper for LH0033 and LH0063 only.

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FIGURE 26. Coaxial Cable Drive Circuit

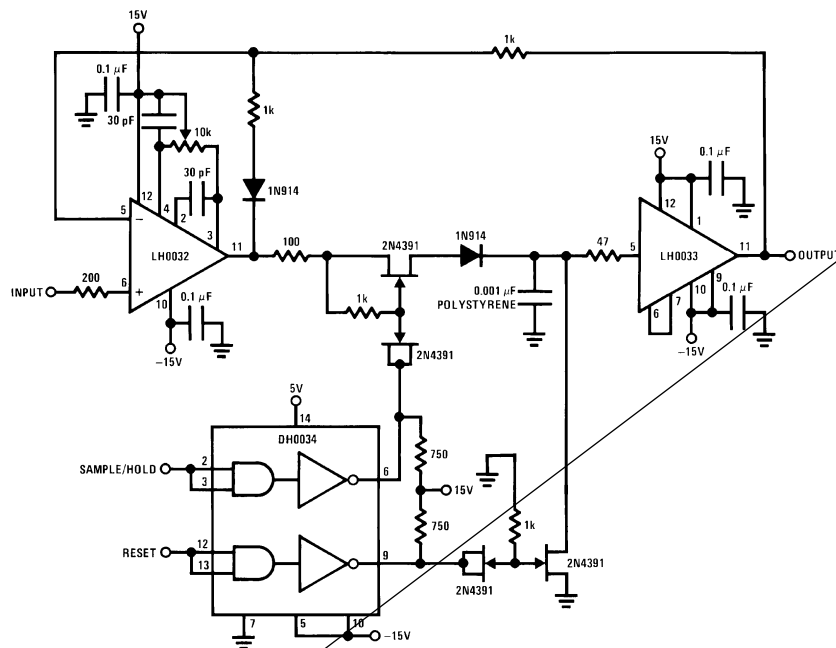


FIGURE 27. High Speed Peak Detector with Hold and Reset Controls

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The LH0033 may be used as a cable-shield driver as shown in *Figure 28*. The advantage is that the source driver is not required to charge the line capacitance of the unterminated coaxial cable, and indeed does not need to match its line impedance; therefore, high speed data transmission is permitted.

The buffers may be used with a single supply without special considerations. A typical application is shown in *Figure 29*. The input is DC biased to mid-operating point and is AC coupled. Its input impedance is approximately 500 k Ω at low frequencies. Note that for DC loads referenced to ground, the quiescent current is increased by the load current set at the input DC bias voltage.

The high input impedance of the LH0033 and LH0063 are suitable for active filter applications. A basic two pole, high pass filter is diagrammed in *Figure 30* using the LH0033. The circuit provides a 10 MHz cutoff frequency. One consideration of the filter is its apparent gain change due to the finite output impedance of the amplifier, which affects the overall gain and the damping factor of the filter stage. Resistor R3 ensures that the input capacitance of the amplifier does not interact with the filter response at the frequency of interest.

An equivalent low pass filter is similarly obtained by capacitance and resistance transformation.

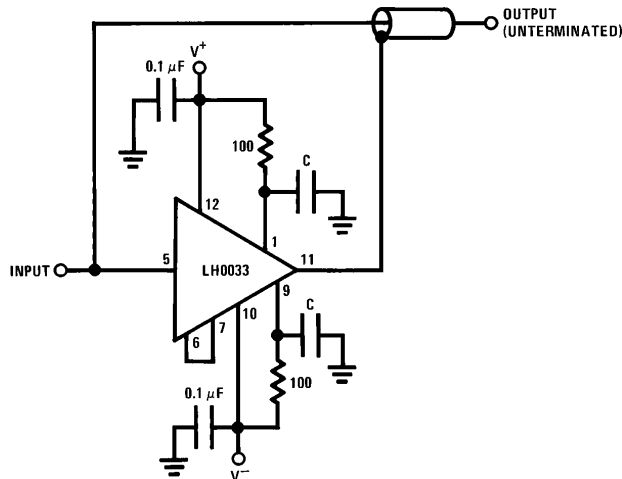


FIGURE 28. High Speed Shield/Line Driver

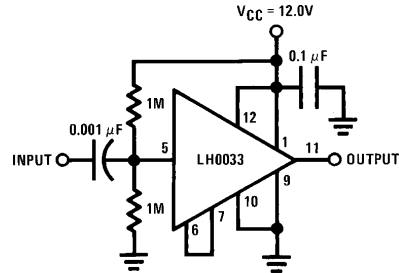


FIGURE 29. Single Supply AC Buffer Amplifier

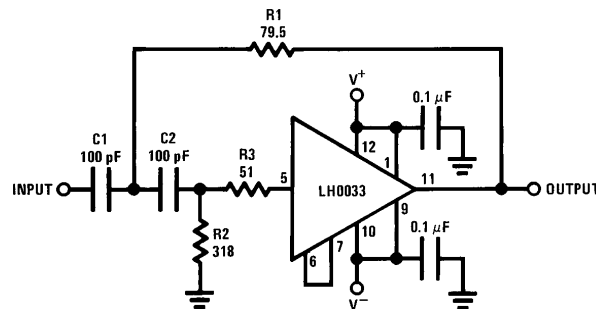


FIGURE 30. Wide Band Two Pole High Pass Filter

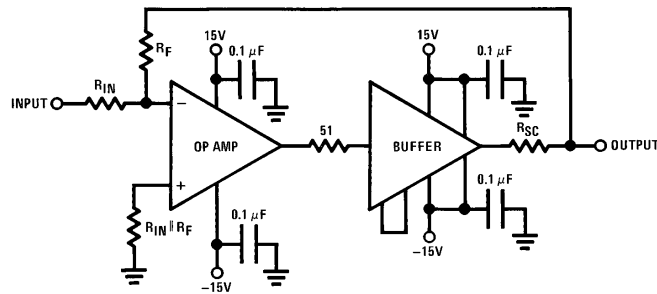
The most common use of the buffers is inside an op amp feedback loop as shown in *Figure 31*. The chart in the figure shows the ideal match of the buffer family to most popular operational amplifiers.

REFERENCES

George S. Moschytz, "Linear Integrated Networks Design," Ch. 3, Active Filter Building Blocks.

"Application of the LH0002 Current Amplifier," National Semiconductor Corporation, AN-13, September 1968.

B. Siegel and L. Van Der Gaag, "Applications For a New Ultra-High Speed Buffer," National Semiconductor Corporation, AN-48, August 1971.



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Op Amp	Recommended Buffer
LM101, LM108, LM741, LF151	LH0002
LH0022, LH0042, LH0052	
LF155, LF156, LF157, LH0024, LH0032	LH0033 $R_{SC} \frac{V_S}{I_{SC}}$
LH0024, LH0032	LH0063

FIGURE 31. Using Voltage Follower as Output Buffer

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
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National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
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