HCMOS Gates Make Frequency multipliers

The rapid edges produced by HCMOS logic ICs are rich in harmonics which can be selectively tuned to make simple frequency multipliers. The desired harmonic may be selected in a number of ways but a few points should be observed. First, the tuning network should not present an excessive capacitive load to the output of the IC and it is recommended that a series current limiting resistor be included. Second, a DC path to ground should be avoided to conserve power. And third, the network should provide good filtering with emphasis placed on the rejection of low frequencies.

Fig. 1 shows a simple multiplier employing two HCMOS inverters. The first inverter produces a harmonic-rich squarewave which is applied to a resistor divider. The divider ensures that the IC is not too heavily loaded and it presents a low impedance to the series tuned circuit that follows to preserve the Q factor. In this application the tuned circuit is tuned to 30MHz (a multiplication factor of 5).

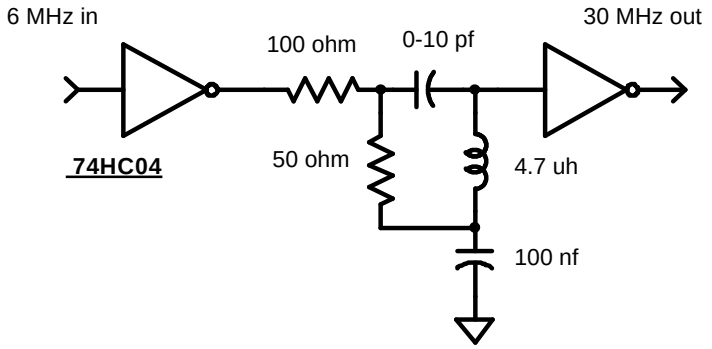

Figure 1: 6 MHz to 30 MHz multiplier with squarewave output.

DC bias for the following gate is provided through the tank inductor from a bypass capacitor which charges to V/2. The tank will have sufficiently high Q if the capacitor is selected to have an impedance of about 1000 ohms at the multiplied frequency. AC gates will work well at higher frequencies but lower Q may be desired to make the value of C a bit larger. The resonating inductor's reactance will be somewhat lower since it must resonate the capacity of the IC input (typically about 4pf for AC). These simplified equations include these assumptions for 1000 ohm reactance:

$$L = 160 / (f + 25 \times 10^{-9} f^2)$$

$C = 160 \times 10^{-6} / f$ where f is the harmonic frequency. (Increase C and decrease L for lower Q.)

The input and output circuits of the multiplier will vary depending on the application. If the input is a sinewave larger than about 1 volts p-p the input may be simply capacitively coupled with a resistor divider to bias the gate. Offset the bias voltage slightly so that the gate is either high or low in the absence of input signal unless the signal will always be present. The output may be converted to a sinewave by using a tuned impedance matching network. An additional network similar to the harmonic selection network shown in fig. 1 is a good choice for the output since it provides a resistive load to the output gate, rejects low frequencies, and generates a large sinewave at the center of the series resonant tank. A low impedance output (50 ohms, etc.) may be achieved by attaching a very small capacitor (about 1 pf) to the top of the 4.7 uh choke as shown in fig. 2.

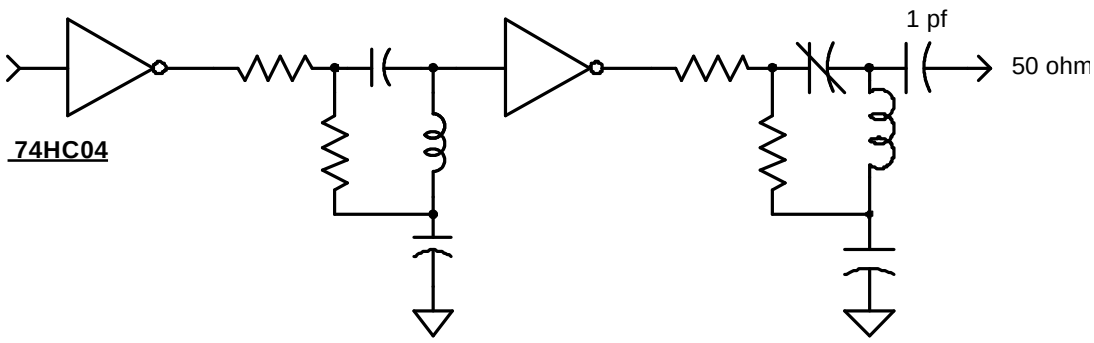

Figure 2: 6 MHz to 30 MHz multiplier with sinewave output.

Note that the output network is tuned to the same frequency as the multiplier network unless two stages of multiplication are desired. The second gate may be left out if a low-level sinewave is adequate.

The frequency synthesizer depicted in fig. 3 illustrates how flip-flops can be used to divide and multiply simultaneously to achieve fractional multiplication factors.

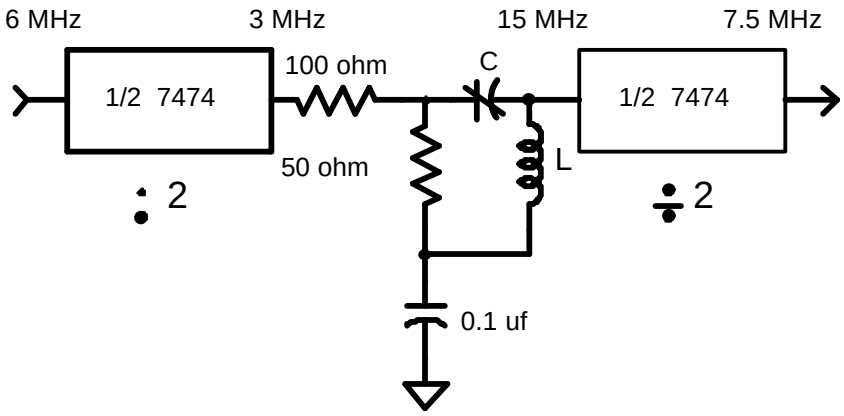

Figure 3 : 6 MHz to 7.5 MHz multiplier

This synthesizer uses a single 7474 flip-flop to convert a 6 MHz input to 7.5 MHz (a multiplication factor of 1.25). The 6 MHz square wave from a clock oscillator is divided by one of the flip-flops and applied to a network similar to fig. 1. The fifth harmonic of 3 MHz (15 MHz) is divided by the second flip-flop to produce 7.5 MHz.

Fig. 4 shows a gated-output multiplier using two nand gates. Network values are selected as before. Gated multipliers are useful when a high on-off ratio at the output frequency is desired since stopping the multiplication process essentially eliminates the frequency. For the best performance choose non-inverting gates since the output will be connected to ground through a very low impedance when the multiplier is off reducing the opportunity for harmonics from other stages to find their way into the output tank via the power buss.

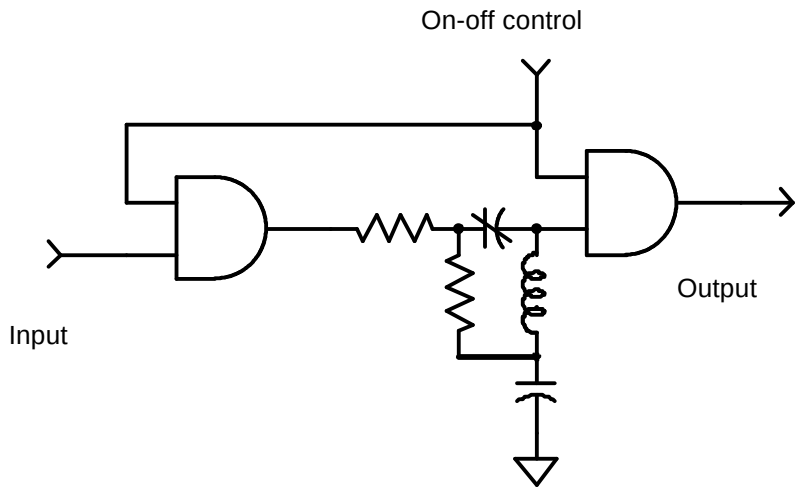

Figure 4 : Gated multiplier exhibiting good on-off ratio.

Here are some additional ideas for experimentation:

By adding a tuned circuit in series with the CMOS output the feed point into a filter can be at a much lower impedance taking advantage of the low output impedance of the CMOS resulting in more output. (The series tank prevents the CMOS from seeing too heavy a load at the fundamental frequency.)

Several gates may be paralleled for increased output. Connect small resistors in series with each output before connecting them.

HCMOS will run with supply voltages as low as two volts and although the signals will be smaller and the device somewhat slower, the power savings will be noticeable.

The output of two gate multipliers may feed the two inputs to an exclusive-or to generate sum or difference frequencies for more complex synthesis. A quad exclusive-or will do the whole job leaving a gate to amplify the output.